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# FDS3672

# N-Channel PowerTrench<sup>®</sup> MOSFET 100V, 7.5A, 22m $\Omega$

### **Features**

- $r_{DS(ON)} = 19m\Omega$  (Typ.),  $V_{GS} = 10V$ ,  $I_D = 7.5A$
- $Q_q(tot) = 28nC (Typ.), V_{GS} = 10V$
- Low Miller Charge
- Low Q<sub>RR</sub> Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

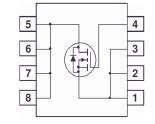
## **Applications**

- DC/DC converters and Off-Line UPS
- · Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- · High Voltage Synchronous Rectifier

Formerly developmental type 82763



SO-8 MOSFET Maximum Ratings  $T_A = 25$ °C unless otherwise noted



Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain to Source Voltage	100	V
$\frac{V_{DSS}}{V_{GS}}$	Gate to Source Voltage	±20	V
I <sub>D</sub>	Drain Current		
	Continuous ( $T_A = 25^{\circ}C$ , $V_{GS} = 10V$ , $R_{\theta JA} = 50^{\circ}C/W$ )	7.5	Α
	Continuous ( $T_A = 100$ °C, $V_{GS} = 10V$ , $R_{\theta JA} = 50$ °C/W)	4.8	А
	Pulsed	Figure 4	А
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 1)	416	mJ
P <sub>D</sub>	Power dissipation	2.5	W
	Derate above 25°C	20	mW/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature	-55 to 150	°C

# **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 10 seconds (Note 3)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	85	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	°C/W

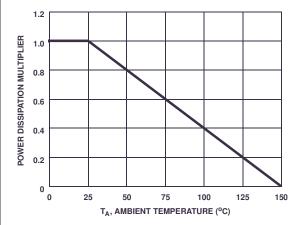
# **Package Marking and Ordering Information**

<b>Device Marking</b>	Device	Package	Reel Size	Tape Width	Quantity
FDS3672	FDS3672	SO-8	330mm	12mm	2500 units

Symbol	Parameter	Test Conditions		Тур	Max	Units
Off Chara	cteristics	•	•			
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100	l -	_	V
D VD 55	Drain to course Broakaswii Voltage	V <sub>DS</sub> = 80V	-	_	1	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0V$ $T_C = 150$		-	250	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20V$	-	-	±100	nA
		40				
	cteristics	N N 1 050 A		1	1 4	
V <sub>GS(TH)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu A$	2	-	4	V
		$I_D = 7.5A, V_{GS} = 10V$	-	0.019	0.023	
r <sub>DS(ON)</sub>	Drain to Source On Resistance	$I_D = 6.8A, V_{GS} = 6V$	-	0.023	0.028	Ω
·DS(ON)		$I_D = 7.5A, V_{GS} = 10V,$ $T_C = 150^{\circ}C$	-	0.035	0.043	
Dynamic	Characteristics					
C <sub>ISS</sub>	Input Capacitance		-	2015	-	рF
C <sub>OSS</sub>	Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$	-	285	-	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance	f = 1MHz	-	70	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V <sub>GS</sub> = 0V to 10V	-	28	37	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 2V$ $V_{DD} = 50$	v -	4	6	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	I <sub>D</sub> = 7.5A		10	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau	$I_{g} = 1.0 \text{m}$	Α	6.8	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	6	-	nC
	Characteristics (V <sub>GS</sub> = 10V)	·	•	•		
t <sub>ON</sub>	Turn-On Time		-	-	51	ns
t <sub>d(ON)</sub>	Turn-On Delay Time		-	14	-	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 50V, I_{D} = 4A$	-	20	-	ns
t <sub>d(OFF)</sub>	Turn-Off Delay Time	$V_{GS} = 10V, R_{GS} = 10\Omega$	-	37	-	ns
t <sub>f</sub>	Fall Time			27	-	ns
t <sub>OFF</sub>	Turn-Off Time		-	-	96	ns
	rce Diode Characteristics		'			
		I <sub>SD</sub> = 7.5A	-	-	1.25	V
$V_{SD}$	Source to Drain Diode Voltage	I <sub>SD</sub> = 4A	-	-	1.0	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>SD</sub> = 7.5A, dI <sub>SD</sub> /dt= 100A/μ	s -	-	55	ns
Q <sub>RR</sub>	Reverse Recovered Charge	I <sub>SD</sub> = 7.5A, dI <sub>SD</sub> /dt= 100A/μs		-	90	nC

Notes:
 1: Starting T<sub>J</sub> = 25°C, L = 13mH, I<sub>AS</sub> = 8A.
 2: R<sub>θ,JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θ,JC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.
 3: R<sub>θ,JA</sub> is measured with 1.0 in<sup>2</sup> copper on FR-4 board





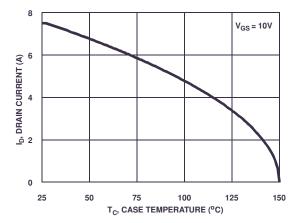


Figure 1. Normalized Power Dissipation vs Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

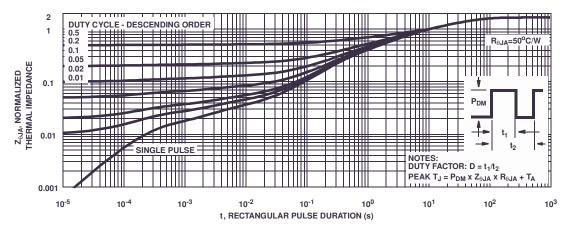


Figure 3. Normalized Maximum Transient Thermal Impedance

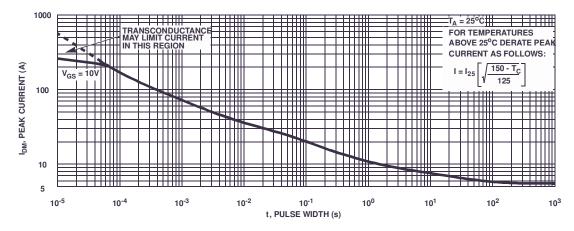


Figure 4. Peak Current Capability

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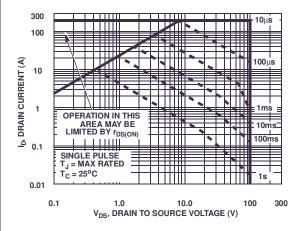


Figure 5. Forward Bias Safe Operating Area

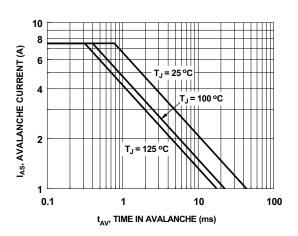


Figure 6. Unclamped Inductive Switching Capability

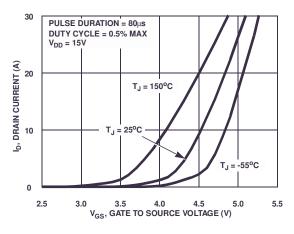


Figure 7. Transfer Characteristics

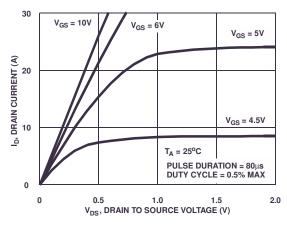


Figure 8. Saturation Characteristics

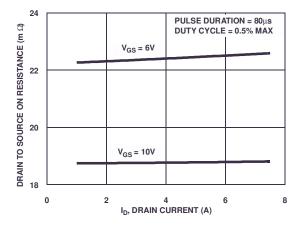


Figure 9. Drain to Source On Resistance vs Drain Current

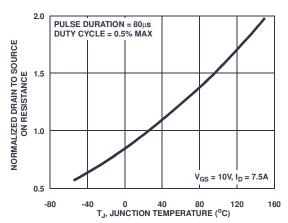


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

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# Typical Characteristics $T_A = 25$ °C unless otherwise noted

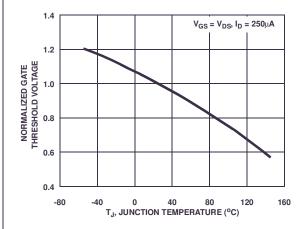


Figure 11. Normalized Gate Threshold Voltage vs
Junction Temperature

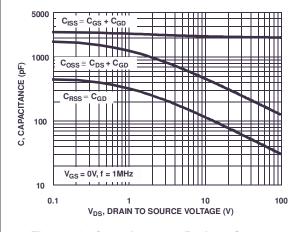


Figure 13. Capacitance vs Drain to Source Voltage

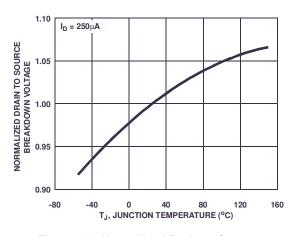


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

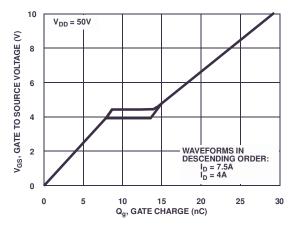
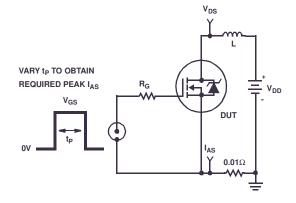


Figure 14. Gate Charge Waveforms for Constant Gate Currents

# **Test Circuits and Waveforms**



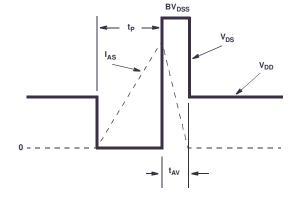


Figure 15. Unclamped Energy Test Circuit

Figure 16. Unclamped Energy Waveforms

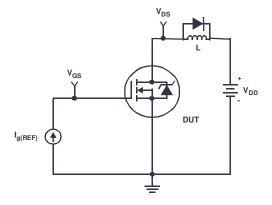


Figure 17. Gate Charge Test Circuit

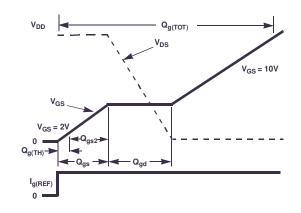


Figure 18. Gate Charge Waveforms

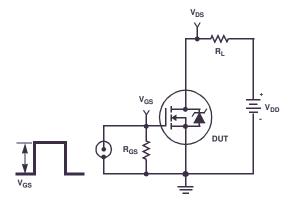


Figure 19. Switching Time Test Circuit

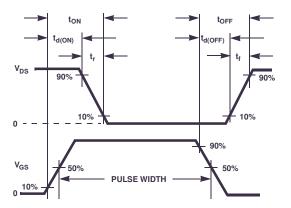


Figure 20. Switching Time Waveforms





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