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PSMN015-100YL

N-channel 100 V, 15 m Ω logic level MOSFET in LFPAK56 Product data sheet

1. **General description**

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

2. **Features and benefits**

- Advanced TrenchMOS provides low R_{DSon} and low gate charge
- Logic level gate operation
- Avalanche rated, 100 % tested
- LFPAK provides maximum power density in a Power SO8 package

Applications 3.

- Synchronous rectification in power supply equipment
- Chargers & adaptors with V_{out} < 10 V
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	100	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	69	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	195	W
Static charact	eristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 20 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$		-	12.1	15	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I _D = 20 A; V _{DS} = 80 V; V _{GS} = 5 V; Fig. 13; Fig. 14		-	16	-	nC



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	[d	G T A
4	G	gate	و و و و	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN015-100YL	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669		

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN015-100YL	15L100

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	195	W
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u>	-	69	Α
		V _{GS} = 5 V; T _{mb} = 100 °C; <u>Fig. 2</u>	-	49	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$; Fig. 3	-	274	Α
T _{stg}	storage temperature		-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
Tj	junction temperature			-55	175	°C
Source-dra	in diode	'				
I _S	source current	T _{mb} = 25 °C		-	69	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	274	Α
Avalanche	ruggedness	'	1			
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 69 A; $V_{sup} \le 100$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[1][2]	-	110	mJ

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.

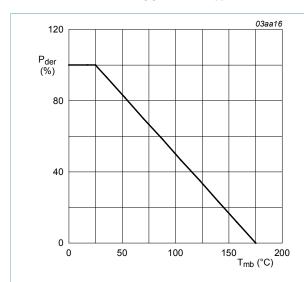


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

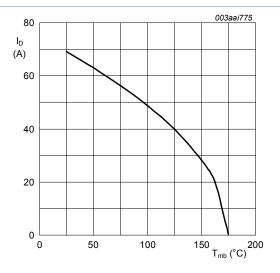


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$

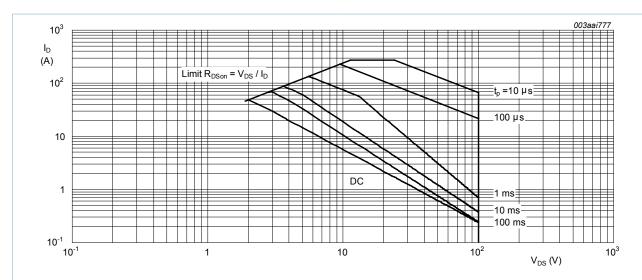
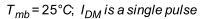


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



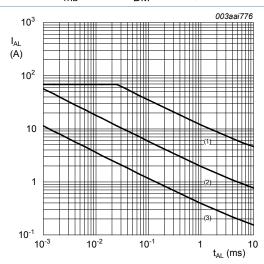


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1)
$$T_{j(init)} = 25$$
°C; (2) $T_{j(init)} = 150$ °C; (3) Repetitive Avalanche

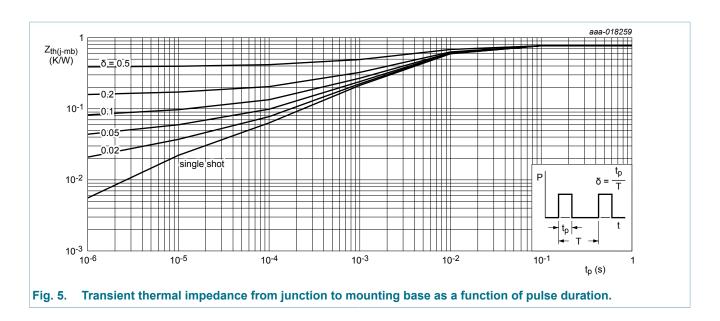
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	0.77	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		'			
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^{\circ}C$	100	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9;$ Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA; } V_{DS} = V_{GS}; T_j = -55 \text{ °C; } Fig. 9$	-	-	2.45	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; <u>Fig. 9</u>	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.11	10	μΑ
	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μΑ	
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state	$V_{GS} = 5 \text{ V}; I_D = 20 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$	-	12.1	15	mΩ
	resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 11	-	11.6	14.7	mΩ
		V _{GS} = 5 V; I _D = 20 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	41.4	mΩ
Dynamic ch	naracteristics		,	'		
Q _{G(tot)} t	total gate charge	I _D = 20 A; V _{DS} = 80 V; V _{GS} = 10 V; Fig. 13; Fig. 14	-	86.3	-	nC
		I _D = 20 A; V _{DS} = 80 V; V _{GS} = 5 V;	-	45.8	-	nC
Q_{GS}	gate-source charge	Fig. 13; Fig. 14	-	11	-	nC
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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Q_{GD}	gate-drain charge			-	16	-	nC
C _{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$		-	4604	6139	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>		-	269	323	pF
C _{rss}	reverse transfer capacitance			-	156	213	pF
t _{d(on)}	turn-on delay time	V_{DS} = 80 V; R_L = 4 Ω ; V_{GS} = 5 V;		-	21	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$		-	32	-	ns
t _{d(off)}	turn-off delay time			-	85	-	ns
t _f	fall time			-	59	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 20 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 ^{\circ}\text{C}$; Fig. 16		-	0.8	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	44	-	ns
Q _r	recovered charge	V _{DS} = 25 V		-	79	-	nC

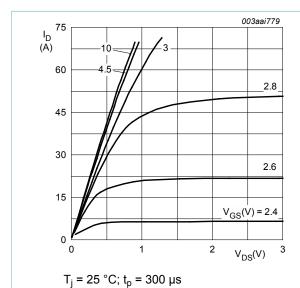


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

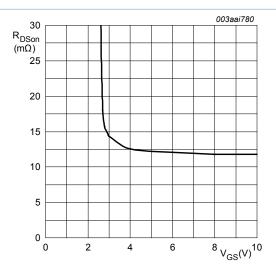


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 20A$$

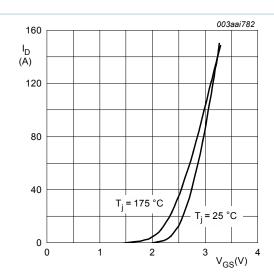


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



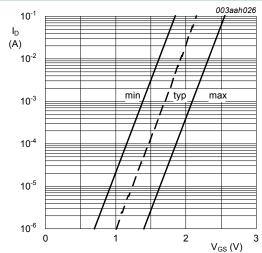


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

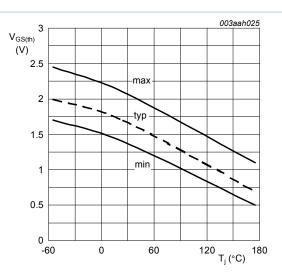
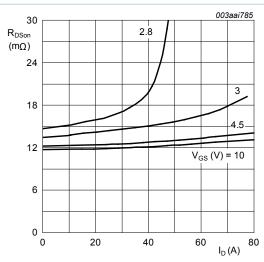


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D$$
 = 1 mA; V_{DS} = V_{GS}



 $T_i = 25 \,^{\circ}\text{C}; t_p = 300 \,\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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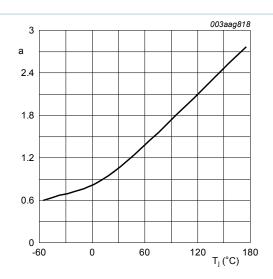


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25 °C)}}$$

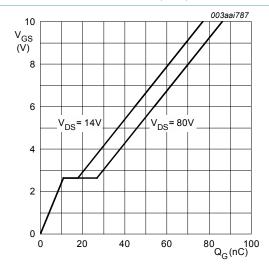


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_i = 25$$
°C; $I_D = 20A$

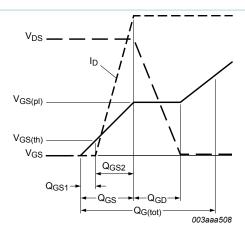


Fig. 13. Gate charge waveform definitions

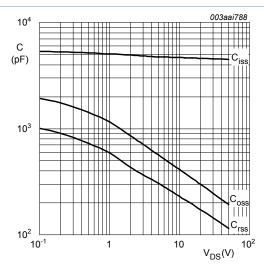


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V$$
; $f = 1MHz$

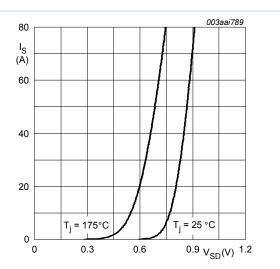


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

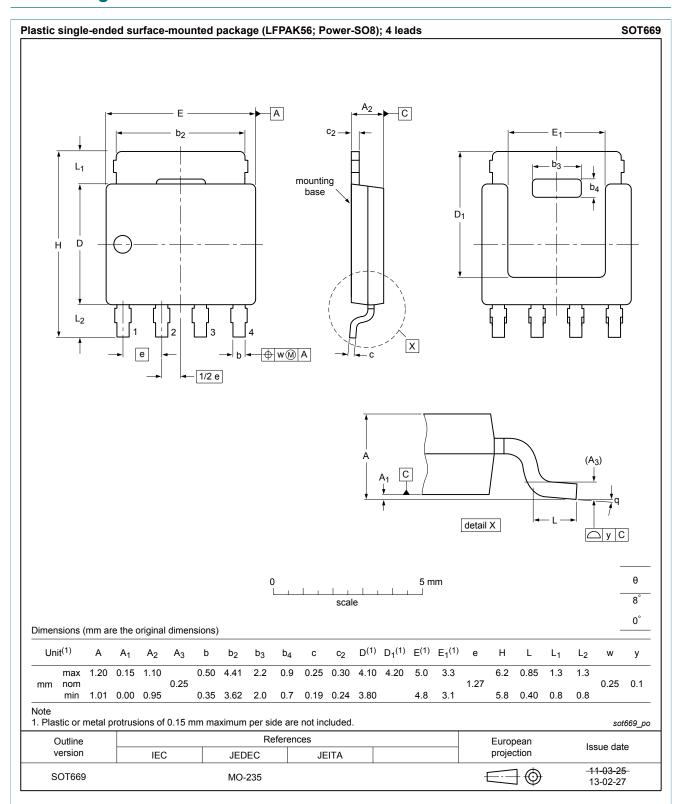


Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

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