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PSMN1R9-40PL

N-channel 40 V, 1.7 mΩ logic level MOSFET in SOT78

1 February 2013 Product data sheet

1. General description

Logic level N-channel MOSFET in SOT78 using TrenchMOS technology. Product design and manufacture has been optimized for use in battery operated power tools.

2. Features and benefits

- High efficiency due to low switching & conduction losses
- Robust construction for demanding applications
- Logic level gate

3. Applications

- Battery-powered tools
- Load switching
- Motor control
- Uninterruptible power supplies

4. Quick reference data

Table 1. Quick reference data

Cumbal	Devenueter	Conditions		Miles	Trees	Mare	1.1 14
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 1</u>	[1]	-	-	150	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	349	W
Static charac	teristics						
R _{DSon}	drain-source on-state	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C;		-	1.4	1.7	mΩ
	resistance	Fig. 11					
Dynamic char	racteristics						
$Q_{G(tot)}$	total gate charge	V_{GS} = 10 V; I_D = 25 A; V_{DS} = 32 V;		-	230	-	nC
Q_{GD}	gate-drain charge	Fig. 13; Fig. 14		-	40.9	-	nC
Avalanche ru	ggedness						
E _{DS(AL)S}	non-repetitive drain-	I_D = 150 A; $V_{sup} \le 40$ V; R_{GS} = 50 Ω;		-	-	801.1	mJ
	source avalanche	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped;					
	energy	Fig. 3					

^[1] Continuous current is limited by package.



N-channel 40 V, 1.7 m Ω logic level MOSFET in SOT78

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D I
2	D	drain	├	
3	S	source	1 2 3 TO 220AB (SOT78)	mbb076 S
			TO-220AB (SOT78)	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PSMN1R9-40PL	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78			

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R9-40PL	PSMN1R9-40PL

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I _D	drain current	T _{mb} = 100 °C; V _{GS} = 10 V; <u>Fig. 1</u>	[1]	-	150	Α
		T _{mb} = 25 °C; V _{GS} = 10 V; <u>Fig. 1</u>	[1]	-	150	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 4		-	1332	А

PSMN1R9-40PL

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N-channel 40 V, 1.7 m Ω logic level MOSFET in SOT78

Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	349	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain	diode					
I _S	source current	T _{mb} = 25 °C	[1]	-	150	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	1332	Α
Avalanche ru	ggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 150 A; $V_{sup} \le 40$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3		-	801.1	mJ

[1] Continuous current is limited by package.

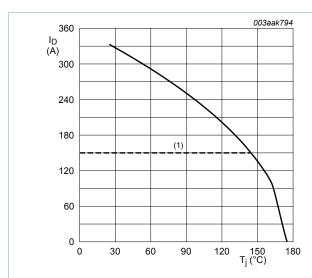


Fig. 1. Continuous drain current as a function of mounting base temperature

 $\label{eq:VGS} V_{\textit{GS}} \! \geq \! 10V$ (1) Capped at 150A due to package

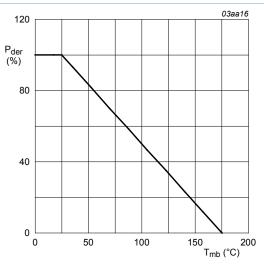


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \,\%$$

N-channel 40 V, 1.7 m Ω logic level MOSFET in SOT78

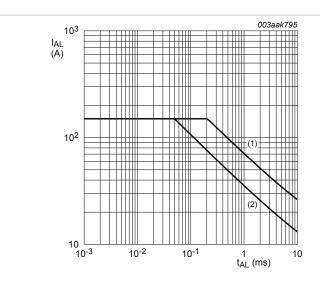
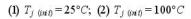


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time



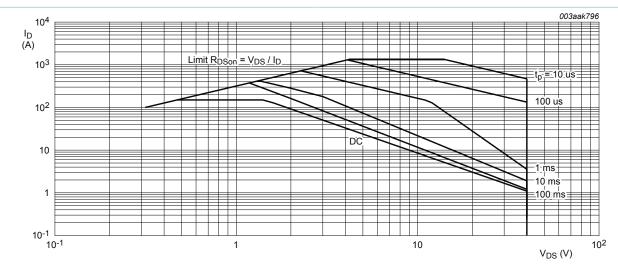


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

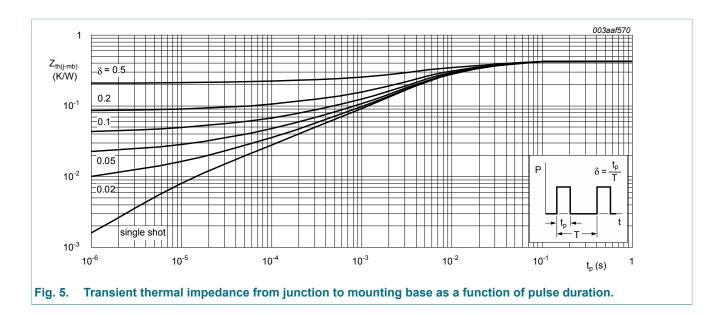
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	0.35	0.43	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

PSMN1R9-40PL

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N-channel 40 V, 1.7 m Ω logic level MOSFET in SOT78



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					_
V _{(BR)DSS}	drain-source	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	40	-		V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V
I _{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.13	1	μΑ
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	1.4	1.7	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 11	-	1.65	1.94	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	3.15	mΩ
R _G	gate resistance	f = 1 MHz	0.38	0.76	1.52	Ω

N-channel 40 V, 1.7 m Ω logic level MOSFET in SOT78

Symbol	Parameter	Conditions	Mir	Тур	Max	Unit
Dynamic cl	naracteristics			l l		
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 5 V; Fig. 13; Fig. 14	-	120	-	nC
		I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V;	-	230	-	nC
Q _{GS}	gate-source charge	Fig. 13; Fig. 14	-	26.9	-	nC
Q_{GD}	gate-drain charge	_	-	40.9	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; <u>Fig. 15</u>	-	13200	-	pF
C _{oss}	output capacitance		-	1530	-	pF
C _{rss}	reverse transfer capacitance		-	740	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	95	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	118	-	ns
t _{d(off)}	turn-off delay time	_	-	195	-	ns
t _f	fall time	_	-	119	-	ns
Source-dra	in diode	1				
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$	-	0.77	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	57	-	ns
Q _r	recovered charge	V _{DS} = 25 V	-	97	-	nC

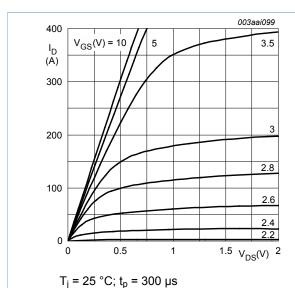


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

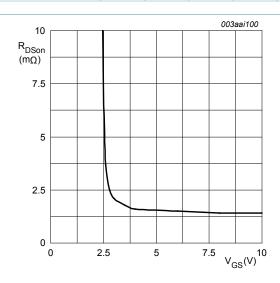


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; \ I_D = 25A$$

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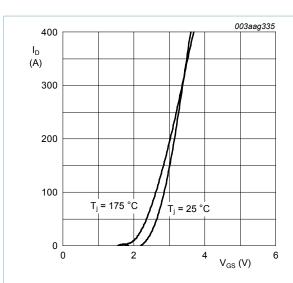


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



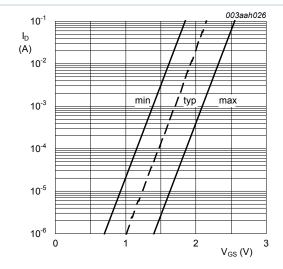


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25$$
°C; $V_{DS} = 5V$

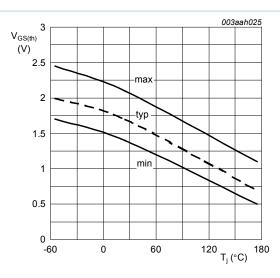
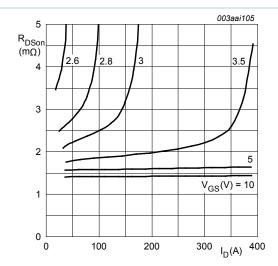


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1$$
 mA; $V_{DS} = V_{GS}$



 $T_i = 25 \,^{\circ}\text{C}; t_p = 300 \,\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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N-channel 40 V, 1.7 m Ω logic level MOSFET in SOT78

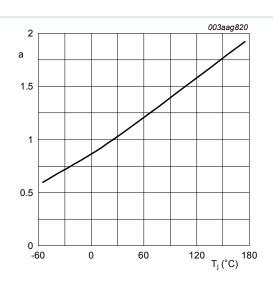


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\mathbf{a} = \frac{R_{DSon}}{R_{DSon(25, C)}}$$



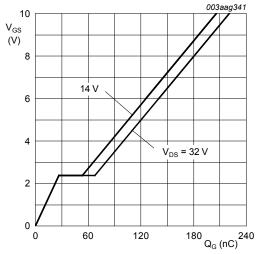


Fig. 14. Gate-source voltage as a function of gate charge; typical values

 $T_i = 25 \,^{\circ}C; I_D = 25 \,^{\circ}A$

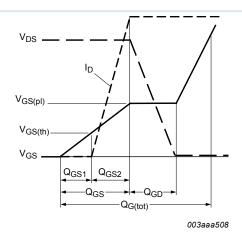


Fig. 13. Gate charge waveform definitions

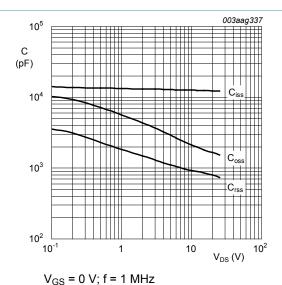
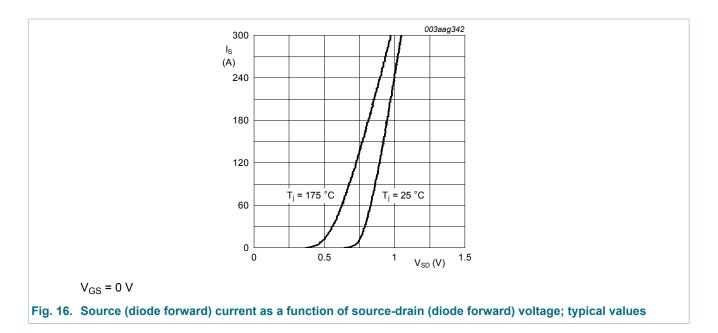
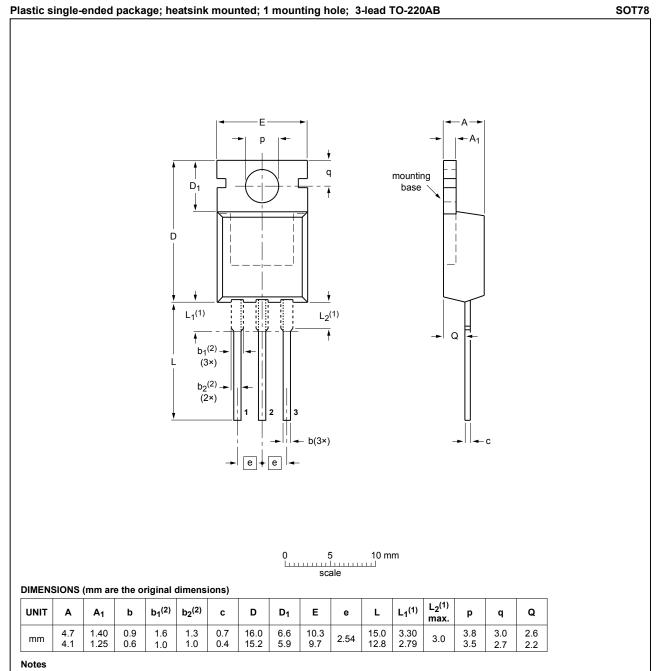


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

N-channel 40 V, 1.7 m Ω logic level MOSFET in SOT78



11. Package outline



- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE		REFERENCES			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	1330E DATE
SOT78		3-lead TO-220AB	SC-46			08-04-23 08-06-13

Fig. 17. Package outline TO-220AB (SOT78)

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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- Please consult the most recently issued document before initiating or completing a design.
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N-channel 40 V, 1.7 m Ω logic level MOSFET in SOT78

13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12

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13 / 13

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