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Real-time Clock Module (I^{2}C Bus)

Features

- ¿ Using external 32.768kHz quartz crystal for PT7C4337
- ¿ Supports I^{2}C-Bus's high speed mode (400 kHz)
- ¿ Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- ¿ Programmable square wave output signal
- ¿ Two Time-of-Day Alarms
- ¿ Oscillator Stop Flag
- ¿ Operating range: 1.8V to 5.5V
- ¿ Timekeeping range: 1.2V to 1.8V

Description

The PT7C4337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output.

Address and data are transferred serially via a 2-wire, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The device is fully accessible through the serial interface while VCC is between 1.8V and 5.5V. I^{2}C operation is not guaranteed below 1.8V. Timekeeping operation is maintained with VCC as low as 1.2V.

Table 1 shows the basic functions of PT7C4337. More details are shown in section: overview of functions.

Table 1. Basic functions of PT7C4337

Item	Function			PT7C4337
1	Oscillator	Source	Crystal(32.768KHz)	External crystal
		Oscillator enable/disable		ı
		Oscillator fail detect		ı
2	Time	Time display	12-hour	ı
			24-hour	ı
		Century bit		-
		Time count chain enable/disable		ı
3	Interrupt	Alarm interrupt output		ı 2
4	Programmable square wave output (Hz)			1, 4.096k, 8.192k, 32.768k
5	Communication	2-wire I^{2}C bus		ı

Pin Assignment

PT7C4337

1	X1		VCC	8
2	X2	SQW/INTB		7
3	INTA	SCL		6
4	GND	SDA		5
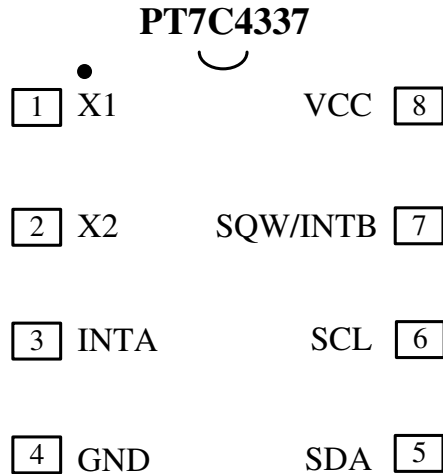
Pin Description

Pin No.	Pin	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X1, 32.768kHz crystal is connected between them. Or external clock input.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them. When 32.768kHz external input, X2 must be float.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^{2}C serial interface.
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
3	INTA	O	**Interrupt Output.** When enabled, INTA is asserted low when the time matches the values set in the alarm registers. This pin is an open-drain output and requires an external pull up resistor.
7	SQW/INTB	O	**Square-Wave/Interrupt Output.** Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pull up resistor.
8	VCC	P	**Power.** Primary power for PT7C4337.
4	GND	P	**Ground.**
/	NC		**No Connect.** These pins are not connected internally, but must be grounded for proper operation.

Maximum Ratings

Storage Temperature .... -65

Operating Mode

The amount of current consumed by the PT7C4337 is determined, in part, by the I^{2}C interface and oscillator operation. The following table shows the relationship between the operating mode and the corresponding I$_{CC}$ parameter.

Operating Mode	V$_{CC}$	Power
I^{2}C Interface Active	1.8V ≤ V$_{CC}$ ≤ 5.5V	I$_{CC}$ Active (I$_{CCA}$)
I^{2}C Interface Inactive	1.8V ≤ V$_{CC}$ ≤ 5.5V	I$_{CC}$ Standby (I$_{CCS}$)
I^{2}C Interface Inactive	1.2V ≤ V$_{CC}$ ≤ 1.8V	Timekeeping (I$_{CCTOSC}$)
I^{2}C Interface Inactive, Oscillator Disabled	1.2V ≤ V$_{CC}$ ≤ 1.8V	Data Retention (I$_{CCTDDR}$)

Recommended Operating Conditions

Part No.	Sym.	Description		Min	Type	Max	Unit
PT7C4337	V$_{CC}$	V$_{CC}$ supply voltage		1.8	3.3	5.5	V
	V$_{CCT}$			1.2	-	1.8	
	V$_{OSC}$	Oscillator start up voltage		1.2	-	5.5	
	V$_{IH}$	Input high level	SCL, SDA	0.7V$_{CC}$	-	V$_{CC}$+0.3	
			$\overline{INTA}$, SQW/$\overline{INTB}$	-	-	5.5	
	V$_{IL}$	Input low level		-0.3	-	0.3V$_{CC}$	
	T$_A$	Operating temperature		-40	-	85	ºC

DC Electrical Characteristics

Unless otherwise specified, V$_{CC}$ = 1.8~5.5V, T$_A$ = -40 °C to +85 °C

Sym.	Item	Pin	Condition	Min	Typ	Max	Unit
V$_{CC}$	Supply voltage	V$_{CC}$	Full operation	1.8	-	5.5	V
V$_{CCT}$			Timekeeping (Note 5)	1.2	-	1.8	
V$_{OSC}$	Oscillator voltage	V$_{CC}$		1.2	-	5.5	V
V$_{IL1}$	Low-level input voltage	SCL		-0.3	-	0.3V$_{CC}$	V
V$_{IH1}$	High-level input voltage	SCL		0.7V$_{CC}$	-	V$_{CC}$+0.3	
V$_{IL2}$	Low-level input voltage	X1		-	0.53	-	V
V$_{IH2}$	High-level input voltage	X1		-	0.53	-	
I$_{OL}$	Low-level output current	SDA, /INTA, /INTB	V$_{OL}$ = 0.4V	3	-	-	mA
I$_{IL}$	Input leakage current	SCL		-1	-	1	mA
I$_{OZ}$	Output current when OFF	SDA, /INTA, /INTB		-1	-	1	mA

DC Electrical Characteristics

Sym.	Item	Pin	Condition	Min	Typ	Max	Unit
Unless otherwise specified, V$_{CC}$ = 1.3~1.8V, T$_A$ = -40 °C to +85 °C							
I$_{CCTOSC}$	Timekeeping current	V$_{CC}$	Note 2, 4, 5	-	450	800	nA
I$_{CCTDDR}$	Data retention current	V$_{CC}$	Note 2,4,5,6	-	-	160	
Unless otherwise specified, V$_{CC}$ = 1.8~3.6V, T$_A$ = -40 °C to +85 °C							
I$_{CCA}$	Active supply current	V$_{CC}$	Note 1, 5	-	-	100	mA

Recommended Layout for Crystal

Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.
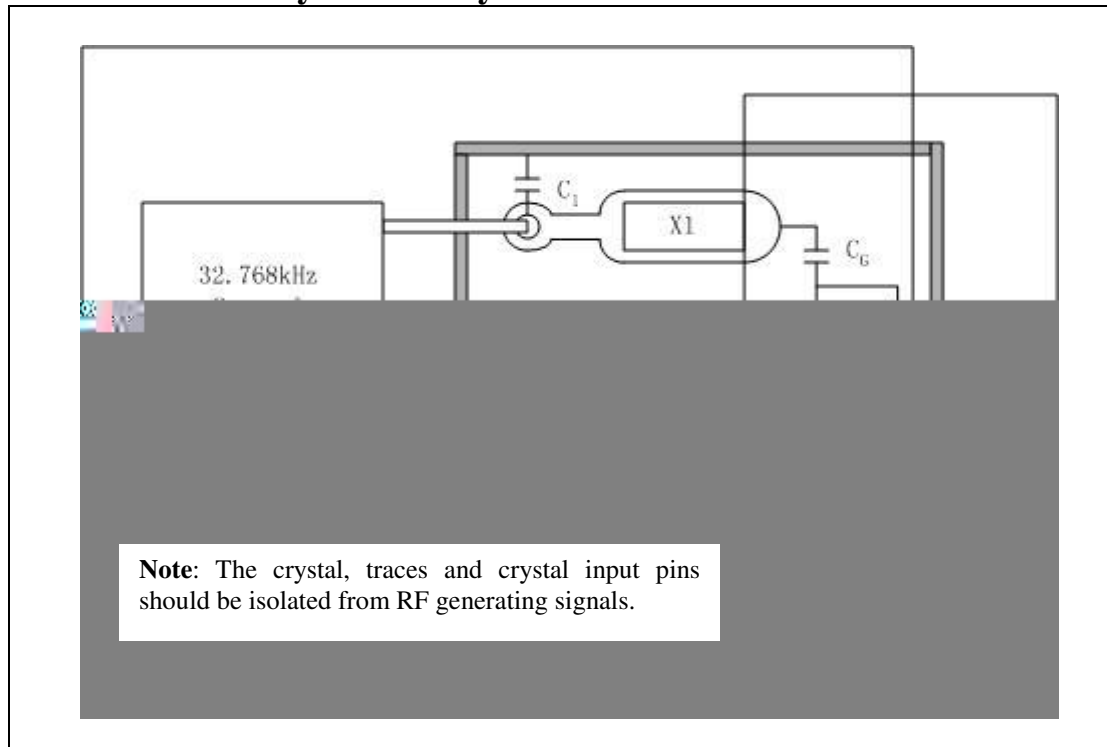
Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	X1 to GND	C_G	12	pF
	X2 to GND	C_D	12	pF
Recommended External capacitors for crystal C_L=12.5pF	X1 to GND	C_1	13	pF
	X2 to GND	C_2	13	pF
Recommended External capacitors for crystal C_L=6pF	X1 to GND	C_1	0	pF
	X2 to GND	C_2	0	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768KHz, C_1 and C_2 should meet the equation as below:

$$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] =C_L$$

Cpar is all parasitical capacitor between X1 and X2.

C_L is crystal's load capacitance.

Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kW
Load Capacitance	C_L	-	6/12.5	-	pF

AC Electrical Characteristics

Sym	Description	Value	Unit
V$_{HM}$	Rising and falling threshold voltage high	0.8 V$_{CC}$	V
V$_{HL}$	Rising and falling threshold voltage low	0.2 V$_{CC}$	V

Over the operating range

Symbol	Item	Min.	Typ.	Max.	Unit
f$_{SCL}$	SCL clock frequency	-	-	400	kHz
t$_{SU;STA}$	START condition set-up time	0.6	-	-	ms
t$_{HD;STA}$	START condition hold time	0.6	-	-	ms
t$_{SU;DAT}$	Data set-up time (RTC read/write)	200	-	-	ns
t$_{HD;DAT1}$	Data hold time (RTC write)	35	-	-	ns
t$_{HD;DAT2}$	Data hold time (RTC read)	0	-	-	ms
t$_{SU;STO}$	STOP condition setup time	0.6	-	-	ms

t$_{BUF}$

Function Block

Oscillator Circuit
PT7C4337

The PT7C4337 uses an external 32.768 kHz crystal. Table2 specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table2 Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit

Function Description
Overview of Functions
Clock function
CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

Alarm function
This device has two alarm system (Alarm 1 and Alarm 2) that outputs interrupt signals from INTA or INTB to CPU when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm is be selectable between on and off for matching alarm or repeating alarm.

Programmable square wave output
A square wave output enable bit controls square wave output at pin 7. Frequencies are selectable: 1, 4.096k, 8.192k, 32.768k Hz.

Interface with CPU
Data is read and written via the I^{2}C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz, which supports the I^{2}C bus's high-speed mode.

Oscillator fail detect
When oscillator fail, PT7C4337 OSF bit will be set.

Oscillator enable/disable
Oscillator and time count chain can be enabled or disabled at the same time by /ETIME bit.

Registers
Allocation of registers

Addr. (hex)[1]	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	0	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
03	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01-12)	Century	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Alarm 1: Seconds	A1M1[2]	S40	S20	S10	S8	S4	S2	S1

08	Alarm 1: Minutes	A1M2[*2]	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3[*2]	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4[*2]	Day, /Date	0, D20	0, D10	0,			

Square wave frequency selection bits

¿ **RS2, RS1**

Square wave Rate Select. These bits control the frequency of the square-wave output when the square wave has been enabled.

RS2, RS1	Data	SQW output freq. (Hz)
Read / Write	00	1
	01	4.096k
	10	8.192k
	11	32.768k ^{Default}

Interrupt related bits

¿ **INTCN**

Interrupt Output pin select bit. This bit controls the relationship between the two alarms and the interrupt output pins.

INTCN	Data	Description
Read / Write	1	A match between the timekeeping registers and the alarm 1 registers activates the $\overline{\text{INTA}}$ pin (if the alarm 1 is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/$\overline{\text{INTB}}$ pin (if the alarm 2 is enabled).
	0	A match between the timekeeping registers and either alarm 1 or alarm 2 registers activates the $\overline{\text{INTA}}$ pin (if the alarms are enabled). In this configuration, a square wave is output on the SQW/$\overline{\text{INTB}}$ pin. ^{Default}

¿ **A1IE**

Alarm 1 Interrupt Enable.

A1IE	Data	Description
Read / Write	0	The A1F bit does not initiate the $\overline{\text{INTA}}$ signal. ^{Default}
	1	Permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{\text{INTA}}$.

¿ **A1F**

Alarm 1 Flag.

A1F	Data	Description
Read / Write	0	The time do not match the alarm 1 registers. ^{Default}
Read	1	Indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the $\overline{\text{INTA}}$ pin goes low. A1F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

¿ **A2IE**

Alarm 2 Interrupt Enable.

A2IE	Data	Description
Read / Write	0	The A2F bit does not initiate an interrupt signal. ^{Default}
	1	Permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{\text{INTA}}$ (when INTCN = 0) or to assert SQW/$\overline{\text{INTB}}$ (when INTCN = 1).

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12, /24	Description	Hours register
0	24-hour time display	
1	12-hour time display	

* Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

Days of the week Counter

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Days of the week	0	0	0	0	0	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

Calendar Counter

The data format is BCD format.
¿   Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
          Range from 1 to 30 (for April, June, September and November).
          Range from 1 to 29 (for February in leap years).
          Range from 1 to 28 (for February in ordinary years).
          Carried to month digits when cycled to 1.
¿   Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
¿   Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
04	Dates	0	0	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
05	Months	Century[1]	0	0	M10	M8	M4	M2	M1
	(default)	Undefined	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

*1:

Alarm Register

¿   **Alarm 1, Alarm 2 Register**

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Alarm 1: Seconds	A1M1[*1]	S40	S20	S10	S8	S4	S2	S1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
08	Alarm 1: Minutes	A1M2[*1]	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
09	Alarm 1: Hours	A1M3[*1]	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0A	Alarm 1: Day, Date	A1M4[*1]	Day, /Date[*1]	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0B	Alarm 2: Minutes	A2M2[*2]	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0C	Alarm 2: Hours	A2M3[*2]	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0D	Alarm 2: Day, Date	A2M4[*2]	Day, /Date[*2]	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

*1 Note: Alarm mask bit, using to select Alarm 1 alarm rate.

*2 Note: Alarm mask bit, using to select Alarm 2 alarm rate.

Alarm Function

Related register

Addr. (hex)	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1

Table 1. Alarm 1 Mask Bits

Day, /Date	Alarm 1 register mask bits				Alarm rate
	A1M4	A1M3	A1M2	A1M1	
¼	1	1	1	1	Alarm once per second
¼	1	1	1	0	Alarm when seconds match
¼	1	1	0	0	Alarm when minutes and seconds match
¼	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match
Others					Ignored.

Table 2. Alarm 2 Mask Bits

| Day, /Date	Alarm 2 register mask bits			Alarm rate
	A2M4	A2M3	A2M2	
¼	1	1	1	Alarm once per minute (00 seconds of every minute)
¼	1	1	0	Alarm when minutes match
¼	1	0	0	Alarm when hours, minutes
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match
Others				Ignored.

I^{2}C Bus Interface

Overview of I^{2}C-BUS

The I^{2}C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I^{2}C bus device does not include a chip select pin such as i

Starting and Stopping I²C Bus Communications

Fig 2. Starting and stopping on I²C bus
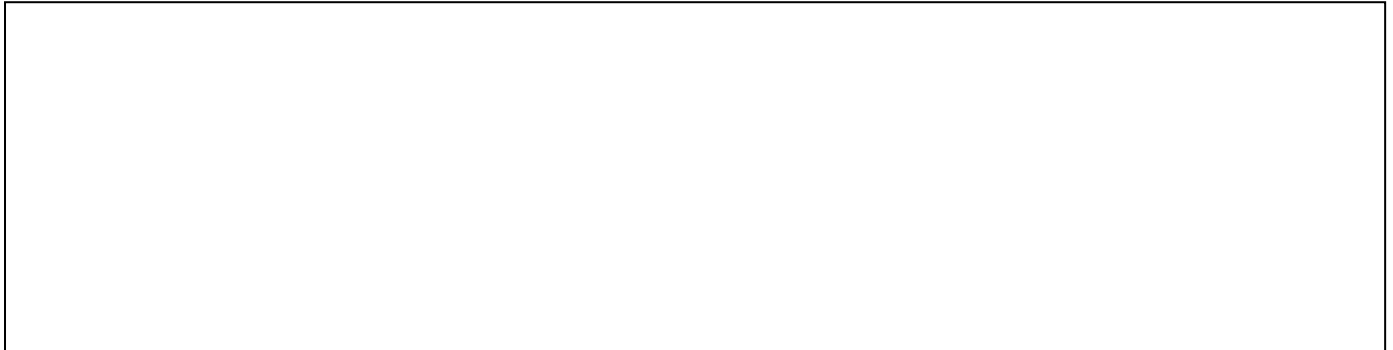
1) **START condition, repeated START condition, and STOP condition**
   a) START condition
      SDA level changes from high to low while SCL is at high level
   b) STOP condition
      SDA level changes from low to high while SCL is at high level
   c) Repeated START condition (RESTART condition)
      In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.
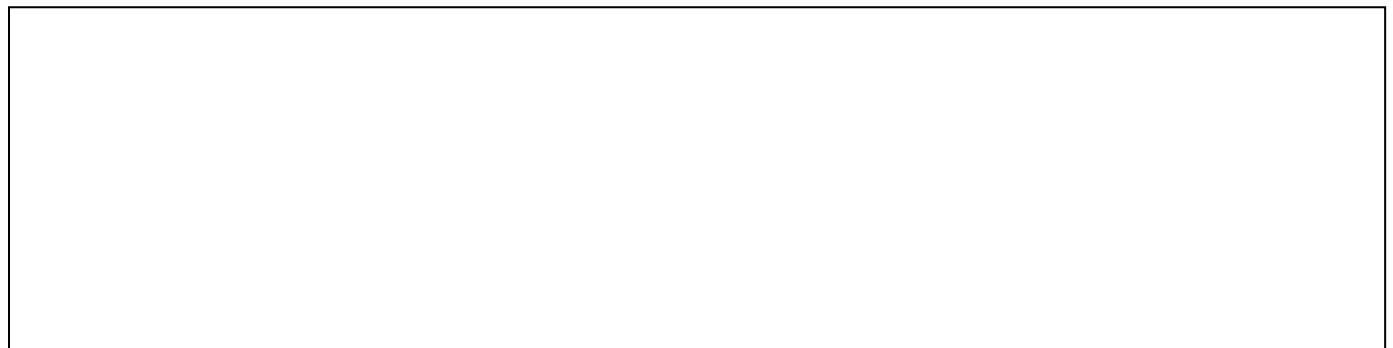
2) **Data Transfers and Acknowledge Responses during I²C-BUS Communication**

a) **Data transfers**
Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.

*Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

b) **Data acknowledge response (ACK signal)**
When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.

After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

Slave Address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.
Slave addresses have a fixed length of 7 bits. See table for the details.
An R/W bit is added to each 7-bit slave address during 8-bit transfers.

Table

Operation	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	D1 h	1	1	0	1	0	0	0	1 (= Read)
Write	D0 h								0 (= Write)

I²C Bus˘s Basic Transfer Format

1) Write via I^{2}C bus

2) Read via I^{2}C bus

    a)   Standard read

    b)   Simplified read

Note:
1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
2. 49H, 4AH are used as test mode address. Customer should not use the addresses.

Mechanical Information

WE (Lead free and Green SOIC-8)

UE(Lead free and Green MSOP-8)

LE (Lead free and Green 8-Pin TSSOP)

ZEE (Lead free and Green 8-Pin TDFN)

Ordering Information

Part Number	Package Code	Package
PT7C4337WE	W	Lead free and Green 8-Pin SOIC
PT7C4337UE	U	Lead free and Green 8-Pin MSOP
PT7C4337ZEE	ZE	Lead free and Green 8-Pin TDFN
PT7C4337LE	L	Lead free and Green 8-Pin TSSOP

Notes: