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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Real-time Clock Module (I^2C Bus)

Product Features

- ¿ Using external 32.768kHz quartz crystal
- ¿ Supports I^2C-Bus's high speed mode (400 kHz)
- ¿ Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- ¿ Programmable square wave output signal
- ¿ 56-byte, battery-backed, nonvolatile (NV) RAM for data storage
- ¿ Automatic power-fail detect and switch circuitry of battery backup
- ¿ UL Recognized: E348121

Product Description

The PT7C4338 serial real-time clock is a low-power clock/calendar with a programmable square-wave output and 56 bytes of nonvolatile RAM.

Address and data are transferred serially via a 2-wire, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

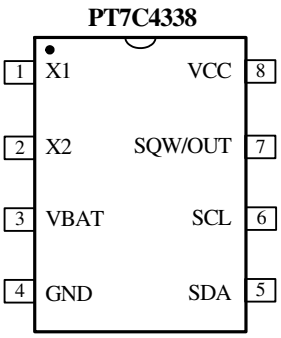
The PT7C4338 series have a built-in power sense circuit that detects power failures and automatically switches to the battery supply.

Table 1 shows the basic functions of PT7C4338. More details are shown in section: overview of functions.

Table 1. Basic functions of PT7C4338

Item	Function			PT7C4338
1	Oscillator	Source: Crystal: 32.768kHz		ı
		Oscillator enable/disable		ı
		Oscillator fail detect		ı
2	Time	Time display	12-hour	ı
			24-hour	ı
		Century bit		-
3	Alarm interrupt			-
4	Programmable square wave output (Hz)			1, 4.096k, 8.192k, 32.768k
5	RAM			56×8
6	Battery backup			ı

Pin Assignment

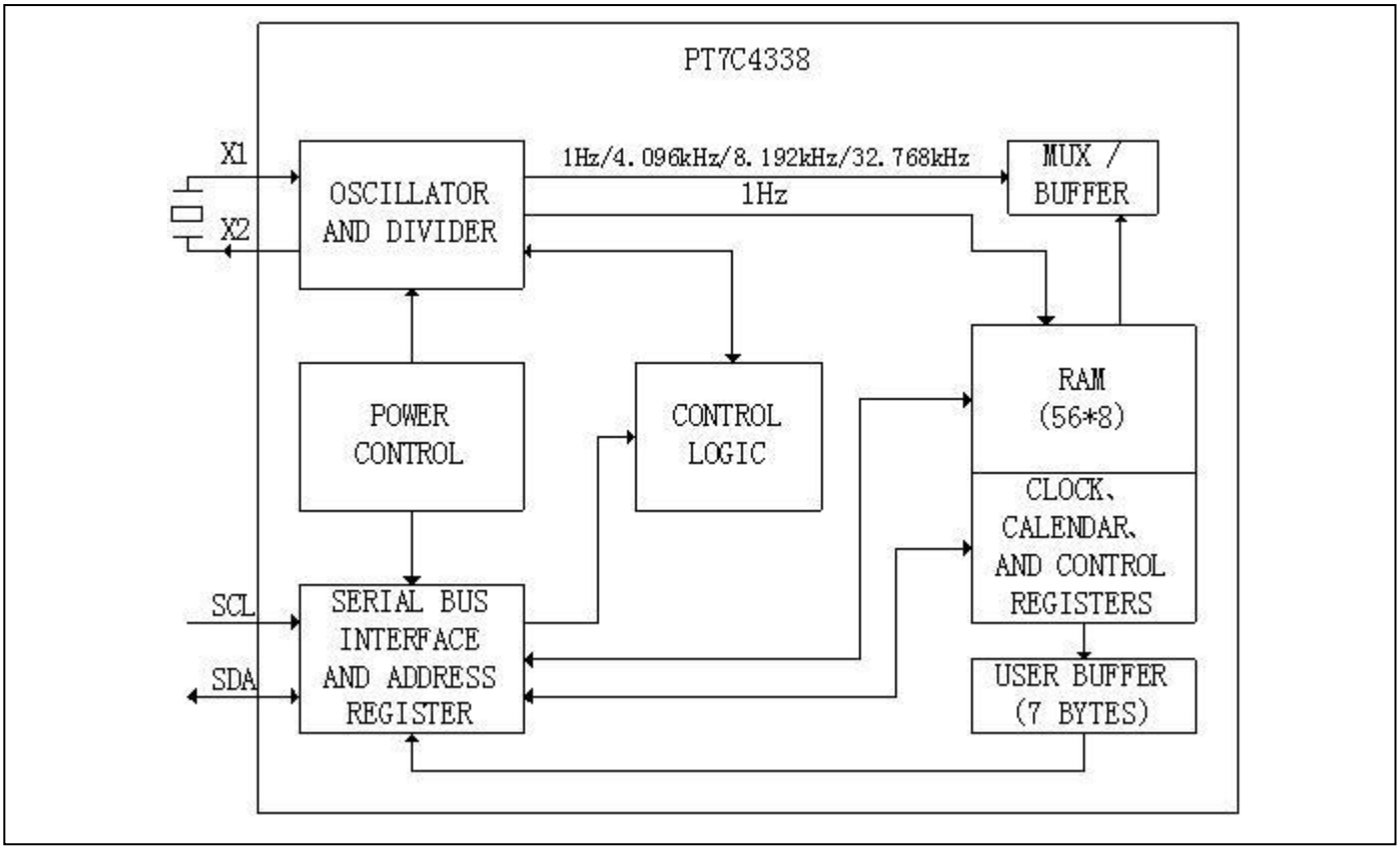


SOIC-8
MSOP-8

Pin Description

Pin no.	Pin	Type	Description
1	X1	I	**32.768kHz Crystal Connections.** The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5pF. Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1. An external 32.768kHz oscillator can also drive the PT7C4338. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
2	X2	O	
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
7	SQW/OUT	O	**Square-Wave/Output Driver.** When enabled and the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). It is open drain and requires an external pull up resistor. Operates with either VCC or VBAT applied.
8	VCC	P	**Supply Voltage.** When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and VCC is below VPF, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.
3	VBAT	P	**+3V Battery Input.** Backup supply input for any standard 3V lithium cell or other energy source. Battery voltage must be held between the minimum and maximum limits for proper operation. If a backup supply is not required, VBAT must be grounded. **UL** recognized to ensure against reverse charging when used with a lithium battery.
4	GND	P	**Ground.** DC power is provided to the device on these pins. VCC is the primary power input. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and VCC is below VPF, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

Function Block



Maximum Ratings

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND)	-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	-0.3V to +6.5V
DC Output Voltage (SDA, /INTA, /INTB pins)	-0.3V to +6.5V
DC Output Current (FOUT)	-0.3V to (V_{cc}+0.3V)
Power Dissipation	320mW (depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40℃ to +85℃.) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	PT7C433833	2.7	3.3	5.5	V
Logic 1	V_{IH}	Note 2	0.7 * V_{CC}	-	V_{CC} + 0.3	
Logic 0	V_{IL}	Note 2	-0.3	-	+0.3 * V_{CC}	
Power-Fail Voltage	V_{PF}	PT7C433833	-	2.59	-	
V_{BAT} Battery Voltage	V_{BAT}	Note 2	1.5	3.0	3.7	

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.

DC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40℃ to +85℃.) (Note 1)

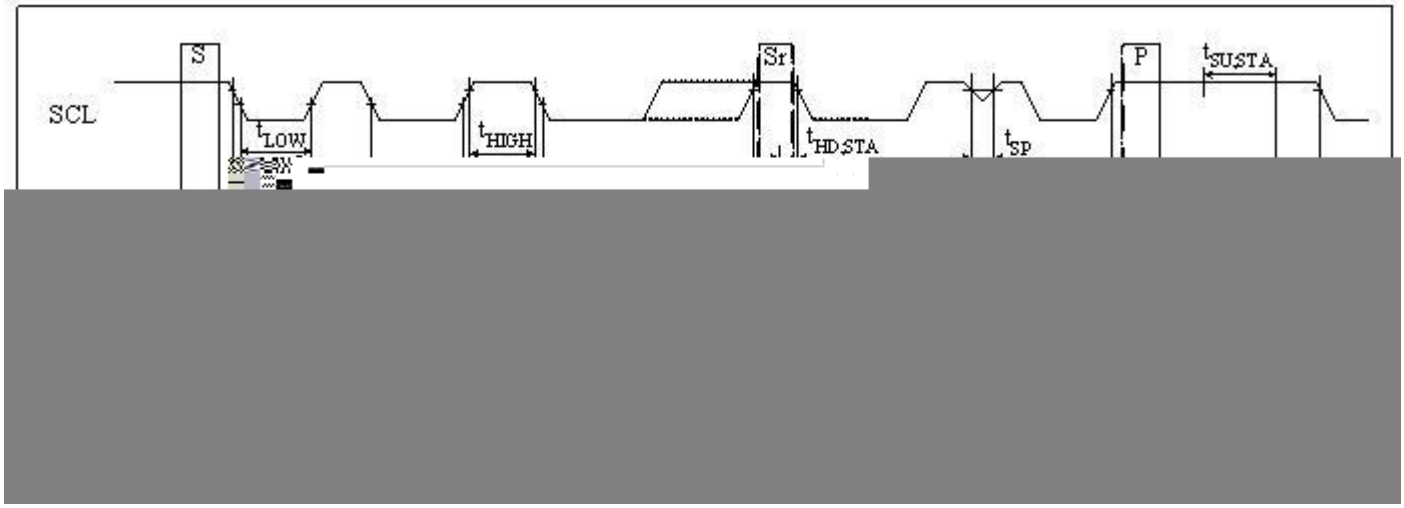
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{BAT} Battery Voltage	V_{BAT}	Note 2	1.5	-	3.7	V
Input Leakage	I_{LI}	Note 3	-	-	1	µA
I/O Leakage	I_{LO}	Note 4	-	-	1	µA
SDA Logic 0 Output	I_{OLSDA}	V_{CC} > 2V; V_{OL} = 0.4V	3.0	-	-	mA
		V_{CC} < 2V; V_{OL} = 0.2 V_{CC}	3.0	-	-	
SQW/OUT Logic 0 Output	I_{OLSQW}	V_{CC} > 2V; V_{OL} = 0.4V	3.0	-	-	mA
		1.71V < V_{CC} < 2V; V_{OL} = 0.2 V_{CC}	3.0	-	-	
		1.5V < V_{CC} < 1.71V; V_{OL} = 0.2 V_{CC}	250	-	-	µA
Active Supply Current (Note 5)	I_{CCA}	PT7C433833	-	120	200	µA
Standby Current (Note 6)	I_{CCS}	PT7C433833	-	85	125	µA

(T_A = -40℃ to +85℃) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL Clock Frequency	f_{SCL}	Fast mode	100	-	400	kHz
		Standard mode	-	-	100	
Bus Free Time Between STOP and START condition	t_{BUF}	Fast mode	1.3	-	-	µs
		Standard mode	4.7	-	-	
Hold Time (Repeated) START Condition (Note 2)	$t_{HD:STA}$	Fast mode	0.6	-	-	µs
		Standard mode	4.0	-	-	
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3	-	-	µs
		Standard mode	4.7	-	-	
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6	-	-	µs
		Standard mode	4.0	-	-	
Setup Time of Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6	-	-	µs
		Standard mode	4.7	-	-	
Data Hold Time (Note 3, 4)	$t_{HD:STA}$	Fast mode	0	-	0.9	µs
		Standard mode	0	-	-	
Data Setup Time (Note 5)	$t_{SU:STA}$	Fast mode	100	-	-	ns
		Standard mode	250	-	-	
Rise Time of Both SDA and SCL Signals (Note 6)	t_r	Fast mode	$20+0.1C_B$	-	300	ns
		Standard mode	$20+0.1C_B$	-	1000	
Fall Time of Both SDA and SCL Signals (Note 6)	t_f	Fast mode	$20+0.1C_B$	-	300	ns
		Standard mode	$20+0.1C_B$	-	300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6	-	-	µs
		Standard mode	4.0	-	-	
Capacitance Load for Each Bus Line	C_B	Note 6	-	-	400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	Note 1	-	-	10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}	Note 7	-	100	-	ms

Note 1: Limits of full temperature are guaranteed by design not production test.
Note 2:

Timing Diagram



Power-Up/Power-Down Characteristics

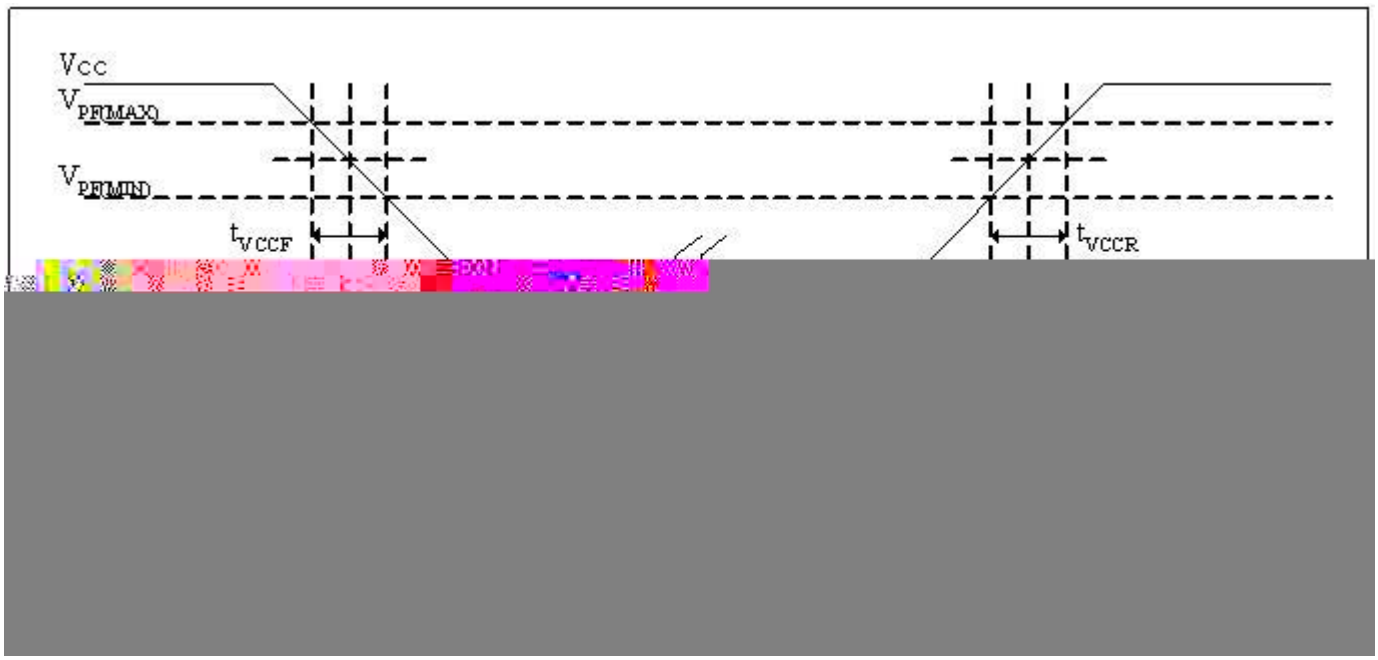
(T_A = -40℃ to +85℃) (Note 1, Fig 3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Recovery at Power-Up (Note 2)	t_{REC}	-	-	2	ms
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}	300	-	-	µs
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}	0	-	-	µs

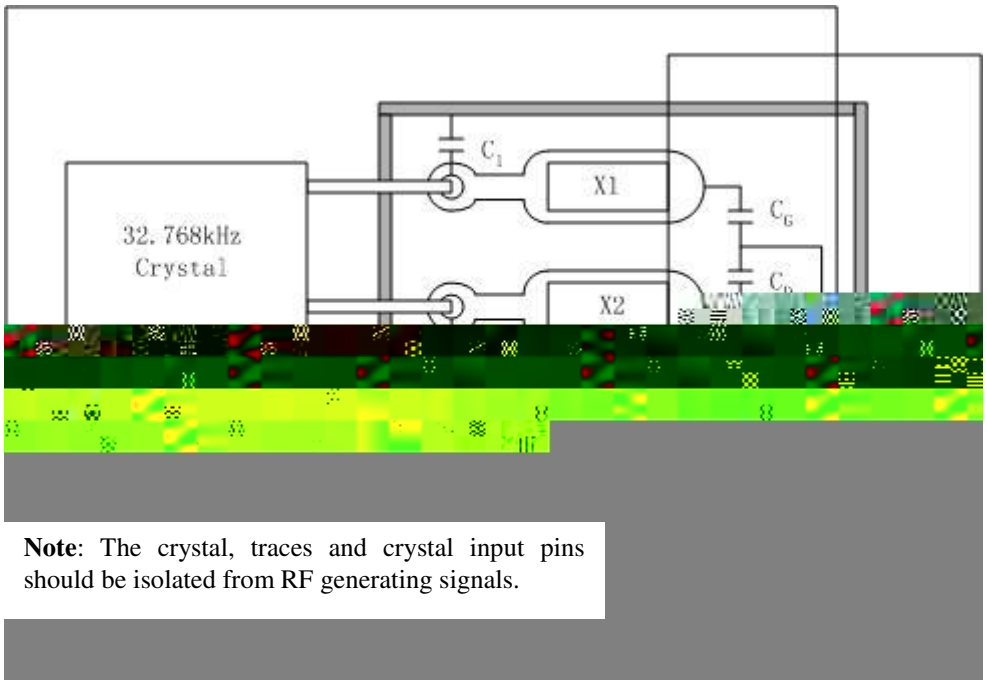
Note 1: Limits at -40°C are guaranteed by design and not production tested.

Note 2: This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

Fig 3. Power-Up/Power-Down Timing



Recommended Layout for Crystal



Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	X1 to GND	C_G	20	pF
	X2 to GND	C_D	20	pF
Recommended External capacitors	X1 to GND	C_1	4	pF
	X2 to GND	C_2	4	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768KHz, C_1 and C_2 should meet the equation as below:

$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$

Cpar is all parasitical capacitor between X1 and X2.

C_L is crystal's load capacitance.

Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kW
Load Capacitance	C_L	-	12.5	-	pF

Function Description

Overview of Functions

Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. 4 frequencies are selectable: 1, 4.096k, 8.192k, 32.768k Hz.

Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

Oscillator enable/disable

Oscillator can be enabled or disabled by /EOSC bit.

Registers

Allocation of registers

Addr. (hex)[*1]	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	/EOSC[*2]	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	0	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
03	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01-12)	0	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

Control and status register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Control	OUT	0	OSF	SQWE	0	0	RS1	RS0
	(default)	1	0	1	1	0	0	1	1

¿ **OUT**

It controls the output level of the SQW/OUT pin when the square wave output is disabled.

OUT	Data	Description
Read / Write	0	When SQWE = 0, SQW/OUT pin output low.
	1	When SQWE = 0, SQW/OUT pin output high. Default

¿ **SQWE (Square Wave Enable)**

This bit, when set to logic 1, will enable the oscillator output. The frequency of the square wave output depends upon the value of the RS0 and RS1 bits. With the square wave output set to 1Hz, the clock registers update on the falling edge of the square wave.

¿ **RS (Rate Select)**

These bits control the frequency of the square wave output when the square wave output has been enabled.

RS1, RS0	Data	SQW output freq. (Hz)
Read / Write	00	1
	01	4.096k
	10	8.192k
	11	32.768k Default

¿ **OSF(Oscillator Stop Flag)**

Logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on VCC and VBAT is insufficient to support oscillation.
3) The /EOSC bit is set to 1, disabling the oscillator.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF bit to logic 1 leaves the value unchanged.