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Real-time Clock Module

Features

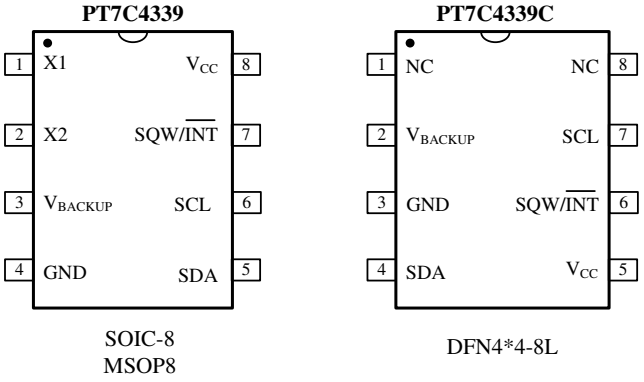
- Real-Time Clock (RTC) Including Time (Seconds, Minutes and Hours) and Calendar (Day, Date, Month and Year with Leap-Year Compensation Valid Up to 2100) counter functions (BCD code)
- Available in a Surface-Mount Package with an Integrated Crystal (Only for PT7C4339C)
- I^2C Serial Interface supports I^2C-Bus's high speed mode (400 kHz)
- Programmable square wave output signal, defaults to 32 kHz on Power-up
- Two Time-of-Day Alarms
- Oscillator Stop Flag
- Automatic Power-Fail Detect and Switch Circuitry
- Temperature Range: -40°C to +85°C
- Package: MSOP-8L and SOIC-8L for PT7C4339
  TDFN4x4-8L for PT7C4339C

Applications

Description

The PT7C4339 real-time clock is a low-power clock/calendar device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I^2C bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The PT7C4339 has a build-in power-sense circuit that detects power failures and automatically switch to the backup supply, maintaining time, date, and alarm operation.

Pin Configuration



SOIC-8
MSOP8

DFN4*4-8L

Table1. Diverse functions of RTC circuits

Item	Function			PT7C4339	PT7C4339C
1	Oscillator	Source	External crystal	External crystal	Integrated Crystal
		Oscillator enable/disable		√	√
		Oscillator fail detect		√	√
2	Time	Time display	12-hour	√	√
			24-hour	√	√
		Century bit		√	√
		Time count chain enable/disable		√	√
3	Interrupt	Alarm interrupt output		√ 2	√ 2
4	Programmable square wave output (Hz)			1, 4.096k, 8.192k, 32.768k	1, 4.096k, 8.192k, 32.768k
5	Communication	2-wire I^2C bus		√	√
6	Power failure detect			√	√

Pin Description

Pin No		Pin Name	Type	Description
4339	4339C			
1	/	X1	I	**Oscillator Circuit Input.** Together with X1, 32.768kHz crystal is connected between them. Or external clock input.
2	/	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them. When 32.768kHz external input, X2 must be float.
6	7	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface. The pull up voltage may be up to 5.5V regardless of the voltage on V_{CC}.
5	4	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor. The pull up voltage may be up to 5.5V regardless of the voltage on V_{CC}.
3	2	V_{BACKUP}	O	**Secondary Power Supply.** Supply voltage must be held between 1.3V and 3.7V for proper operation. This pin can be connected to a primary cell, such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used in conjunction with the trickle-charge feature. Diodes should not be placed in series between the backup source and the V_{BACKUP} input, or improper operation will result. If a backup supply is not required, V_{BACKUP} must be grounded.
7	6	SQW /INT	O	**Square-Wave/Interrupt Output.** Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pull up resistor. The pull up voltage may be up to 5.5V regardless of the voltage on V_{CC}. If not used, this pin may be left unconnected.
8	5	V_{CC}	P	**Power.** When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected and V_{CC} is below V_{PF}, reads and writes are inhibited. The timekeeping and alarm functions operate when the device is powered by V_{CC} or V_{BACKUP}.
4	3	GND	P	**Ground.**
/	1,8	NC		**No Connect.** These pins are not connected internally, but must be grounded for proper operation.

Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Ambient Temperature with Power Applied..... -40°C to +85°C
Supply Voltage to Ground Potential (V_{CC} to GND) ..... -0.3V to +6.0V
DC Input (All Other Imputs except V_{CC} & GND) ..... -0.3V to V_{CC} +0.3V
DC Output Voltage (SDA, SQW /INT pins) ..... -0.3V to +6.0V
Power Dissipation ..... 320mW(depend on package)
Lead Temperature (soldering, 10s)..... +260 °C
Soldering Temperature (reflow)..... +260 °C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Min	Type	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	5.5	V
V_{BACKUP}	Backup Supply Voltage	1.3	3.0	3.7	V
V_{IH}	Input high level	$0.7V_{CC}$	-	V_{CC}+0.3	V
V_{IL}	Input low level	-0.3	-	$0.3V_{CC}$	V
V_{PF}	Power-Fail Voltage	1.60	1.72	1.88	V
T_A	Operation Temperature	-40	-	85	ºC

DC Electrical Characteristics

Unless otherwise specified, V_{CC} = MIN to MAX, V_{BACKUP}=MIN to MAX, T_A = -40 °C to +85 °C

Item	Sym.	Pin	Condition	Min	Typ	Max	Units
Input Leakage	I_{LI}	SCL	$V_{IN}=V_{CC}$ or GND	-1		1	µA
I/O Leakage	I_{LO}	SDA, SQW/INT		-1		1	µA
Logic0 Out V_{OL}= 0.4V; V_{CC}> V_{CCMIN}	I_{OL1}	SQW/INT		1.0	3.0	-	mA
	I_{OL2}	SDA,		1.5	3.0	-	mA
Logic 0 Out V_{OL}= 0.2V; V_{BACKUP} >= $V_{BACKMIN}$	I_{OL1}	SQW/INT	V_{CC} absent, BBSQI=1		0.25	-	mA
V_{CC} Active Current	I_{CCA}		(Note 1)		80	250	µA
V_{CC} Standby Current(Note 2)	I_{CCS}	V_{CC} = 3.3V			40	100	µA
		V_{CC} = 5.5V				150	
Trickle-Charger Resistor Register10h = A5h, V_{CC} = Typ, V_{BACKUP}= 0V	R1		(Note 3)		200		Ω
Trickle-Charger Resistor Register10h = A6h, V_{CC} = Typ, V_{BACKUP} = 0V	R2				2000		Ω
Trickle-Charger Resistor Register10h = A7h, V_{CC} = Typ, V_{BACKUP} = 0V	R3				4000		Ω
V_{BACKUP} Leakage Current	I_{BKLKG}	V_{BACKUP}			25	100	nA

DC Electrical Characteristics

Unless otherwise specified, V_{CC} = 0V, V_{BACKUP}=MIN to MAX, T_A = -40 °C to +85 °C

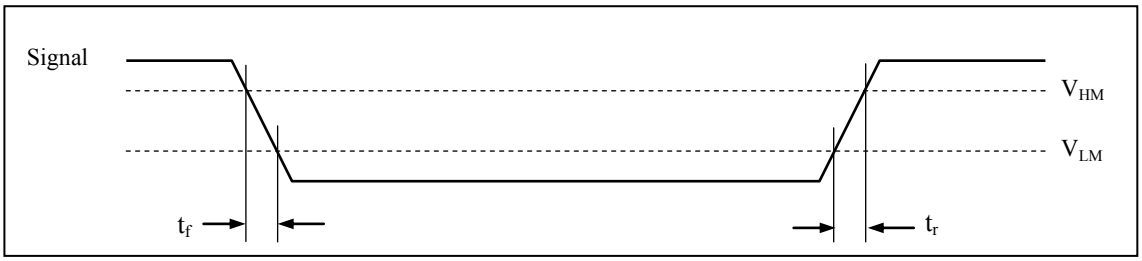
Item	Sym.	Condition	Min	Typ	Max	Units
V_{BACKUP} Current, /EOSC=0, SQW Off	I_{BKOSC}	Note 4, Note5		300	600	nA
V_{BACKUP} Current, /EOSC=0, SQW On	I_{BKSQW}	Note 4		400	900	nA
V_{BACKUP} Current, /EOSC=1	I_{BKDR}	Note6		10	100	nA

Note:

1. SCL clocking at max frequency = 400 kHz, V_{IL} = 0.0V, V_{IH} = VCC, trickle charger disabled.
2. Specified with 2-wire bus inactive, V_{IL} = 0.0V, V_{IH} = VCC, trickle charger disabled.
3. V_{CC} must be less than 3.63V if 200Ω resistance is selected.
4. Using recommended crystal on X1 and X2.
5. Specified with the SQW function disabled by setting INTCN = 1.
6. Crystal oscillator is disabled.

AC Electrical Characteristics

Sym	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.2 V_{CC}	V



Over the operating range (Figure 1)

Symbol	Item	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	-	-	400	kHz
$t_{SU;STA}$	START condition set-up time	0.6	-	-	µs
$t_{HD;STA}$	START condition hold time	0.6	-	-	µs
$t_{SU;DAT}$	Data set-up time (RTC read/write)	200	-	-	ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35	-	-	ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0	-	-	µs
$t_{SU;STO}$	STOP condition setup time	0.6	-	-	µs
t_{BUF}	Bus idle time between a START and STOP condition	1.3	-	-	µs
t_{LOW}	When SCL = "L"	1.3	-	-	µs
t_{HIGH}	When SCL = "H"	0.6	-	-	µs
t_r	Rise time for SCL and SDA	-	-	0.3	µs
t_f	Fall time for SCL and SDA	-	-	0.3	µs
t_{SP}*	Allowable spike time on bus	-	-	50	ns
C_B	Capacitance load for each bus line	-	-	400	pF
$C_{I/O}$ *	I/O Capacitance (SDA, SCL)	-	-	10	pF
T_{OSF}	Oscillator Stop Flag (OSF) Delay	-	-	100	ms

*** Note:** only reference for design

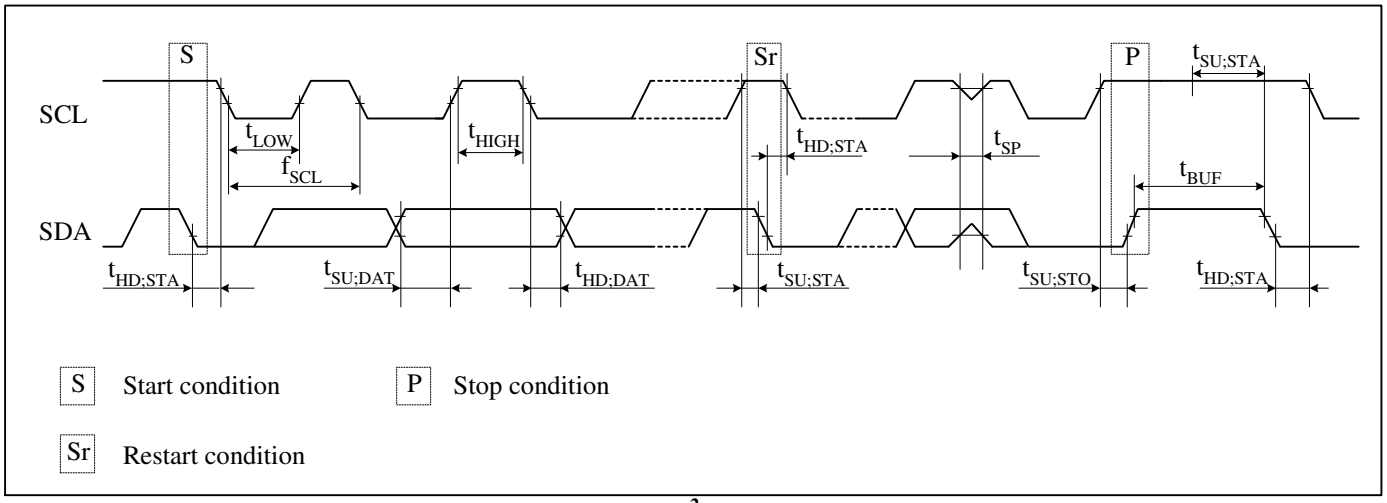
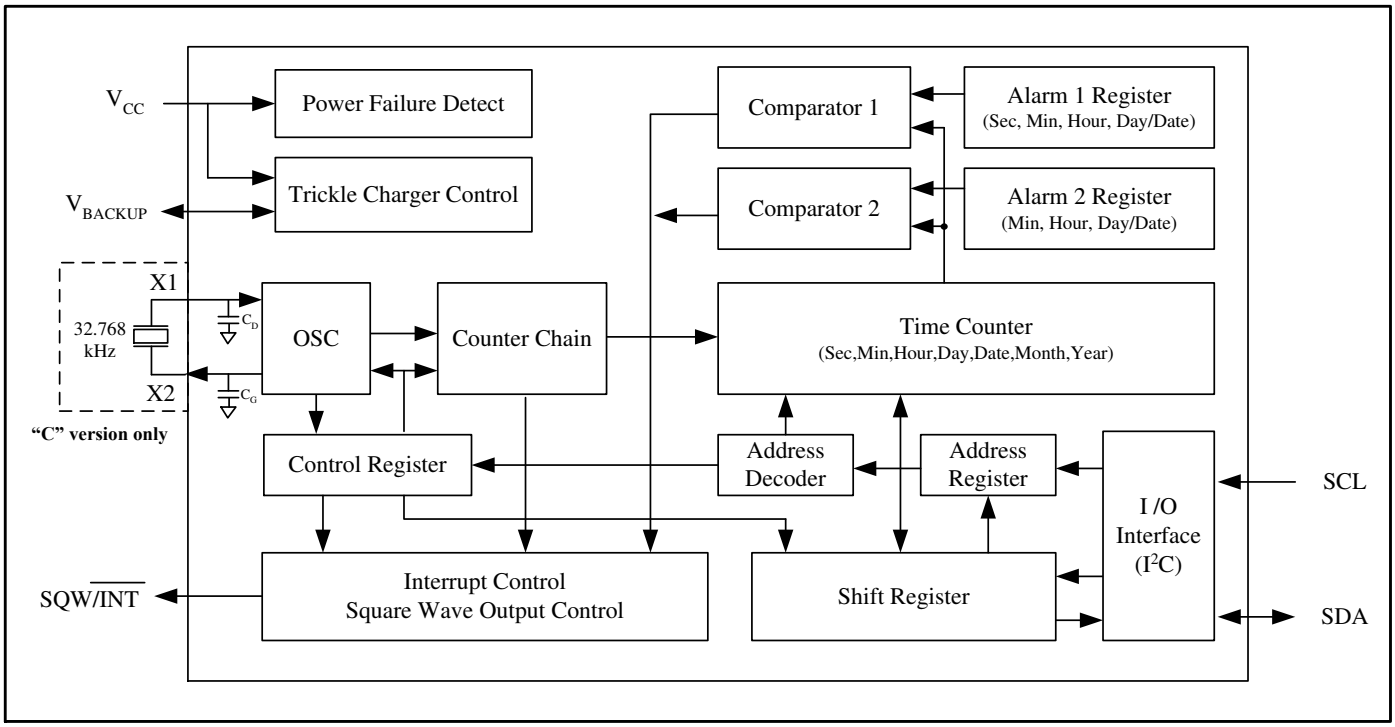


Figure1 I^2C Timing

Functional Block Diagram



Oscillator Circuit

PT7C4339

The PT7C4339 uses an external 32.768 kHz crystal. Table1 specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table1 Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_L	-	6	-	pF

Note: The crystal, traces, and crystal input pins should be isolated from RF generating signals.

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 2 shows a typical PC board layout for isolating the crystal and oscillator from noise.

PT7C4339C

The PT7C4339C integrates a standard 32,768Hz crystal in the package. Typical accuracy at nominal VCC and +25°C is approximately ±10ppm.

Recommended Layout for Crystal (only for PT7C4339)

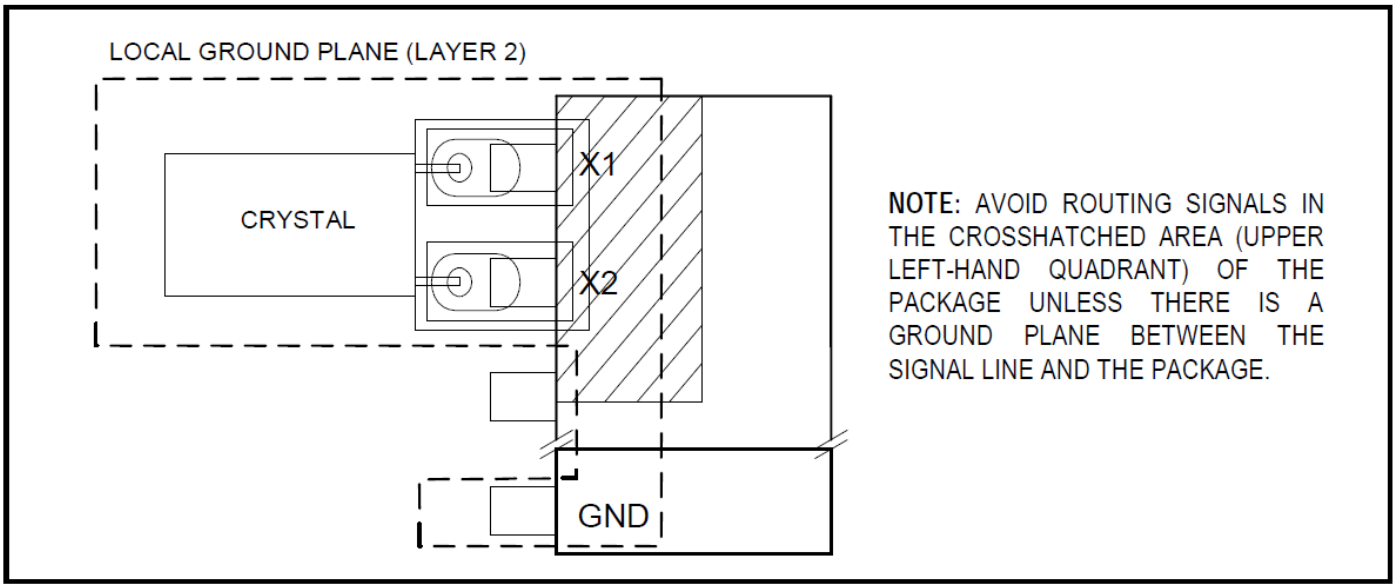


Figure 2 typical PC board layout for isolating the crystal and oscillator from noise

Functional Description

1. Overview of Functions

1.1. Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

For PT7C4339 on a power-on reset (POR), the time and date are set to 00:00:00 01/01/00 (hh:mm:ss DD/MM/YY) and the Day register is set to 01.

1.2. Alarm function

This device has two alarm system (Alarm 1 and Alarm 2) that outputs interrupt signals from SQW/INT to CPU when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm is be selectable between on and off for matching alarm or repeating alarm.

1.3. Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. Frequencies are selectable: 1, 4.096k, 8.192k, 32.768 kHz.

1.4. Interface with CPU

Data is read and written via the I2C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz, which supports the I2C bus's high-speed mode.

1.5. Oscillator fail detect

When oscillator fail, PT7C4339 OSF bit will be set.

1.6. Oscillator enable/disable

Oscillator can be enabled or disabled at the same time by /EOSC bit.

2. Operation

The PT7C4339 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels.

3. Power Control

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (Table 2). After V_{CC} returns above V_{PF}, read and write access is allowed after t_{REC} (Figure 1). On the first application of power to the device the time and date registers are reset to 01/01/00 01 00:00:00 (MM/DD/YY DOW HH:MM:SS).

Table 2:

Power Control Supply Condition	Read/Write Access	Power by
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$	No	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

4. Registers

4.1. Allocation of registers

Addr. (hex) *1	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	0	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
03	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01-12)	Century	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Alarm 1: Seconds	A1M1*2	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2*2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3*2	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4*2	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0B	Alarm 2: Minutes	A2M2*3	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3*3	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4*3	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0E	Control	/EOSC*4	0	BBSQI	RS2*5	RS1*5	INTCN*6	A2IE*7	A1IE*7
0F	Status	OSF*9	0	0	0	0	0	A2F*8	A1F*8
10	Trickle charger	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0

Caution points:

*1. PT7C4339 uses 8 bits for address. For excess 10H address, PT7C4339 will not respond (no acknowledge signal was given).
*2. Alarm 1 mask bits. Select alarm repeated rate when an alarm occurs.
*3. Alarm 2 mask bits. Select alarm repeated rate when an alarm occurs.
*4. Oscillator enable/disable bit.
*5. Square wave output frequency select.
*6. Interrupt output pin select bit.
*7. Alarm 1 and alarm 2 enable bits.
*8. Alarm 1 and alarm 2 flag bits.
*9. Oscillators stop flag.
*10. All bits marked with "0" are read-only bits. Their value when read is always "0".

4.2. **Control and status register**

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
0E	Control	/EOSC	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE
	(default)	0	0	0	1	1	0	0	0
0F	Status	OSF	0	0	0	0	0	A2F	A1F
	(default)	1	0	0	0	0	0	Undefined	Undefined

1) Oscillator related bits

/EOSC

Enable oscillator bit.

/EOSC	Data	Description
Read / Write	0	Starts the oscillator. Default
	1	The oscillator is stopped.

2) BBSQI

Battery-Backed Square-Wave and Interrupt Enable bit.

BBSQI	Data	Description
Read / Write	0	The SQW/INT pin goes high impedance when VCC falls below the power-fail trip point. Default
	1	Enables the square wave or interrupt output when VCC is absent and the PT7C4339 is being powered by the VBACKUP pin.

3) Square wave frequency selection bits

RS2, RS1

Square wave Rate Select. These bits control the frequency of the square-wave output when the square wave has been enabled.

RS2, RS1	Data	SQW output freq. (Hz)
Read / Write	00	1
	01	4.096k
	10	8.192k
	11	32.768k Default

4) OSF

Oscillator Stop Flag

Logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on VCC is insufficient to support oscillation.
3) The /EOSC bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

5) Interrupt related bits

INTCN

Interrupt Output pin select bit. This bit controls the relationship between the two alarms and the interrupt output pins.

INTCN	Data	Description
Read/write	1	A match between the timekeeping registers and the alarm 1 or alarm 2 registers activate the SQW/INT pin (provided that the alarm is enabled).
	0	In this configuration, a square wave is output on the SQW/INT pin. Default

A1IE

Alarm 1 Interrupt Enable.

A1IE	Data	Description
Read/write	0	The A1F bit does not initiate the SQW/INT signal. Default
	1	Permits the alarm 1 flag (A1F) bit in the status register to assert SQW/INT.

A1F

Alarm 1 Flag.

A1F	Data	Description
Read / Write	0	The time does not match the alarm 1 registers. Default
Read	1	A logic 1 in the Alarm 1 Flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/INT pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

A2IE

Alarm 2 Interrupt Enable.

A2IE	Data	Description
Read/write	0	The A2F bit does not initiate an interrupt signal. Default
	1	Permits the alarm 2 flag (A2F) bit in the status register to assert SQW/INT (when INTCN = 1).

A2F

Alarm 2 Flag.

A1F	Data	Description
Read / Write	0	The time does not match the alarm 2 registers. Default
Read	1	A logic 1 in the Alarm 2 Flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/INT pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

4.3. **Time Counter**

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
02	Hours	0	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Any registered imaginary time should be replaced with correct time, otherwise it will cause the clock counter malfunction.

12, /24 bit

This bit is used to select between 12-hour clock system and 24-hour clock system.

12, /24	Data	Description
Read / Write	0	24-hour system
	1	12-hour system

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12, /24	Description	Hours register
0	24-hour time display	
1	12-hour time display	

24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	52 (AM 12)	12	72 (PM 12)
01	41 (AM 01)	13	61 (PM 01)
02	42 (AM 02)	14	62 (PM 02)
03	43 (AM 03)	15	63 (PM 03)
04	44 (AM 04)	16	64 (PM 04)
05	45 (AM 05)	17	65 (PM 05)
06	46 (AM 06)	18	66 (PM 06)
07	47 (AM 07)	19	67 (PM 07)
08	48 (AM 08)	20	68 (PM 08)
09	49 (AM 09)	21	69 (PM 09)
10	50 (AM 10)	22	70 (PM 10)
11	51 (AM 11)	23	71 (PM 11)

***** Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

4.4. **Days of the week Counter**

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Days of the week	0	0	0	0	0	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

4.5. **Calendar Counter**

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  - Range from 1 to 30 (for April, June, September and November).
  - Range from 1 to 29 (for February in leap years).
  - Range from 1 to 28 (for February in ordinary years).
  - Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
04	Dates	0	0	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
05	Months	Century*1	0	0	M10	M8	M4	M2	M1
	(default)	Undefined	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

***1:** The century bit is toggled when the years register overflows from 99 to 00.

4.6. **Alarm Register**

Alarm 1, Alarm 2 Register

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Alarm 1: Seconds	A1M1*1	S40	S20	S10	S8	S4	S2	S1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
08	Alarm 1: Minutes	A1M2*1	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
09	Alarm 1: Hours	A1M3*1	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0A	Alarm 1: Day, Date	A1M4*1	Day, /Date*1	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0B	Alarm 2: Minutes	A2M2*2	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0C	Alarm 2: Hours	A2M3*2	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0D	Alarm 2: Day, Date	A2M4*2	Day, /Date*2	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

***1** Note: Alarm mask bit, using to select Alarm 1 alarm rate.

***2** Note: Alarm mask bit, using to select Alarm 2 alarm rate.

4.7. **Alarm Function**

Related register

Addr. (hex)	Function	Register definition							
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
02	Hours	0	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
03	Days of the week	0	0	0	0	0	W4	W2	W1
04	Dates	0	0	D20	D10	D8	D4	D2	D1
07	Alarm 1: Seconds	A1M1	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0B	Alarm 2: Minutes	A2M2	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0E	Control	/EOSC	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE
0F	Status	OSF	0	0	0	0	0	A2F	A1F

Note: Alarm function does not support different hour system adopted in time and alarm register.

The PT7C4339 contains two time-of-day/date alarms. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes - each alarm can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits.

When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h ~ 04h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table3 and Table4 show the possible settings.

The Day, /Date bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 ~ 5 of that register reflects the day of the week or the date of the month. If the bit is written to logic 0, the alarm is the result of a match with date of the month. If the bit is written to logic 1, the alarm is the result of a match with day of the week.

When the PT7C4339 register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output (SQW/INT) signals. The match is tested on the once-per-second update of the time and date registers.

Table3. Alarm 1 Mask Bits

Day, /Date	Alarm 1 register mask bits				Alarm rate
	A1M4	A1M3	A1M2	A1M1	
×	1	1	1	1	Alarm once per second
×	1	1	1	0	Alarm when seconds match
×	1	1	0	0	Alarm when minutes and seconds match
×	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match
Others					Ignored.

Table4. Alarm 2 Mask Bits

Day, /Date	Alarm 2 register mask bits			Alarm rate
	A2M4	A2M3	A2M2	
×	1	1	1	Alarm once per minute (00 seconds of every minute)
×	1	1	0	Alarm when minutes match
×	1	0	0	Alarm when hours, minutes
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match
Others				Ignored.

4.8. **Trickle Charger Register (10h)**

The simplified schematic in Figure 5 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode-select (DS) bits (bits 2 and 3) select whether or not a diode is connected between VCC and VBACKUP. The ROUT bits (bits 0 and 1) select the value of the resistor connected between VCC and VBACKUP. Table 5 shows the bit values.

Table5. Trickle Charger Register (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Function
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 200Ω resistor
1	0	1	0	1	0	0	1	One diode, 200Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Initial power-up values

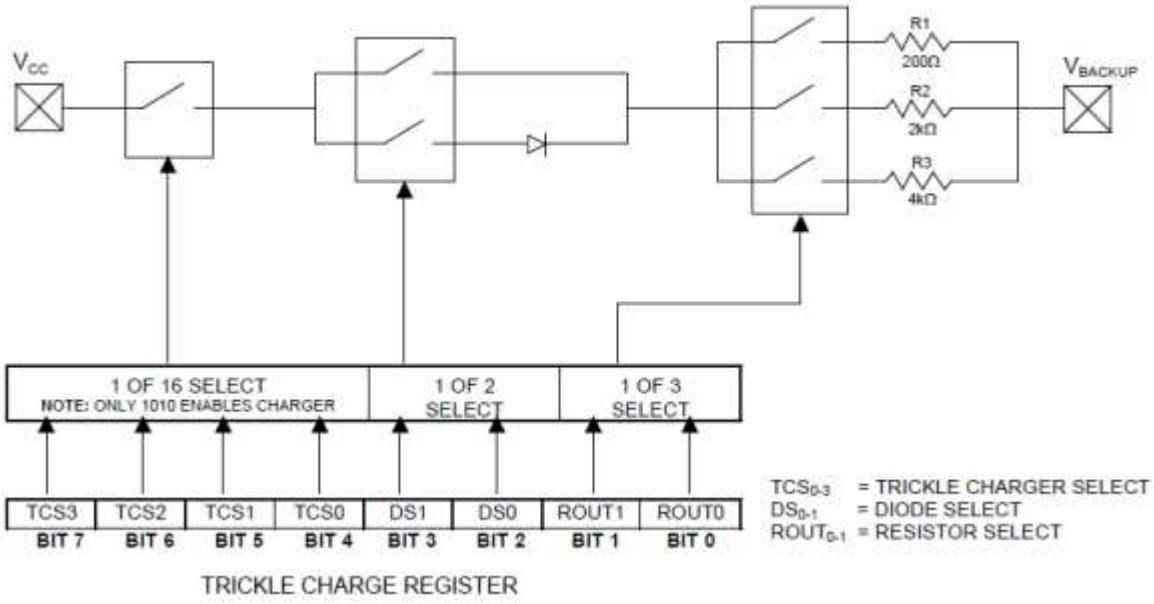
Warning: The ROUT value of 200Ω must not be selected whenever V_{CC} is greater than 3.63V.

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a 3.3V system power supply is applied to VCC and a super cap is connected to VBACKUP. Also assume that the trickle charger has been enabled with a diode and resistor R2 between VCC and VBACKUP. The maximum current IMAX would therefore be calculated as follows:

IMAX = (3.3V - diode drop) / R2 ≈ (3.3V - 0.7V) / 2kΩ ≈ 1.3mA

As the super cap or battery charges, the voltage drop between VCC and VBACKUP decreases and therefore the charge current decreases.

Figure 5: Programmable Trickle Charger



5. I²C Bus Interface

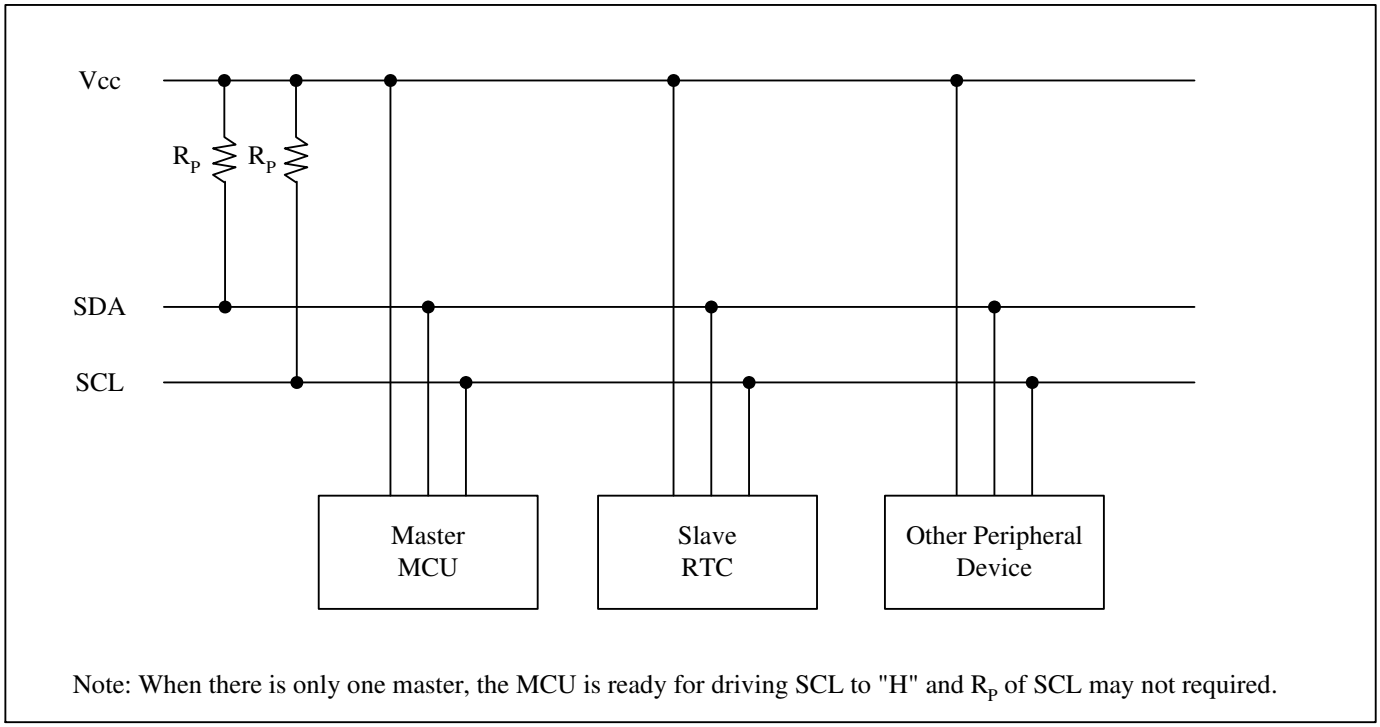
5.1. Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

5.2. System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VCC line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Note: When there is only one master, the MCU is ready for driving SCL to "H" and R_P of SCL may not required.

Fig2. System configuration

5.3. Starting and Stopping I2C Bus Communications

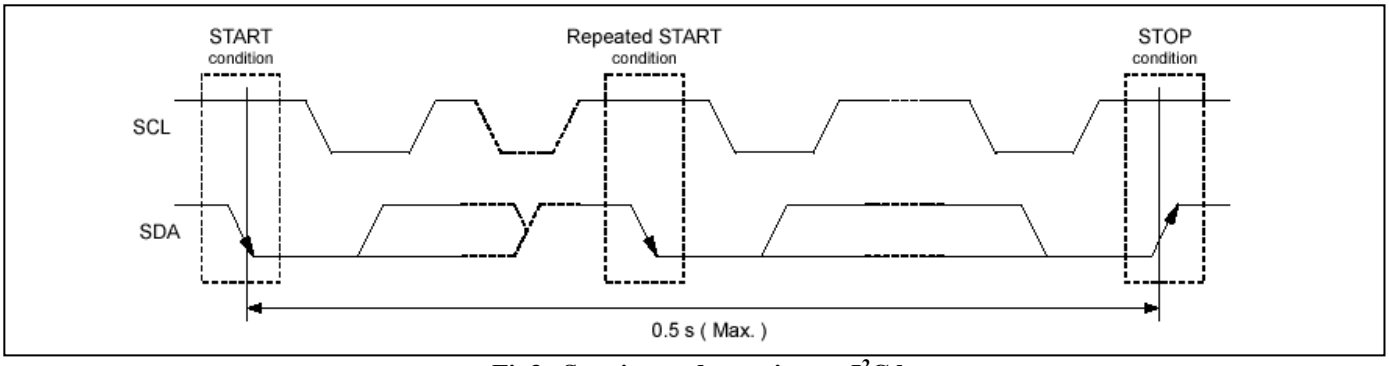


Fig3. Starting and stopping on I^2C bus

1) START condition, repeated START condition, and STOP condition

a) START condition

SDA level changes from high to low while SCL is at high level

b) STOP condition

SDA level changes from low to high while SCL is at high level

c) Repeated START condition (RESTART condition)

In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Data Transfers and Acknowledge Responses during I^2C-BUS Communication

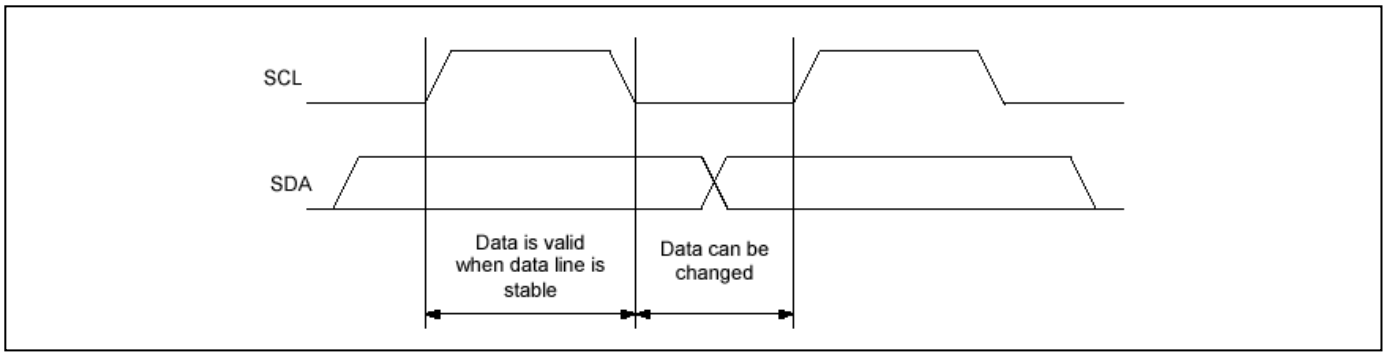
a) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.

The receiver (receiving side) captures data while the SCL line is at high level.

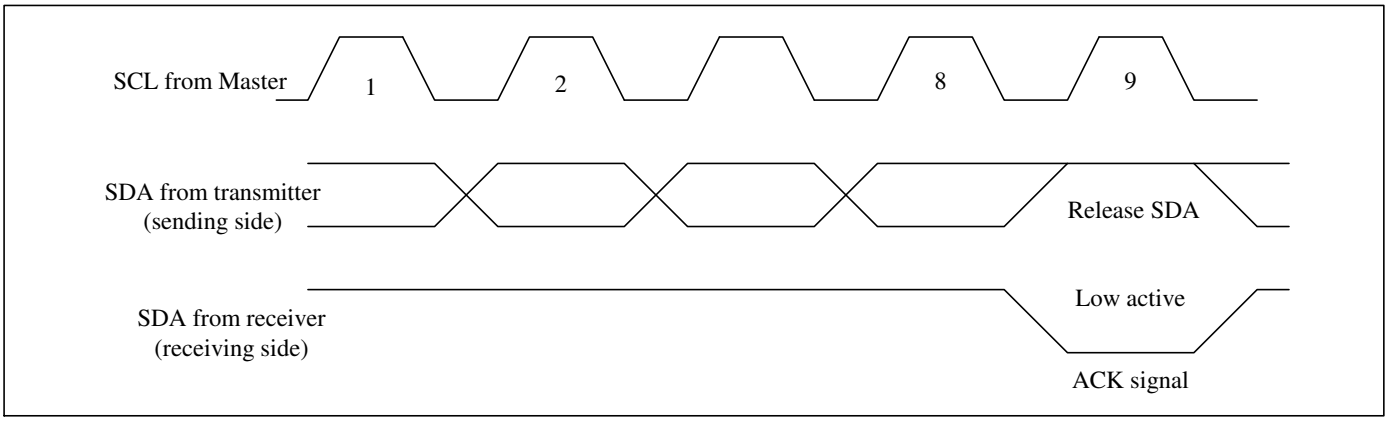


*__Note:__ with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

b) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

5.4. Slave Address

The I2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.

All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

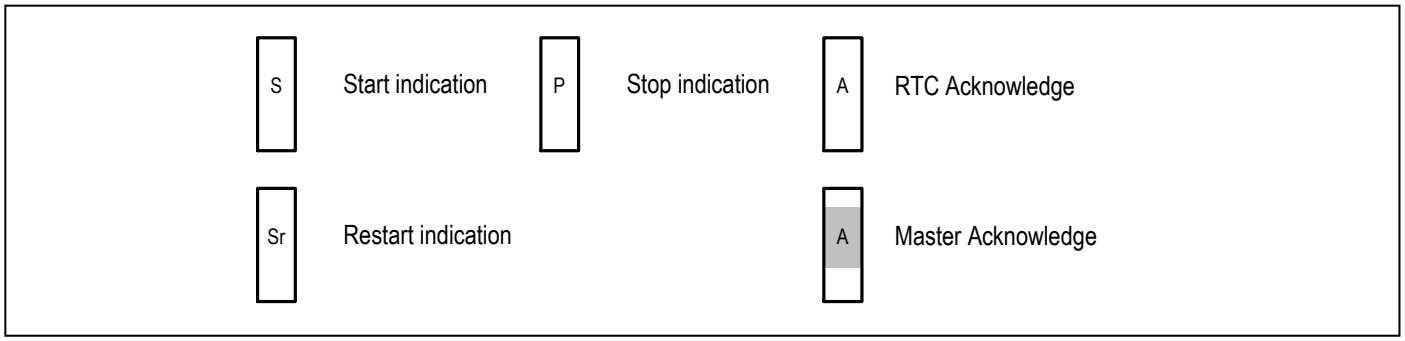
Slave addresses have a fixed length of 7 bits. See table for the details.

An R/W bit is added to each 7-bit slave address during 8-bit transfers.

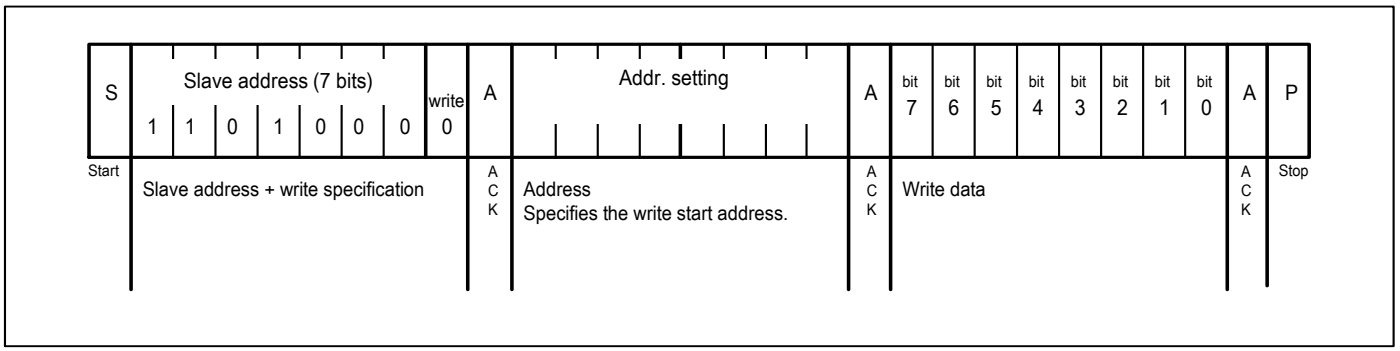
Table

Operation	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	D1 h	1	1	0	1	0	0	0	1 (= Read)
Write	D0 h								0 (= Write)

5.5. I²C Bus's Basic Transfer Format

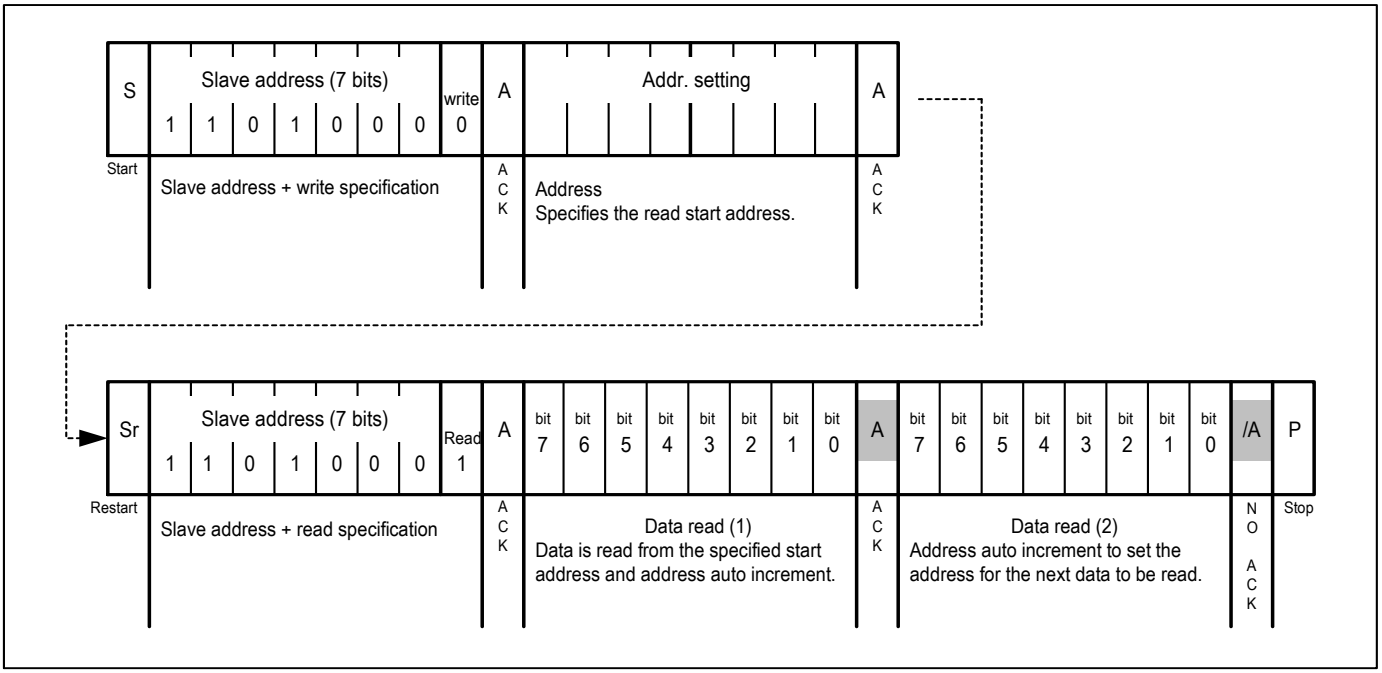


1) Write via I²C bus

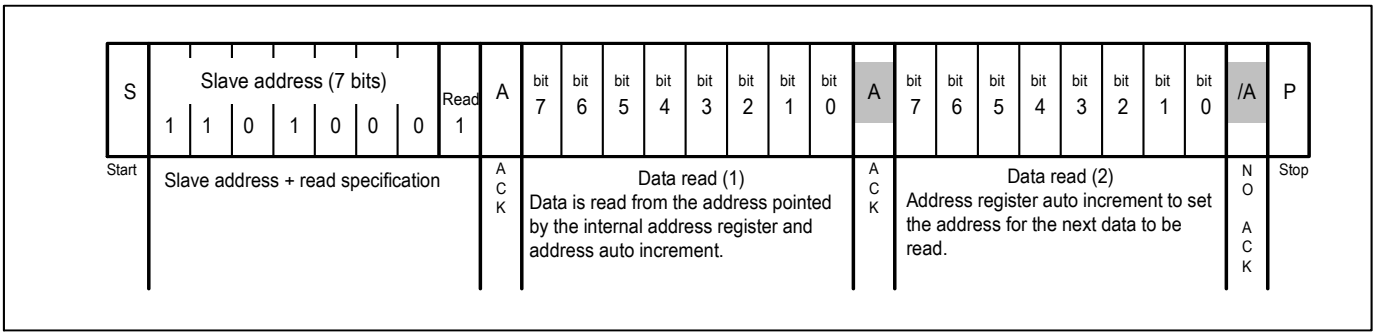


2) Read via I²C bus

(1) Standard read



(2) Simplified read

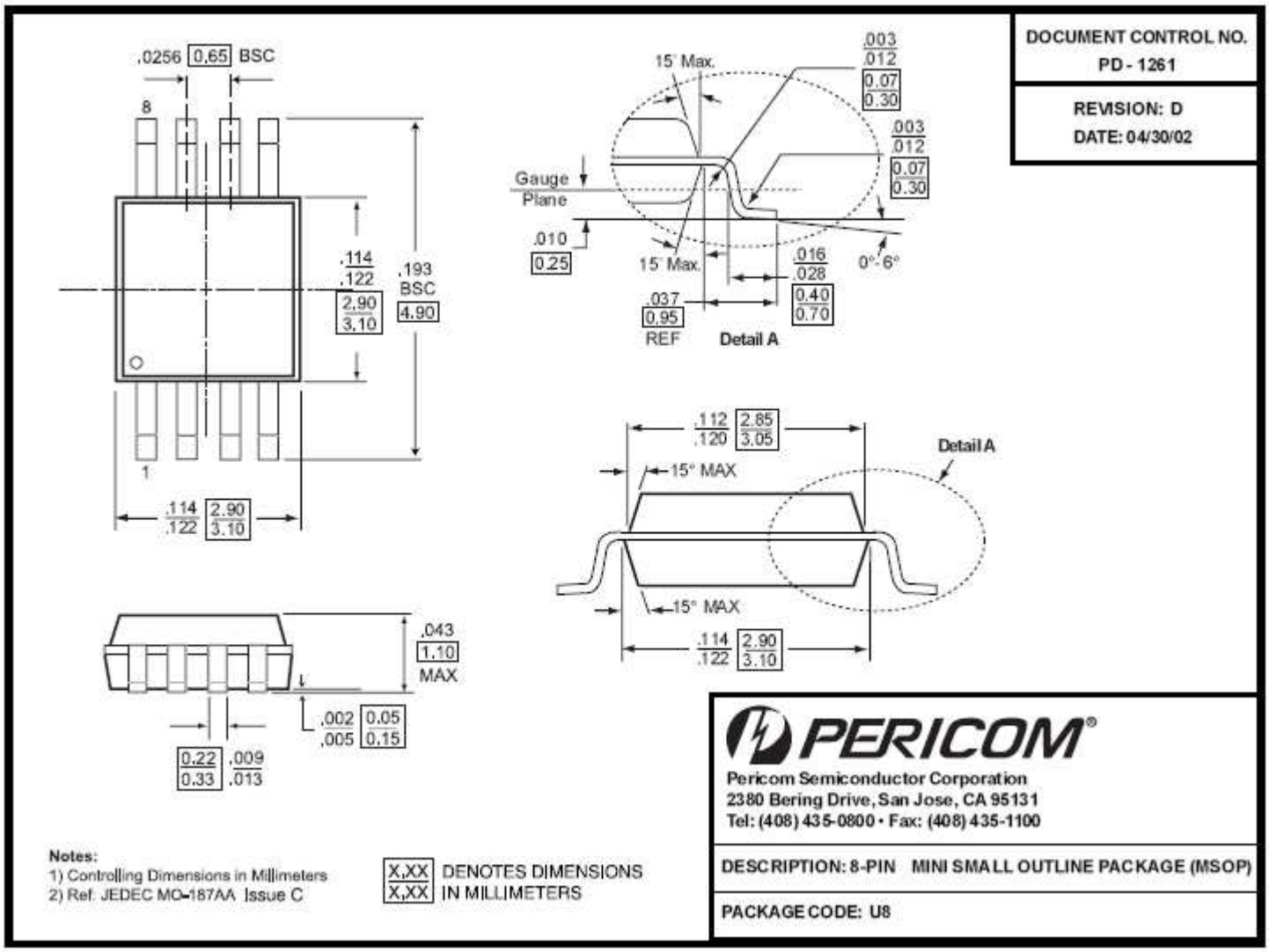


Note:

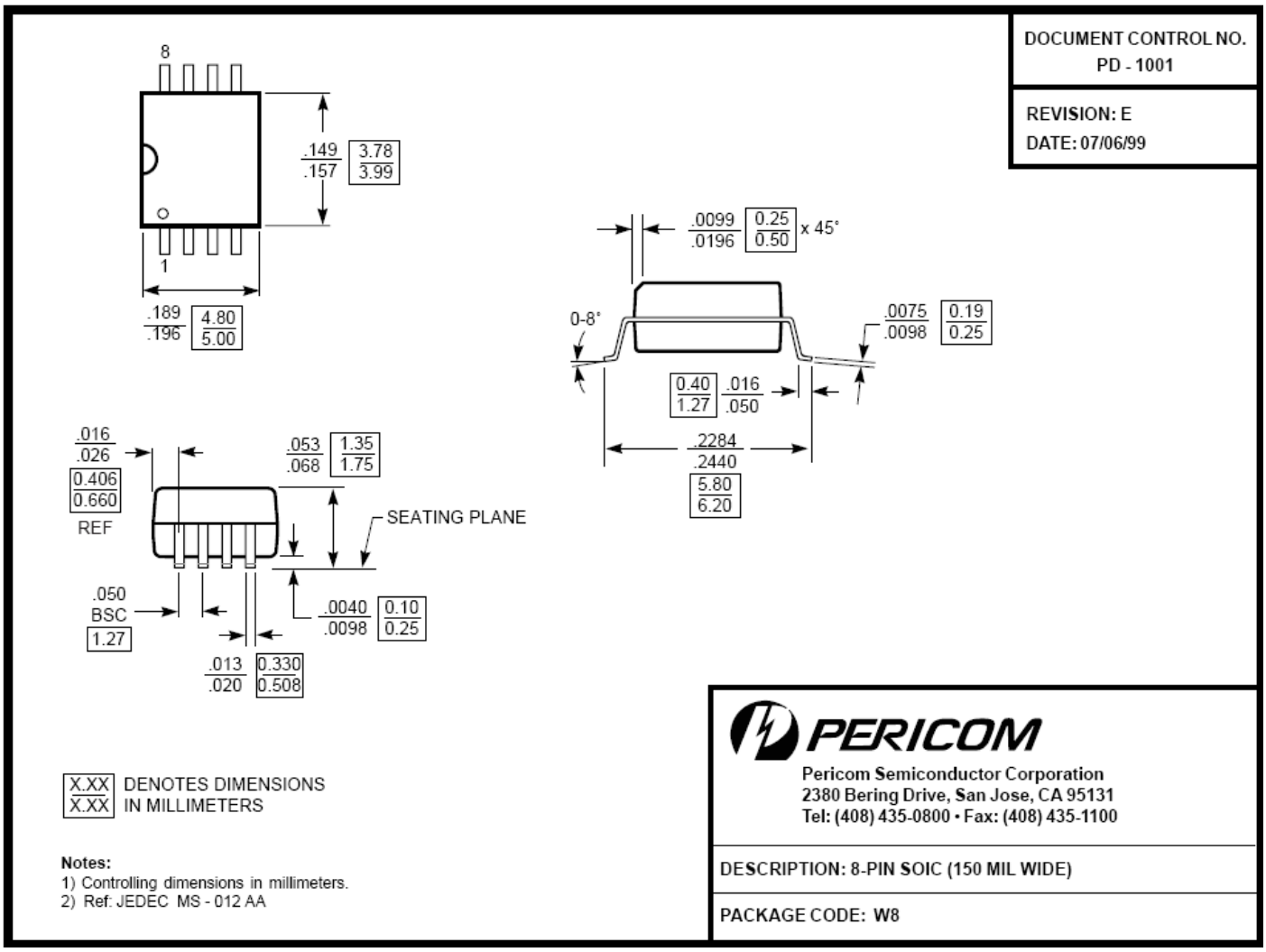
1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
2. 49H, 4AH are used as test mode address. Customer should not use the addresses.

Mechanical Information

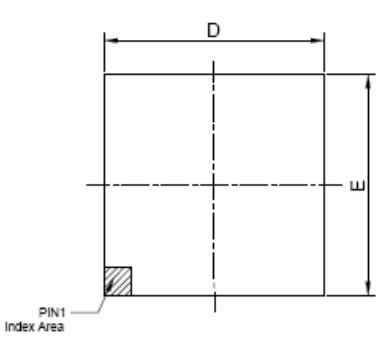
MSOP-8L



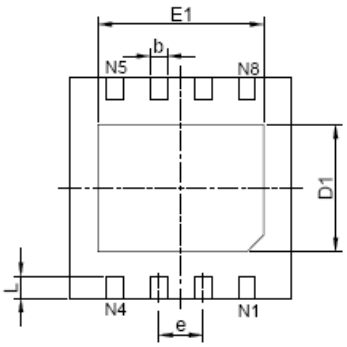
SOIC-8L


DOCUMENT CONTROL NO.
PD - 1001
REVISION: E
DATE: 07/06/99
8
1
.149 / .157 3.78 / 3.99
.189 / .196 4.80 / 5.00
.0099 / .0196 0.25 / 0.50 x 45°
0-8°
.0075 / .0098 0.19 / 0.25
0.40 / 1.27 .016 / .050
.2284 / .2440 5.80 / 6.20
.016 / .026 0.406 / 0.660 REF
.053 / .068 1.35 / 1.75
SEATING PLANE
.050 BSC 1.27
.0040 / .0098 0.10 / 0.25
.013 / .020 0.330 / 0.508
X.XX / X.XX DENOTES DIMENSIONS IN MILLIMETERS
Notes:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS - 012 AA
PERICOM
Pericom Semiconductor Corporation
2380 Bering Drive, San Jose, CA 95131
Tel: (408) 435-0800 • Fax: (408) 435-1100
DESCRIPTION: 8-PIN SOIC (150 MIL WIDE)
PACKAGE CODE: W8

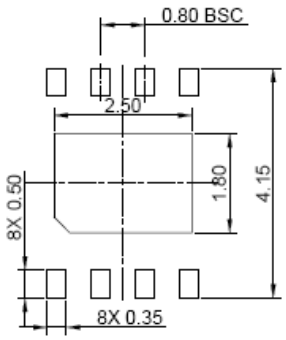
TDFN4.0x4.0-8L



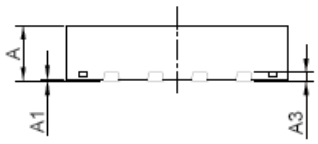
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN(unit:mm)



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.95	1.05
A1	0.00	0.05
A3	0.15 REF	
D	4.00 BSC	
E	4.00 BSC	
D1	2.20	2.40
E1	2.90	3.10
b	0.25	0.35
e	0.80 TYP	
L	0.35	0.45

Notes:
1. Ref: JEDEC MO-287A

PERICOM Enabling Serial Connectivity — DATE: 03/14/14

DESCRIPTION: 8-Pin, DFN, 4X4

PACKAGE CODE: ZSA (ZSA8)

DOCUMENT CONTROL # : PD-2183 REVISION: --

Ordering Information

Part No.	Package Code	Package
PT7C4339UE	U	Lead free and Green 8-pin MSOP
PT7C4339UEX	U	Lead free and Green 8-pin MSOP Tape/Reel
PT7C4339WE	W	Lead free and Green 8-pin SOIC
PT7C4339WEX	W	Lead free and Green 8-pin SOIC Tape/Reel
PT7C4339CZSAE*	ZSA	Lead free and Green 8-pin TDFN4.0x4.0

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel
- * Pls connect Pericom for available.