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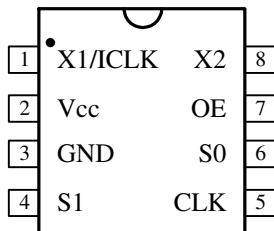


PLL Clock Multiplier

Features

- Zero ppm multiplication error
- Input crystal frequency of 5 - 30 MHz
- Input clock frequency of 1 - 50 MHz
- Output clock frequencies up to 200 MHz
- Peak to Peak Jitter less than 200ps over 200ns interval (100~200MHz)
- Low period jitter 50ps (100~200MHz)
- 9 selectable frequencies controlled by S0, S1 pins
- Operating voltages of 3.0 to 5.5V
- Tri-state output for board level testing
- Lead free SOIC-8 package

Pin Configuration



Pin Description

Name	Pin No.	Type	Description
X1/ICLK	1	X1	Crystal connection or clock input.
Vcc	2	P	Connect to +3.3V or +5V.
GND	3	P	Connect to ground.
S1	4	T1	Multiplier select pin, connect to GND or Vcc or floating (no connection).
CLK	5	O	Clock output per Table below.
S0	6	T1	Multiplier select pin 0, connect to GND or Vcc or floating (no connection).
OE	7	I	Output enable, tri-state CLK output when low. Internal pull-up.
X2	8	XO	Crystal connection. Leave unconnected for clock input.

Description

The PT7C4511 is a high performance frequency multiplier, which integrates Analog Phase Lock Loop techniques.

The PT7C4511 is the most cost effective way to generate a high quality, high frequency clock output from a lower frequency crystal or clock input. It is designed to replace crystal oscillators in most electronic systems, clock multiplier and frequency translation.

Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 200 MHz.

The complex Logic divider is the ability to generate nine different popular multiplication factors, allowing one chip to output many common frequencies.

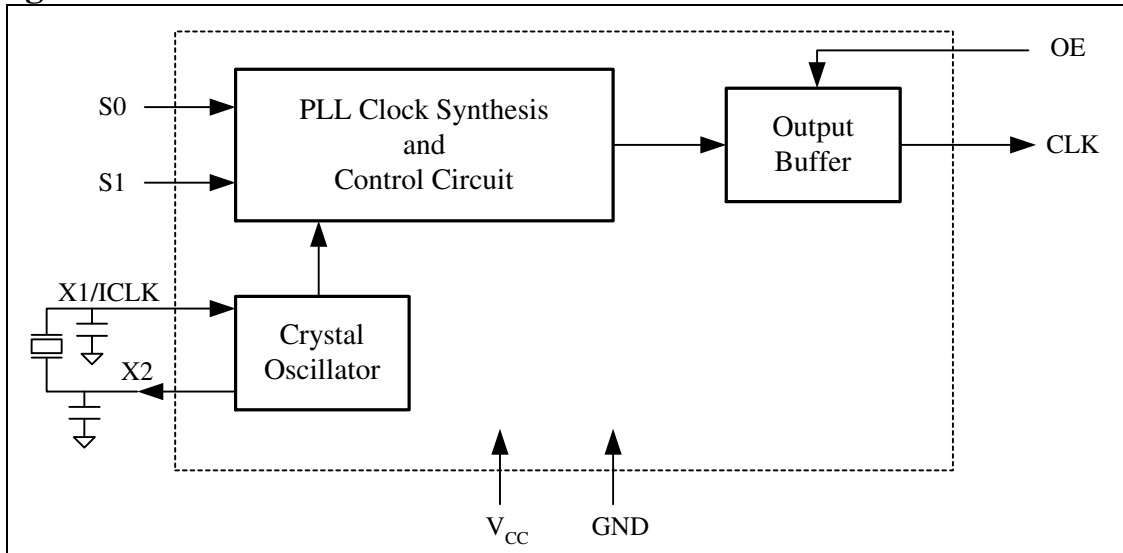
The device also has an Output Enable pin that tri-states the clock output when the OE pin is taken low. This product is intended for clock generation and frequency translation with low output jitter (variation in the output period).

Clock Output Table

S1	S0	CLK
0	0	×4
0	M	×(16/3)
0	1	×5
M	0	×2.5
M	M	×2
M	1	×(10/3)
1	0	×6
1	M	×3
1	1	×8

- 1) **Note:** CLK output frequency=ICLK × 4.
- 2) **Note:** M=Leave unconnected (self-biases to Vcc/2).

Block Diagram



External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the PT7C4511 must be isolated from system power supply noise to perform optimally. A decoupling capacitor of 0.01 μ F or 0.1 μ F must be connected between VCC and the GND. It must be connected close to the PT7C4511 to minimize lead inductance. No external power supply filtering is required for the PT7C4511.

Series Termination Resistor

A 33 Ω terminating resistor can be used next to the CLK pin for trace lengths over one inch.

Crystal Load Capacitors

There is no on-chip capacitance build-in chip. A parallel resonant, fundamental mode crystal should be used. The device crystal connections should include

pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should equal $C_L * 2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 15 pF load capacitance, each crystal capacitor would be 30pF.

Maximum Ratings

Storage Temperature.....	-65 $^{\circ}$ C to +150 $^{\circ}$ C
Ambient Operating Temperature.....	-40 $^{\circ}$ C to +85 $^{\circ}$ C
Supply Voltage to Ground Potential (V _{CC}).....	-0.3V to +7.0V
Inputs(Referenced to GND).....	-0.5V to V _{CC} +0.5V
Clock Output(Referenced to GND).....	-0.5V to V _{CC} +0.5V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Sym	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	Supply voltage	-	3.0	-	5.5	V
T _A	Operating temperature	-	-40	-	+85	$^{\circ}$ C

DC Electrical Characteristics

($V_{CC} = 3.3V \pm 0.3V$, $T_A = -40 \sim 85^\circ C$, unless otherwise noted)

Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	-	V _{CC}	3	3.3	3.6	V
I _{CC}	Supply Current	no load, 20MHz crystal, 100MHz output	V _{CC}	-	12	20	mA
V _{IH}	Input Logic High	-	ICLK	(V _{CC} /2)+1	V _{CC} /2	-	V
			OE	2	-	-	V
V _{IL}	Input Logic Low	-	ICLK	-	V _{CC} /2	(V _{CC} /2)-1	V
			OE	-	-	0.8	V
V _{IH}	Input Logic High	-	S0, S1	V _{CC} -0.5	-	-	V
V _{IM}	Input mid-level	-	S0, S1	-	V _{CC} /2	-	V
V _{IL}	Input Logic Low	-	S0, S1	-	-	0.5	V
V _{OH}	High-level output voltage	I _{OH} = -12mA	CLK	2.4	-	-	V
V _{OL}	Low-level output voltage	I _{OL} = 12mA	CLK	-	-	0.4	V
R	Internal pull up resistance	-	OE	-	270	-	kΩ
I _S	Short Circuit Current	-	CLK	-	±30	-	mA

($V_{CC} = 5.0V \pm 0.5V$, $T_A = -40 \sim 85^\circ C$, unless otherwise noted)

Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	-	V _{CC}	4.5	5.0	5.5	V
I _{CC}	Supply Current	no load, 20MHz crystal, 100MHz output	V _{CC}	-	20	30	mA
V _{IH}	Input Logic High	-	ICLK	(V _{CC} /2)+1	V _{CC} /2	-	V
			OE	0.65*V _{CC}	-	-	V
V _{IL}	Input Logic Low	-	ICLK	-	V _{CC} /2	(V _{CC} /2)-1	V
			OE	-	-	0.8	V
V _{IH}	Input Logic High	-	S0, S1	V _{CC} -0.4	-	-	V
V _{IM}	Input mid-level	-	S0, S1	-	V _{CC} /2	-	V
V _{IL}	Input Logic Low	-	S0, S1	-	-	0.4	V
V _{OH}	High-level output voltage	I _{OH} = -12mA	CLK	V _{CC} -0.5	-	-	V
V _{OL}	Low-level output voltage	I _{OL} = 12mA	CLK	-	-	0.4	V
R	Internal pull up resistance	-	OE	-	270	-	kΩ
I _S	Short Circuit Current	-	CLK	-	±70	-	mA

AC Electrical Characteristics

($V_{CC} = 3.3V \pm 0.3V$, $T_A = -40 \sim 85^\circ C$, unless otherwise noted)

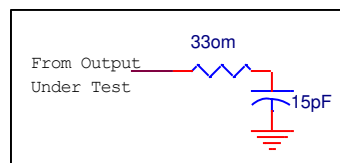
Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	-	ICLK	1	-	50	MHz
f_{OUT}	Output Frequency	$V_{CC}: 3.0$ to $3.6V$	CLK	20	-	180	MHz
t_R	Output clock rise time	0.8 to $2.0V$, $15pF$ load	CLK	-	1	-	ns
t_F	Output clock fall time	2.0 to $0.8V$, $15pF$ load	CLK	-	1	-	ns
Duty	Output clock duty cycle	At $V_{CC}/2$, below $160MHz$	CLK	45	50	55	%
		At $V_{CC}/2$, $160MHz$ to $180MHz$	CLK	40	-	60	%
	PLL bandwidth	-	-	10	-	-	kHz
	Output enable time	OE high to output on	-	-	-	50	ns
	Output disable time	OE low to tri-rise	-	-	-	50	ns
	Period Jitter	$70MHz \sim 180MHz$	CLK	-	50	100	ps
	Jitter over 200ns interval	$100MHz \sim 180MHz$	CLK	-	-	200	ps

($V_{CC} = 5.0V \pm 0.5V$, $T_A = -40 \sim 85^\circ C$, unless otherwise noted)

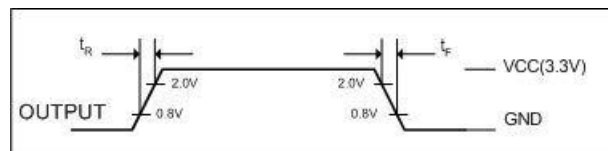
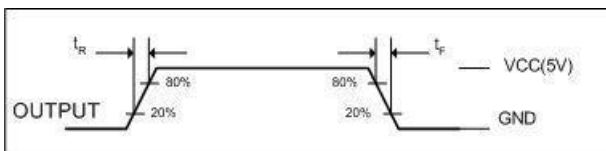
Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	-	ICLK	1	-	50	MHz
f_{OUT}	Output Frequency	$V_{CC}: 4.5$ to $5.5V$	CLK	20	-	200	MHz
t_R	Output clock rise time	$20\%V_{CC}$ to $80\%V_{CC}$, $15pF$ load	CLK	-	1.2	-	ns
t_F	Output clock fall time	$80\%V_{CC}$ to $20\%V_{CC}$, $15pF$ load	CLK	-	1.2	-	ns
Duty	Output clock duty cycle	At $V_{CC}/2$, below $160MHz$	CLK	45	50	55	%
		At $V_{CC}/2$, $160MHz$ to $200MHz$	CLK	40	-	60	%
	PLL bandwidth	-	-	10	-	-	kHz
	Output enable time	OE high to output on	-	-	-	50	ns
	Output disable time	OE low to tri-rise	-	-	-	50	ns
	Period Jitter	$70MHz \sim 200MHz$	CLK	-	50	100	ps
	Jitter over 200ns interval	$100MHz \sim 200MHz$	CLK	-	-	200	ps

Test circuits

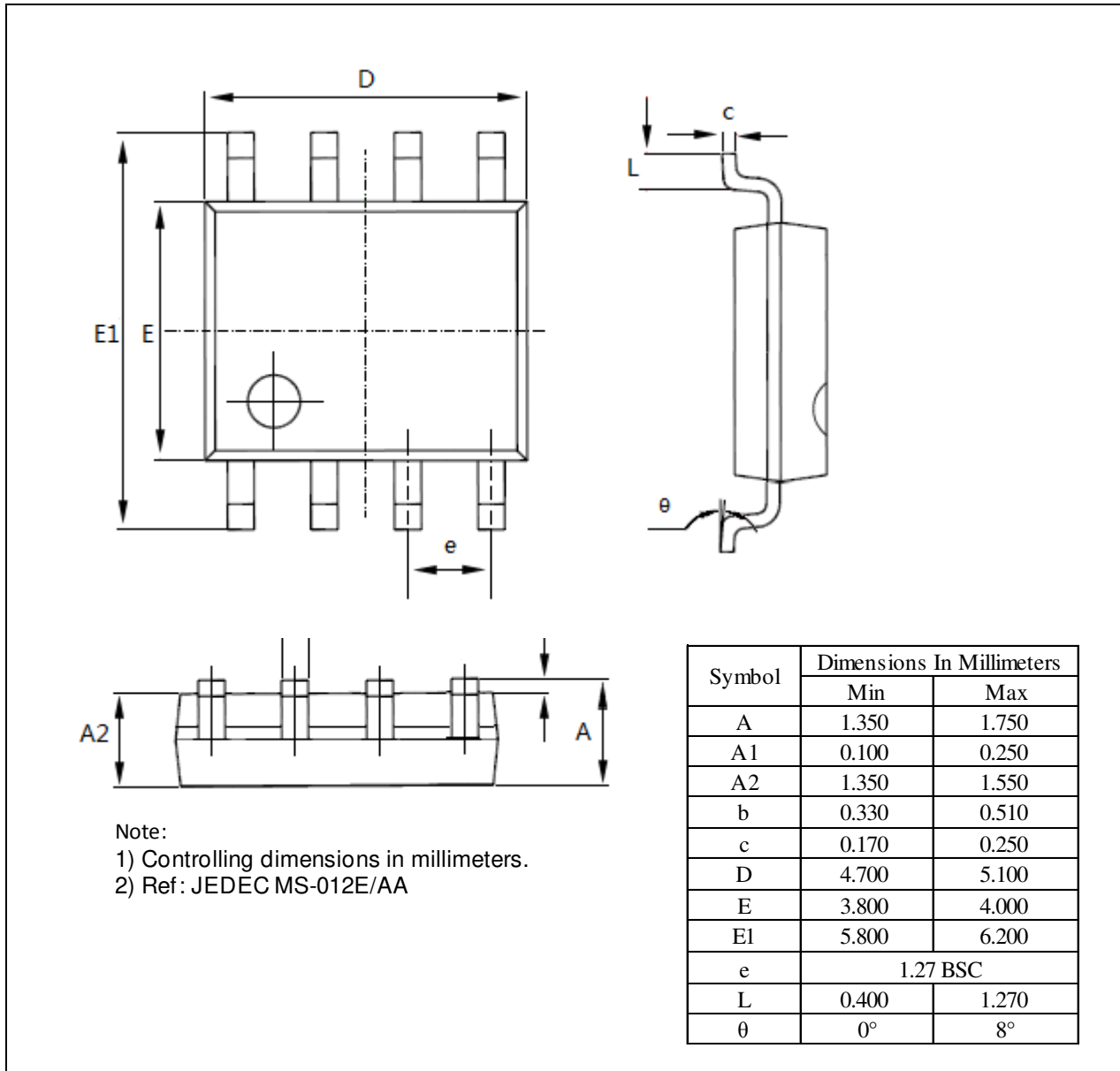
1>Load circuit for output clock duty cycle, rise and fall time Measurement



2>Timing Definitions for output clock rise and fall time Measurement



Mechanical Information
SOIC-8



Ordering Information

Part No.	Package Code	Package
PT7C4511WE	W	Lead free and Green 8-pin SOIC

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