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## Features

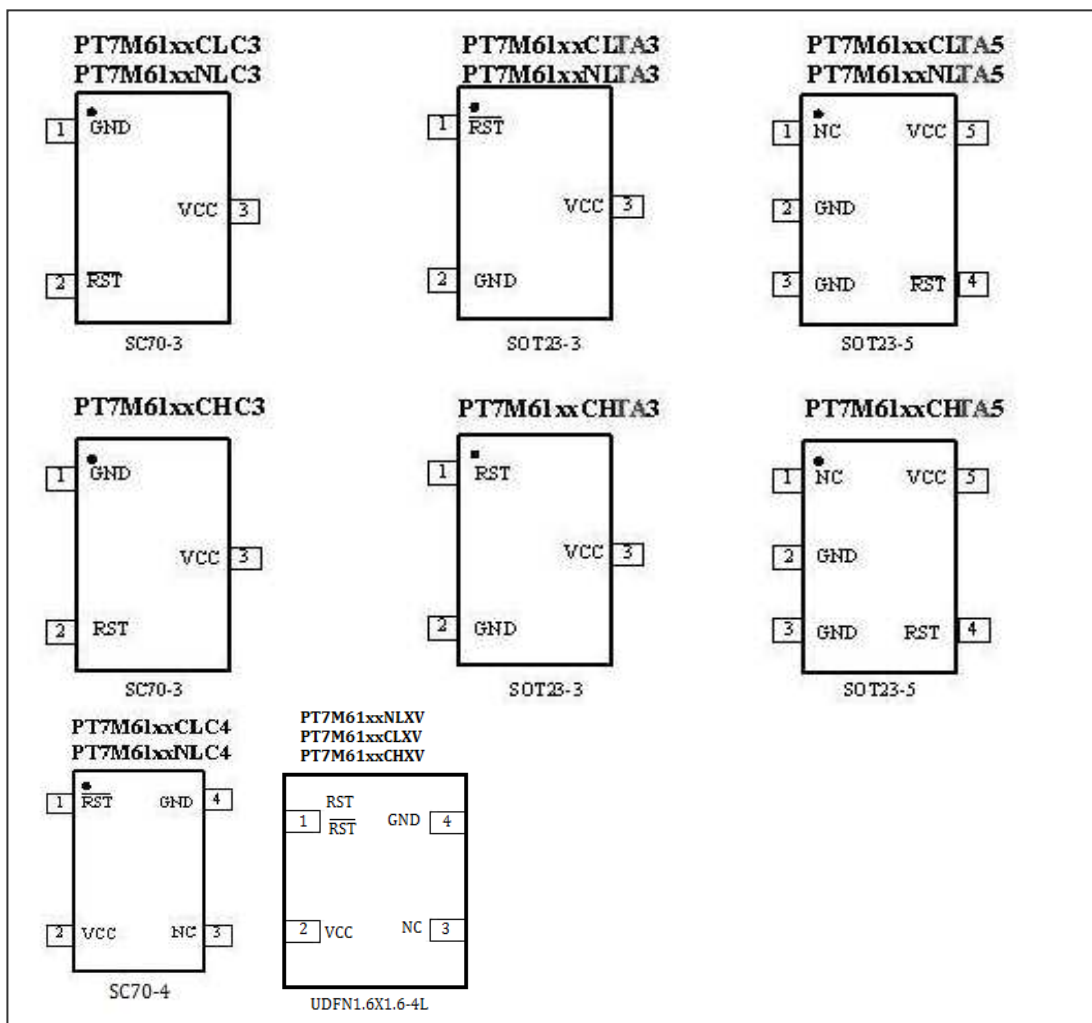
- Highly accurate:  $\pm 1.5\%$  ( $25^{\circ}\text{C}$ )
- Low power consumption:  $1\mu\text{A}$  @  $3.6\text{V}$   $V_{\text{CC}}$
- Detect voltage range: 1.8 to 5V in 100mV increments
- Operating voltage range: 1.2V ~ 5.5V
- Operating temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Detect voltage accuracy over temperature:  $\pm 2.5\% \times \text{Typ}$
- Output configuration: N-channel open drain or CMOS

## Description

The PT7M61xx series of ultra-low-power voltage detectors monitor battery, power-supply and system voltages. Each circuit includes a precision bandgap reference, a comparator, internally trimmed resistor networks that set specified trip thresholds, and an internal 1% and 5% threshold hysteresis circuit. Output is asserted when  $V_{\text{CC}}$  falls below the internal  $V_{\text{TH-}}$  and remains asserted until  $V_{\text{CC}}$  rises above  $V_{\text{TH+}}$  ( $V_{\text{TH+}} = V_{\text{TH-}} \times 1.05$ ). These devices provide excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltages from +1.8V to +5V in 100mV increments. The series are voltage detectors with a propagation delay of 17 $\mu\text{s}$ .

The family is available with three output stage options: push-pull with active-low output, push-pull with active-high output, and open drain with active-low output. These devices specified over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.

## Pin Configuration

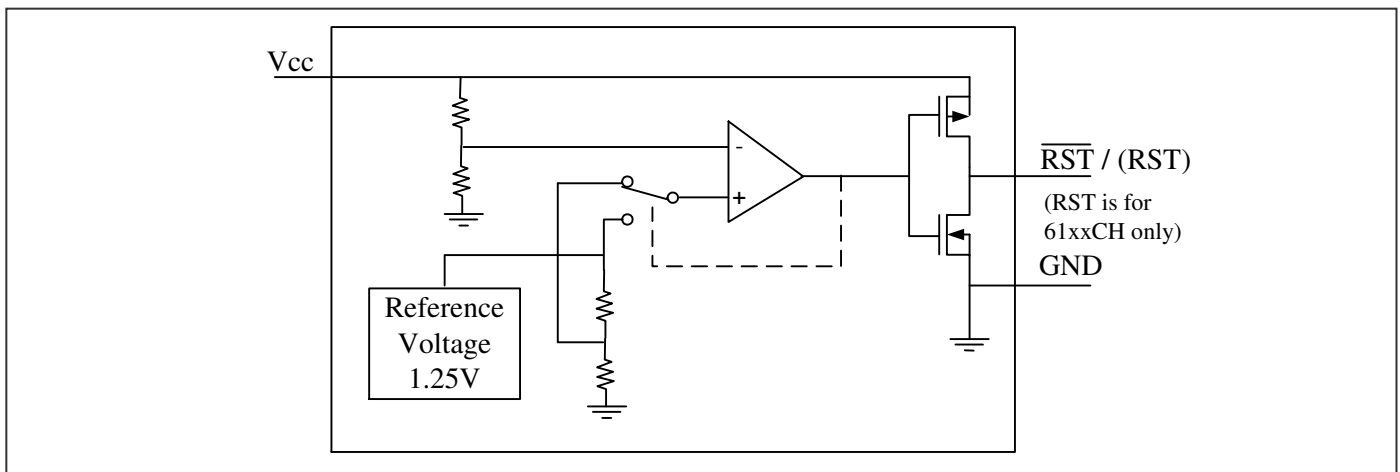


## Pin Description

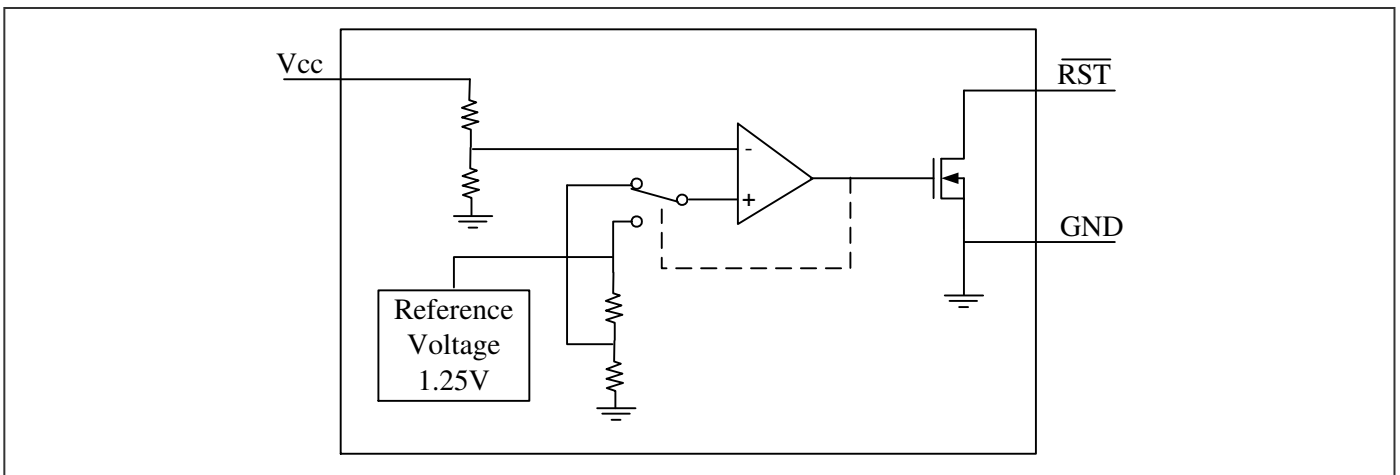
Name	Type	Description
$\overline{\text{RST}}$	O	<b>Reset Output (PT7M61xxCL/NL):</b> $\overline{\text{RST}}$ is asserted when $V_{CC}$ drops below voltage threshold $V_{TH}$ . Active low.
RST	O	<b>Reset Output (PT7M61xxCH).</b> RST is asserted when $V_{CC}$ drops below voltage threshold $V_{TH}$ . Active high.
GND	P	<b>Ground</b>
$V_{CC}$	P	<b>Supply Voltage.</b>

## Block Diagram

Block Diagram of PT7M61xxCL/CH



Block Diagram of PT7M61xxNL



## Maximum Ratings

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage to Ground Potential (V <sub>CC</sub> to GND) .....	-0.3V to +6.0V
DC Input Voltage (All inputs except V <sub>CC</sub> and GND).....	-0.3V to V <sub>CC</sub> +0.3V
DC Output Current (All outputs) .....	20mA
Power Dissipation .....	320mW (Depend on package)

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC Electrical Characteristics

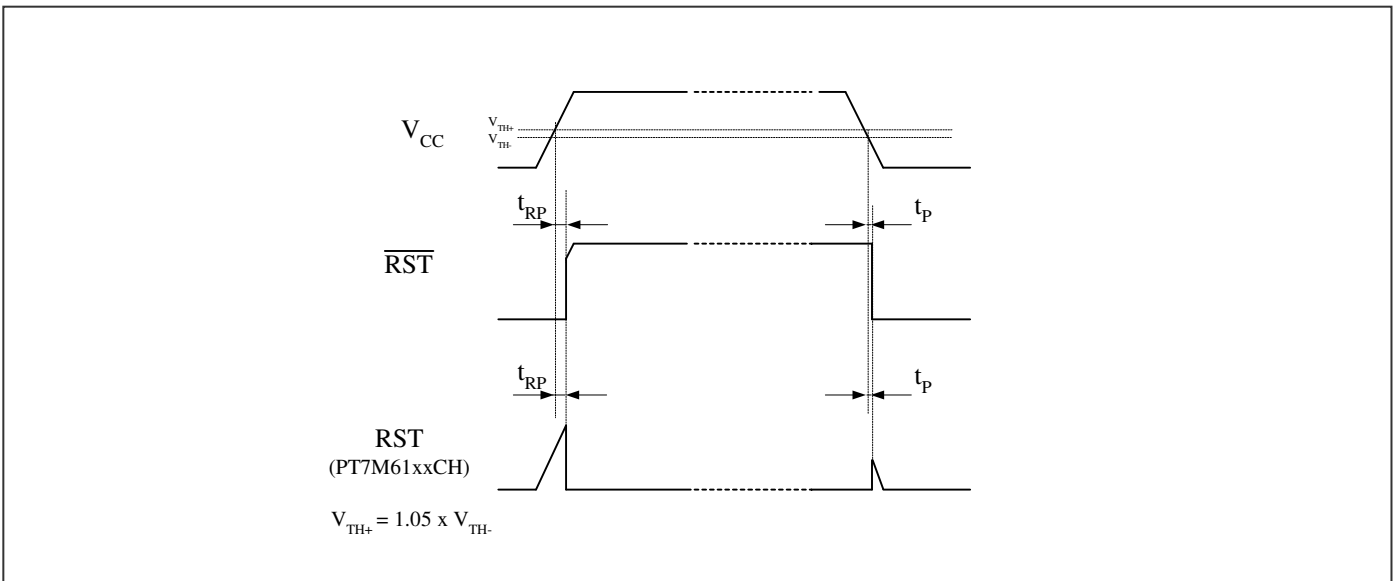
(V<sub>CC</sub> = 1.2V to 5.5V, T<sub>A</sub> = -40~85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C)

Description		Sym.	Test Conditions	Min	Typ	Max	Unit
Supply Voltage		V <sub>CC</sub>	T <sub>A</sub> = 0~70°C	1.0	-	5.5	V
			T <sub>A</sub> = -40~85°C	1.2	-	5.5	
Supply Current		I <sub>CC</sub>	V <sub>CC</sub> = 3.6V. No load.	-	1.0	3.0	μA
			V <sub>CC</sub> = 5V. No load.	-	1.3	3.6	μA
Output Driving	Output high	V <sub>OH</sub>	V <sub>CC</sub> ≥ 1.8V, I <sub>source</sub> = 1mA	0.8×V <sub>CC</sub>	-	-	V
			V <sub>CC</sub> ≥ 2.5V, I <sub>source</sub> = 3mA	0.8×V <sub>CC</sub>	-	-	
			V <sub>CC</sub> ≥ 4.5V, I <sub>source</sub> = 8mA	0.8×V <sub>CC</sub>	-	-	
	Output low	V <sub>OL</sub>	V <sub>CC</sub> ≥ 1.2V, I <sub>sink</sub> = 1mA	-	-	0.3	V
			V <sub>CC</sub> ≥ 2.5V, I <sub>sink</sub> = 4mA	-	-	0.3	
			V <sub>CC</sub> ≥ 4.5V, I <sub>sink</sub> = 9mA	-	-	0.4	
Open-Drain Output Leakage Current		I <sub>LKG</sub>	-	-	-	1	μA
Voltage Threshold		V <sub>TH-</sub>	+25°C	(V <sub>TH-</sub> ) ×0.985	V <sub>TH-</sub>	(V <sub>TH-</sub> ) ×1.015	V
			-40°C~85°C	(V <sub>TH-</sub> ) ×0.975	V <sub>TH-</sub>	(V <sub>TH-</sub> ) ×1.025	
		V <sub>TH+</sub>	+25°C	(V <sub>TH+</sub> ) ×0.985	V <sub>TH+</sub>	(V <sub>TH+</sub> ) ×1.015	
			-40°C~85°C	(V <sub>TH+</sub> ) ×0.975	V <sub>TH+</sub>	(V <sub>TH+</sub> ) ×1.025	
voltage threshold Hysteresis		V <sub>HYST</sub>	V <sub>HYST</sub> = [(V <sub>TH+</sub> )-(V <sub>TH-</sub> )]/(V <sub>TH-</sub> ) ×100%	3	4.5	6	%
			-	-	1	-	

**Note:** V<sub>TH+</sub> = 1.05 × V<sub>TH-</sub>. V<sub>TH-</sub> is voltage threshold when V<sub>CC</sub> falls from high to low. V<sub>TH+</sub> is voltage threshold when V<sub>CC</sub> rises from low to high.

## AC Electrical Characteristics

### Timing diagram

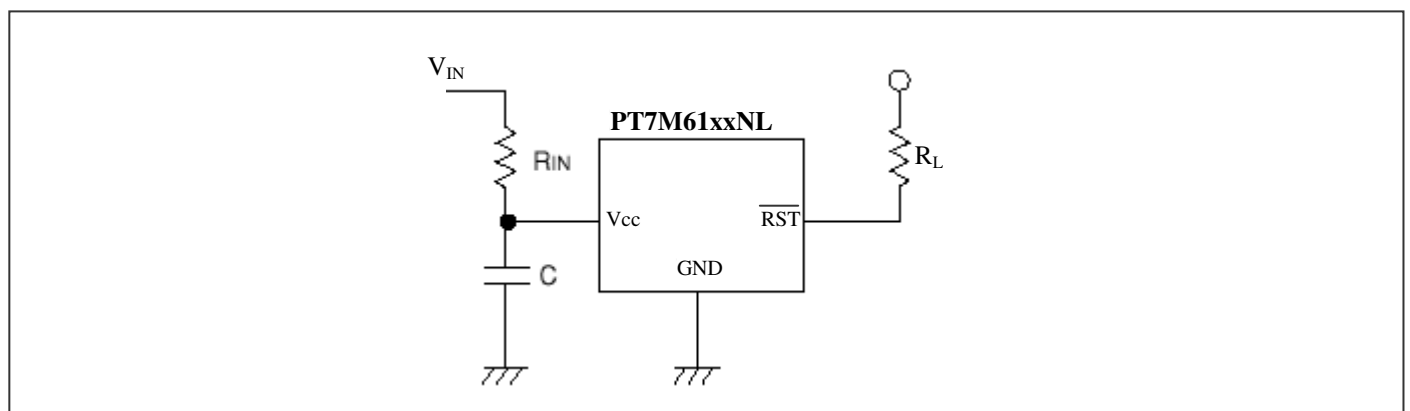


( $V_{CC} = 1.2V$  to  $5.5V$ ,  $T_A = -40 \sim 85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ )

Sym.	Description	Test Conditions	Min	Typ	Max	Unit
$t_{RP}$	Timeout Period	-	-	-	200	$\mu s$
$t_p$	Delay	-	-	50	-	$\mu s$
$t_{overdrive}$	$V_{CC}$ Maximum Transient Duration	Reset threshold overdrive=500mV ( $V_{CC} - V_{th} = -500mV$ )	-	20	-	$\mu s$

## Typical Operation Circuit

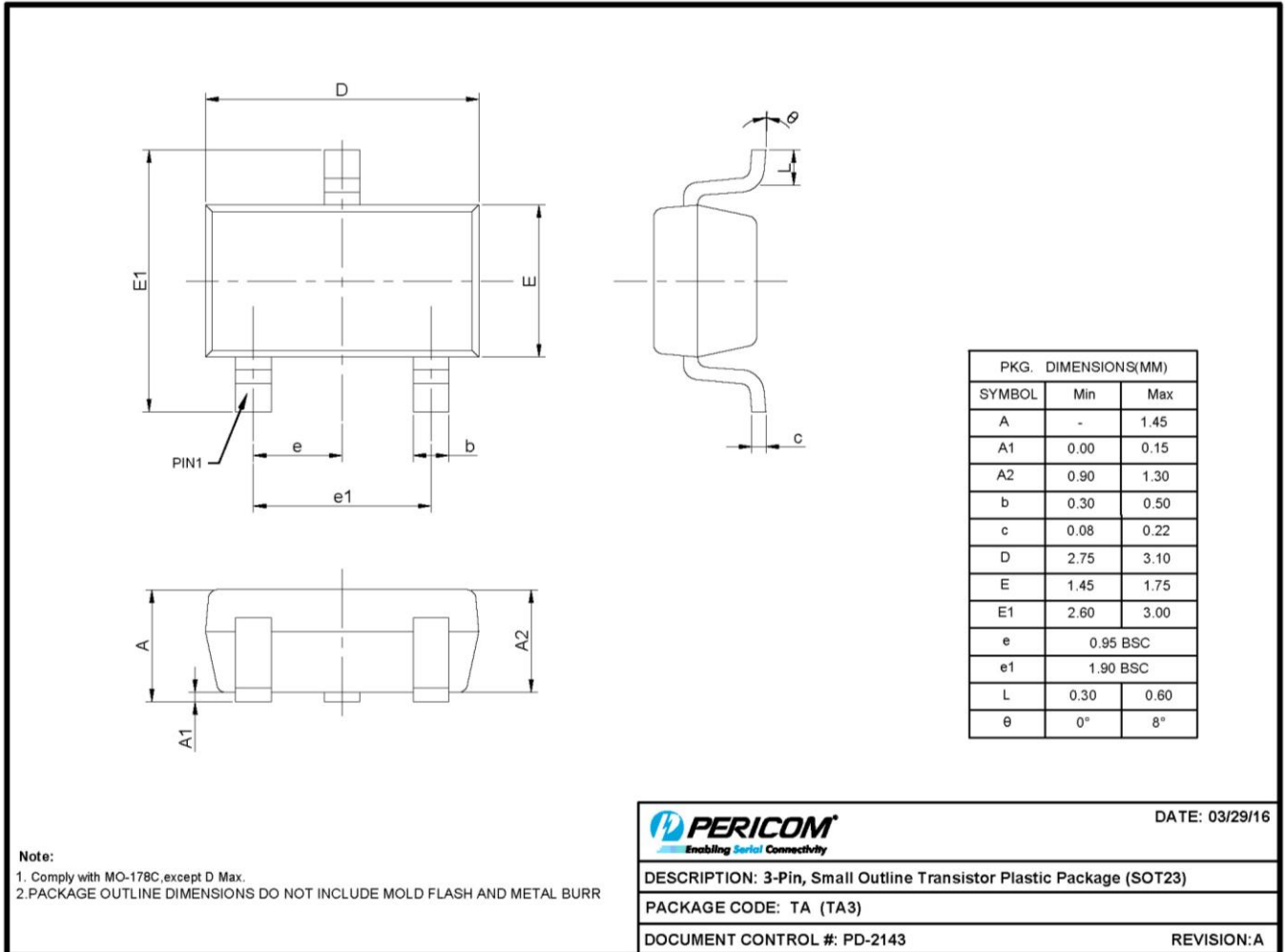
### PT7M61xxNL Application Example



Please use N-ch open drains configuration, when a resistor  $R_{IN}$  is connected between the  $V_{CC}$  pin and power source  $V_{IN}$ . In such cases, please ensure that  $R_{IN}$  is less than  $10k\Omega$  and that  $C$  is more than  $0.1\mu F$ .  $R_L$  could be  $1k\Omega$  to  $510k\Omega$ .

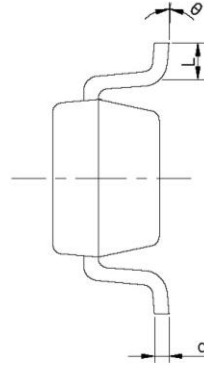
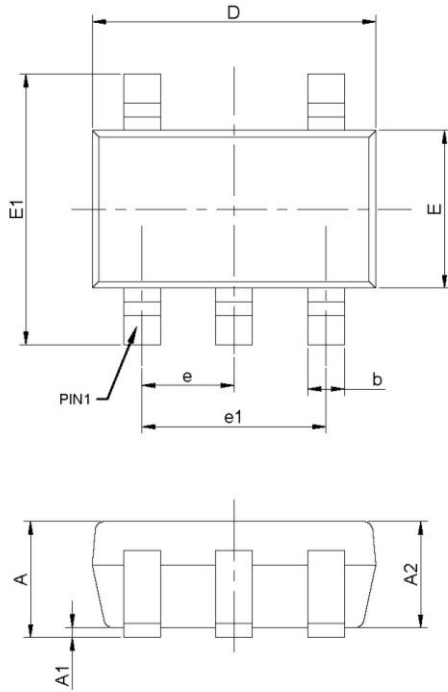
## Mechanical Information

TA3 (SOT23-3)



16-0080

TA5 (SOT23-5)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	-	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.75	3.05
E	1.45	1.75
E1	2.60	3.00
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
$\theta$	0°	8°

Note:

1. Ref: JEDEC MO-178C/AA
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BUR



DATE: 03/29/16

DESCRIPTION: 5-Pin, Small Outline Transistor Plastic Package (SOT23)

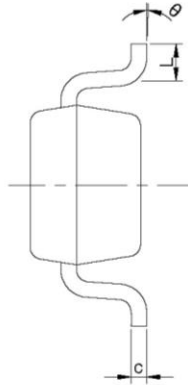
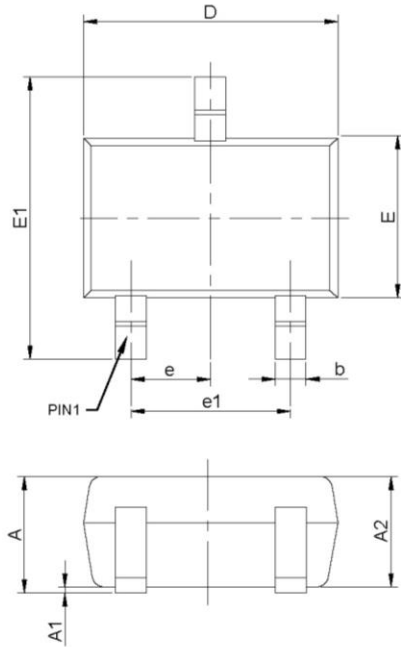
PACKAGE CODE: TA (TA5)

DOCUMENT CONTROL #: PD-2144

REVISION: A

16-0081

C3 (SC70-3)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	-	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.15	0.40
c	0.08	0.22
D	1.80	2.20
E	1.10	1.40
E1	1.75	2.45
e	0.65 BSC	
e1	1.30 BSC	
L	0.26	0.46
theta	0°	8°

Note:

1. Comply with MO-203C, except b Max, D Min, D Max, E1 Min and E1 Max.
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR



DATE: 03/29/16

DESCRIPTION: 3-Pin, SOT323 (SC70)

PACKAGE CODE: C (C3)

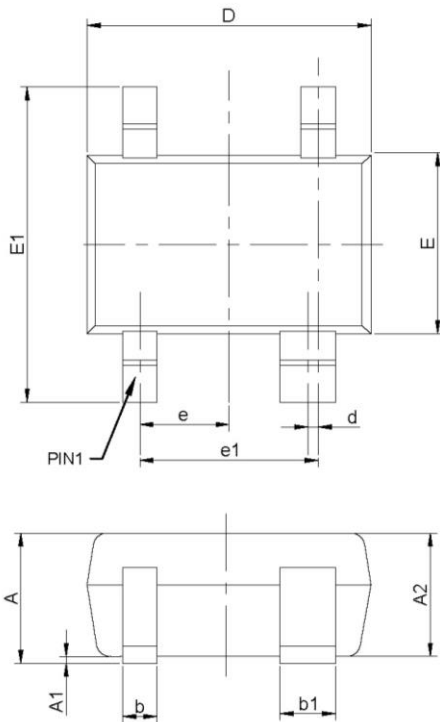
DOCUMENT CONTROL#: PD-2147

REVISION: A

16-0077



C4 (SC70-4)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.90	1.10
A1	0.00	0.10
A2	0.90	1.00
b	0.25	0.40
b1	0.35	0.50
c	0.08	0.15
D	2.00	2.20
d	0.05 TYP	
E	1.15	1.35
E1	2.15	2.45
e	0.65 TYP	
e1	1.20	1.40
L	0.26	0.46
θ	0°	8°

Notes:

1. Ref. JEDEC MO-203B



DATE: 06/18/13

DESCRIPTION: 4-Pin, SOT343 (SC70)

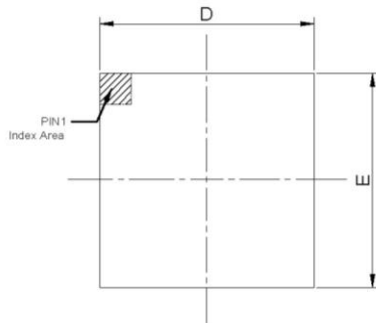
PACKAGE CODE: C (C4)

DOCUMENT CONTROL# PD-2148

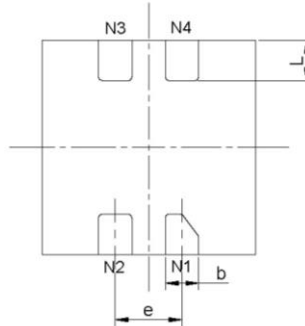
REVISION: --

13-0187

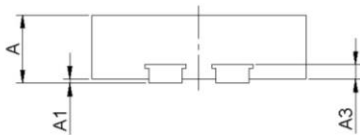
**XV (UDFN1.6x1.6-4L)**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.11 REF	
D	1.55	1.65
E	1.55	1.65
b	0.20	0.30
e	0.50 TYP	
L	0.25	0.35

**Notes:**

1. Ref: JEDEC MO-287A



DATE: 06/18/13

DESCRIPTION: 4-Pin, UDFN, 1.6X1.6, MIS

PACKAGE CODE: XV (XV4)

DOCUMENT CONTROL #: PD-2130

REVISION: --

13-0169

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

## Ordering Information

Part Number	Package Code	Package
PT7M61xxCLTA3E	TA3	3-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M61xxCLTA5E	TA5	5-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M61xxCLC3E	C3	3-Pin, SOT323 (SC70)
PT7M61xxCLC4E	C4	4-Pin, SOT343 (SC70)
*PT7M61xxCHTA3E	TA3	Lead free and Green SOT23-3
*PT7M61xxCHTA5E	TA5	5-Pin, Small Outline Transistor Plastic Package (SOT23)
*PT7M61xxCHC3E	C3	3-Pin, SOT323 (SC70)
*PT7M61xxCHC4E	C4	4-Pin, SOT343 (SC70)
PT7M61xxNLTA3E	TA3	3-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M61xxNLTA5E	TA5	5-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M61xxNLC3E	C3	3-Pin, SOT323 (SC70)
PT7M61xxNLC4E	C4	4-Pin, SOT343 (SC70)
PT7M61xxCLETA3E	TA3	3-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M61xxCLETA5E	TA5	5-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M61xxCLEC3E	C3	3-Pin, SOT323 (SC70)
PT7M61xxCLEC4E	C4	4-Pin, SOT343 (SC70)
*PT7M61xxCHETA3E	TA3	3-Pin, Small Outline Transistor Plastic Package (SOT23)
*PT7M61xxCHETA5E	TA5	5-Pin, Small Outline Transistor Plastic Package (SOT23)
*PT7M61xxCHEC3E	C3	3-Pin, SOT323 (SC70)
*PT7M61xxCHEC4E	C4	4-Pin, SOT343 (SC70)
PT7M61xxNLETA3E	TA3	3-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M61xxNLETA5E	TA5	5-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M61xxNLEC3E	C3	3-Pin, SOT323 (SC70)
PT7M61xxNLEC4E	C4	4-Pin, SOT343 (SC70)
PT7M61xxNLEXVE	XV	4-Pin, 1.6x1.6, MIS (UDFN)
PT7M61xxNLXVE	XV	4-Pin, 1.6x1.6, MIS (UDFN)
PT7M61xxCLXVE	XV	4-Pin, 1.6x1.6, MIS (UDFN)
PT7M61xxCLEXVE	XV	4-Pin, 1.6x1.6, MIS (UDFN)
*PT7M61xxCHXVE	XV	4-Pin, 1.6x1.6, MIS (UDFN)
*PT7M61xxCHEXVE	XV	4-Pin, 1.6x1.6, MIS (UDFN)

### Notes:

- 1: "xx" refer to voltage range, see below table 1.
- 2: Adding E suffix=1% Hysteresis. For example: PT7M61xxCLETA3E.
- 3: None E suffix=5% Hysteresis. For example: PT7M61xxCLTA3E.
- 4: E = Pb-free and Green
- 5: Adding X Suffix= Tape/Reel
- 6: Contact Pericom for availability
- 7: "\*" for CH part, please check the storage with related sales.

**Table 1 Function comparison**

Item	Part No.	Reset Output				Threshold
		Open-Drain		Push-Pull		
		Active high	Active low	Active high	Active low	
1	PT7M61xxCL	-	-	-	√	1.8V to 5.0V in 100mV increments
2	PT7M61xxCH	-	-	√	-	
3	PT7M61xxNL	-	√	-	-	

**Table 2 Suffix “xx” definition of PT7M61xx**

Suffix xx	V <sub>TH</sub> (V)	Suffix xx	V <sub>TH</sub> (V)	Suffix xx	V <sub>TH</sub> (V)	Suffix xx	V <sub>TH</sub> (V)	Suffix xx	V <sub>TH</sub> (V)
18	1.8	25	2.5	32	3.2	39	3.9	46	4.6
19	1.9	26	2.6	33	3.3	40	4.0	47	4.7
20	2.0	27	2.7	34	3.4	41	4.1	48	4.8
21	2.1	28	2.8	35	3.5	42	4.2	49	4.9
22	2.2	29	2.9	36	3.6	43	4.3	50	5.0
23	2.3	30	3.0	37	3.7	44	4.4		
24	2.4	31	3.1	38	3.8	45	4.5		

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