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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



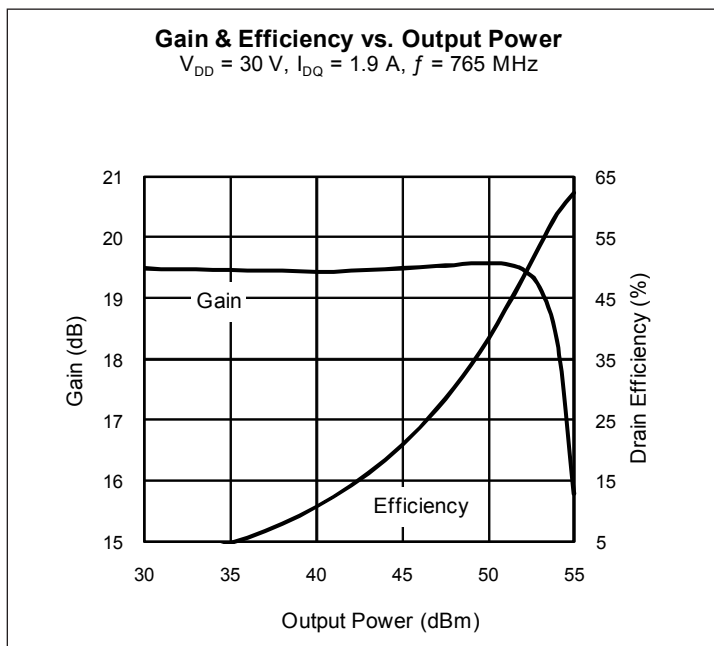
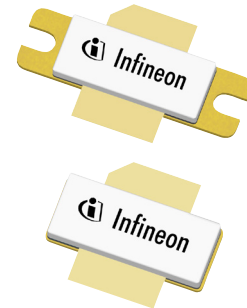
Thermally-Enhanced High Power RF LDMOS FETs 240 W, 725 – 770 MHz

Description

The PTFA072401EL and PTFA072401FL are 240-watt LDMOS FETs designed for use in cellular power amplifier applications in the 725 to 770 MHz frequency band. These devices feature internal I/O matching and thermally-enhanced, open-cavity ceramic packages. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA072401EL
Package H-33288-2

PTFA072401FL
Package H-34288-2



Features

- Broadband internal matching
- Typical two-carrier WCDMA performance at 770 MHz, 30 V
 - Average output power = 40 W
 - Linear Gain = 19 dB
 - Efficiency = 25%
 - Intermodulation distortion = -39 dBc
- Typical CW performance, 770 MHz, 30 V
 - Output power at P_{1dB} = 240 W
 - Efficiency = 58%
- Integrated ESD protection
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 30 V, 240 W (CW) output power
- Thermally-enhanced packages, Pb-free and RoHS compliant with low gold (<0.25 micron) plating

RF Characteristics

Two-carrier WCDMA Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
 $V_{DD} = 30\text{ V}$, $I_{DQ} = 1800\text{ mA}$, $P_{OUT} = 40\text{ W}$ average, $f_1 = 760\text{ MHz}$, $f_2 = 770\text{ MHz}$, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8.1 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	19	—	dB
Drain Efficiency	η_D	—	25	—	%
Intermodulation Distortion	IMD	—	-39	—	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

$V_{DD} = 30\text{ V}$, $I_{DQ} = 1800\text{ mA}$, $P_{OUT} = 220\text{ W PEP}$, $f = 765\text{ MHz}$, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18	19	—	dB
Drain Efficiency	η_D	43	45	—	%
Intermodulation Distortion	IMD	—	-29	-28	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
On-State Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	1.82	—	Ω
Operating Gate Voltage	$V_{DS} = 30\text{ V}$, $I_{DQ} = 1800\text{ mA}$	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

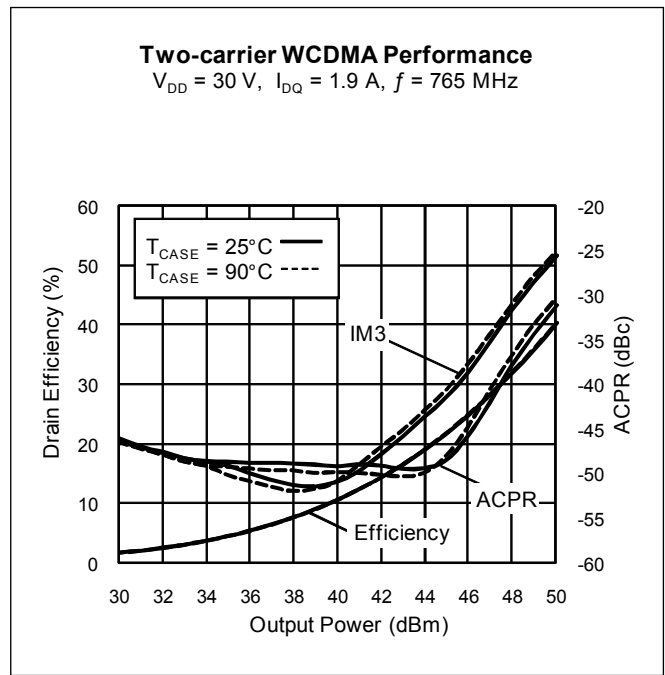
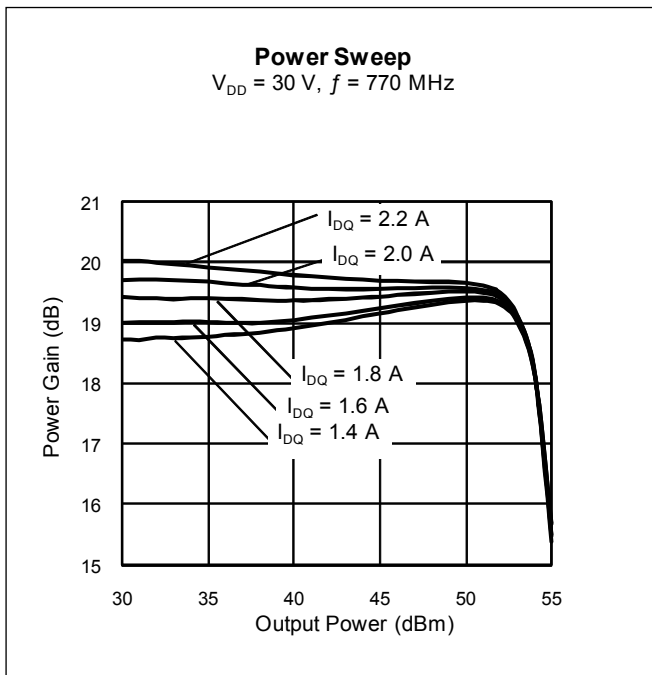
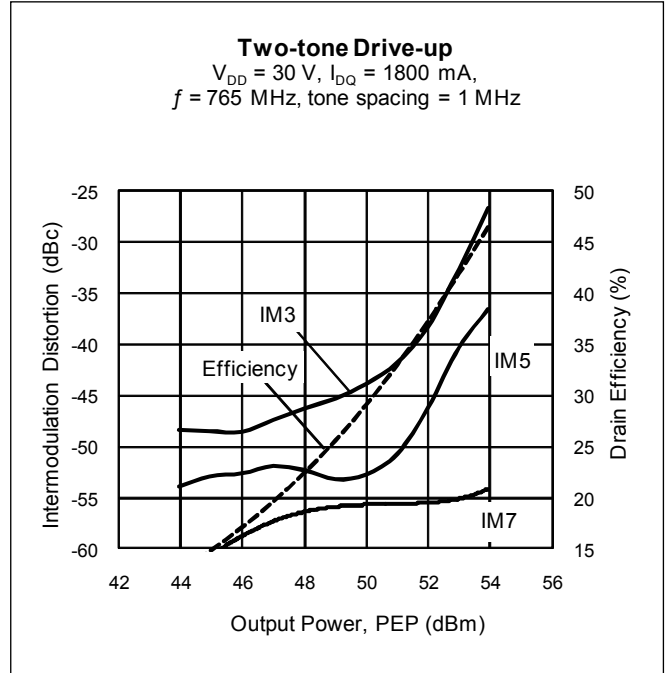
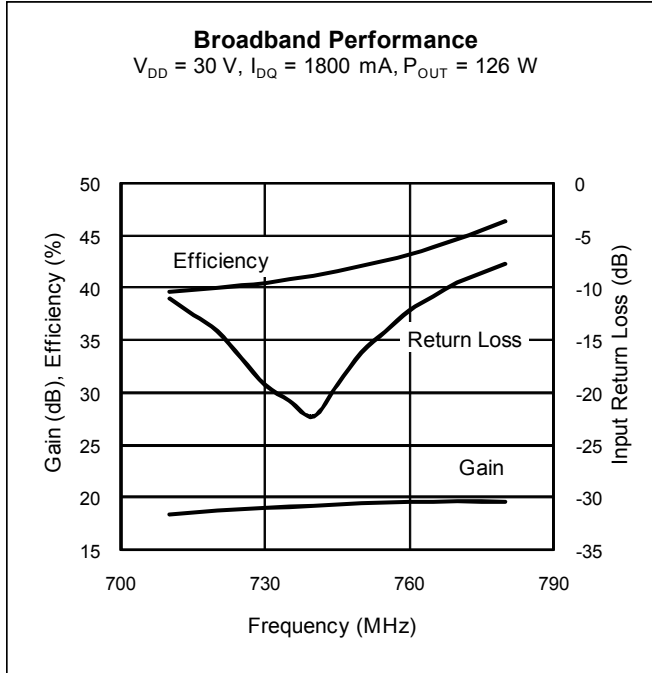
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	-0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Total Device Dissipation	P_D	700	W
		Above 25 $^{\circ}\text{C}$ derate by	4.0
Storage Temperature Range	T_{STG}	-40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$, 240 W CW)	$R_{\theta JC}$	0.28	$^{\circ}\text{C/W}$

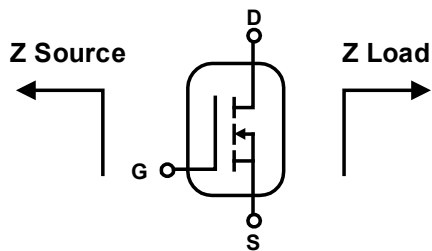
Ordering Information

Type and Version	Package Outline	Package Description	Shipping
PTFA072401EL V4	H-33288-2	Thermally-enhanced slotted flange, single-ended	Tray
PTFA072401FL V4	H-34288-2	Thermally-enhanced earless flange, single-ended	Tray

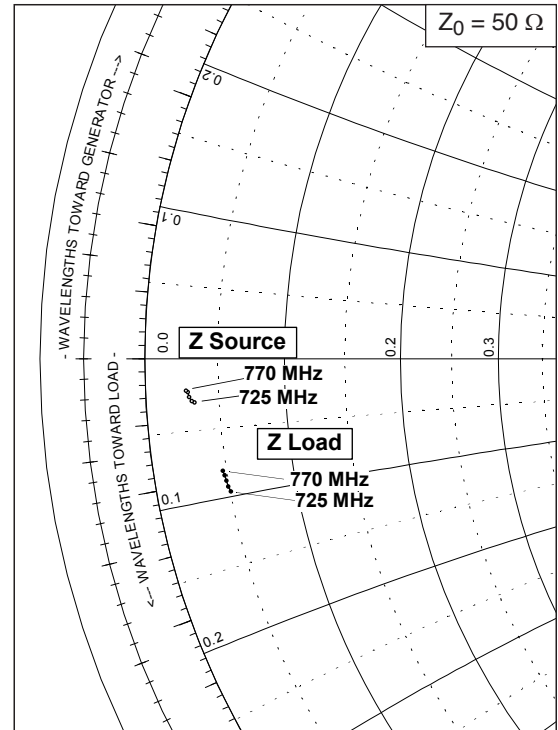
Typical Performance (data taken in a production test fixture)



Broadband Circuit Impedance

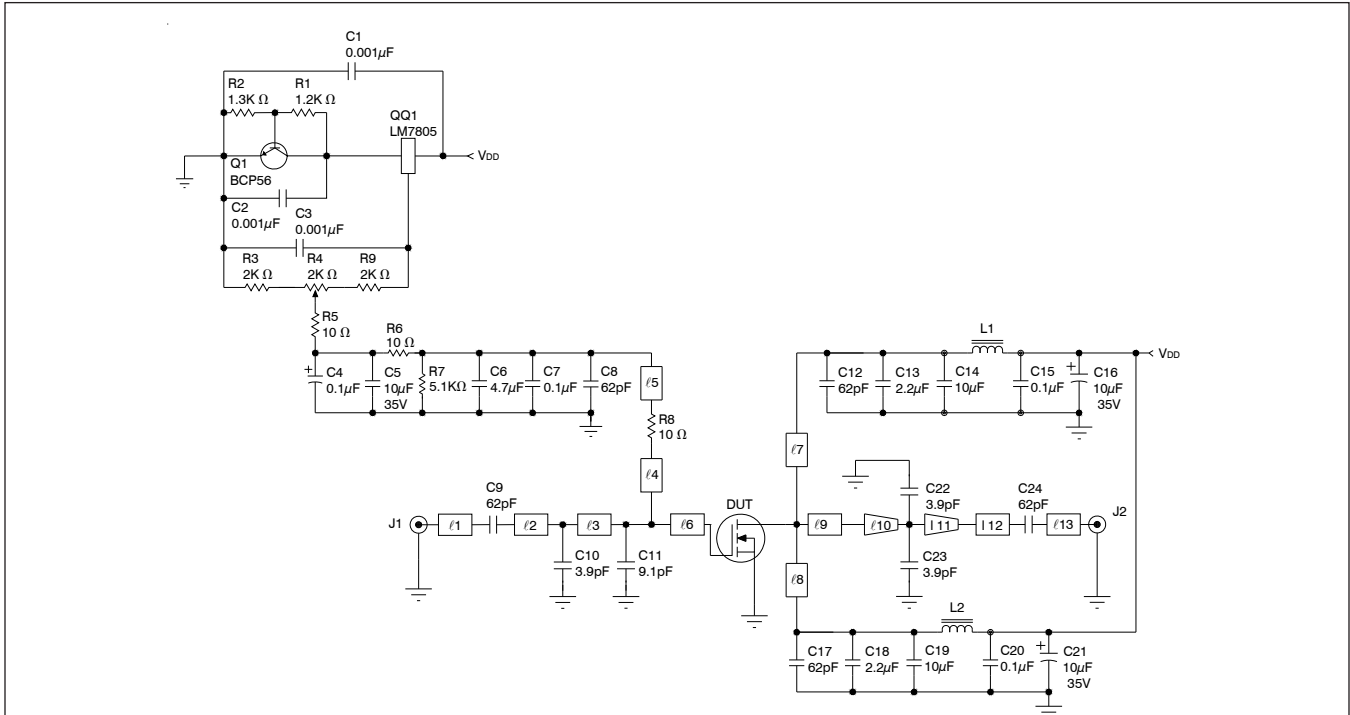


Frequency MHz	Z Source Ω		Z Load Ω	
	R	jX	R	jX
725	2.53	-4.83	1.64	-1.54
736	2.48	-4.64	1.55	-1.48
748	2.44	-4.41	1.46	-1.33
759	2.41	-4.22	1.42	-1.17
770	2.37	-4.04	1.36	-1.11



See next page for reference circuit information

Reference Circuit



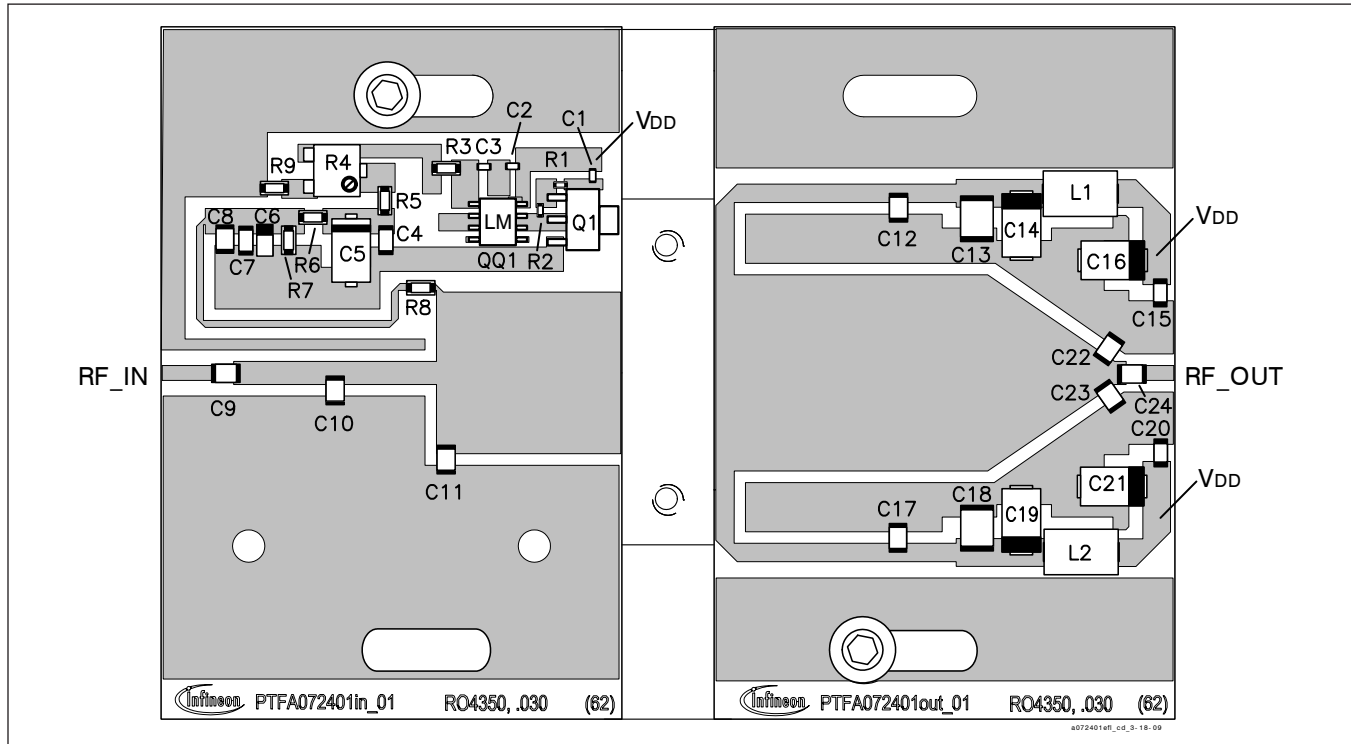
Reference circuit schematic for $f = 770 \text{ MHz}$

Circuit Assembly Information

DUT	PTFA072401EL or PTFA072401FL	LD MOS Transistor
PCB	LTN/PTFA072401E or LTN/PTFA072401F	Rogers RO4350: 0.76 mm [.030"] thick, $\epsilon_r = 3.48$, 1 oz. copper

Microstrip	Electrical Characteristics at 770 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
l1	0.025λ , 50.7 Ω	5.84 x 1.65	0.230 x 0.065
l2, l3	0.048λ , 38.4 Ω	11.18 x 2.54	0.440 x 0.100
l4	0.002λ , 76.8 Ω	0.51 x 0.76	0.020 x 0.030
l5	0.145λ , 76.8 Ω	35.43 x 0.76	1.395 x 0.030
l6	0.094λ , 7.8 Ω	20.32 x 17.78	0.800 x 0.700
l7, l8	0.108λ , 44.5 Ω	25.40 x 2.03	1.000 x 0.080
l9	0.140λ , 6.5 Ω	29.97 x 21.59	1.180 x 0.850
l10 (taper)	0.058λ , 6.5 Ω / 29.4 Ω	13.13 x 21.59 / 3.68	0.517 x 0.850 / 0.145
l11 (taper)	0.004λ , 29.4 Ω / 38.4 Ω	0.84 x 3.68 / 2.54	0.033 x 0.145 / 0.100
l12	0.005λ , 38.4 Ω	1.27 x 2.54	0.050 x 0.100
l13	0.016λ , 50.7 Ω	3.76 x 1.65	0.148 x 0.065

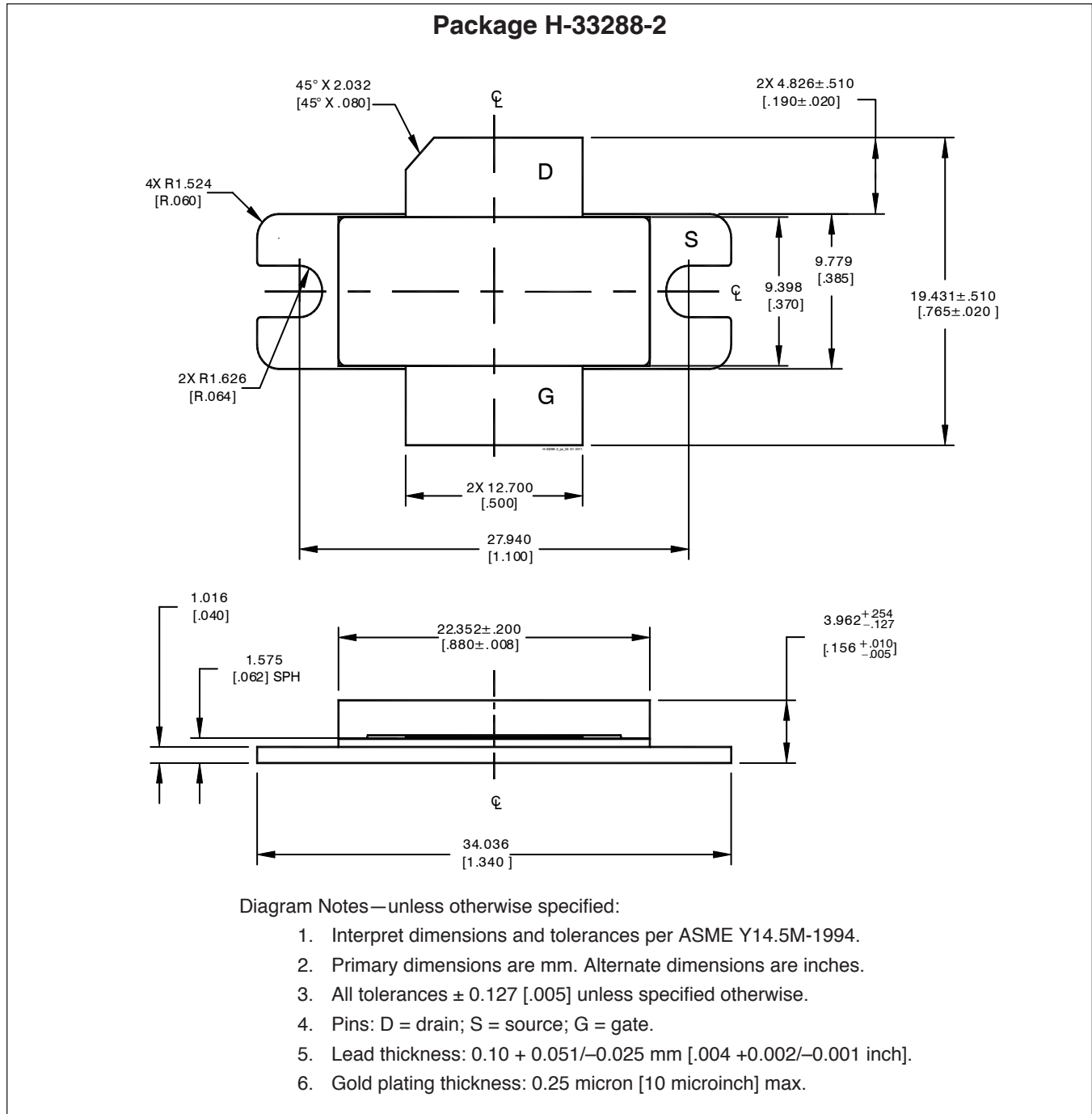
Reference Circuit (cont.)



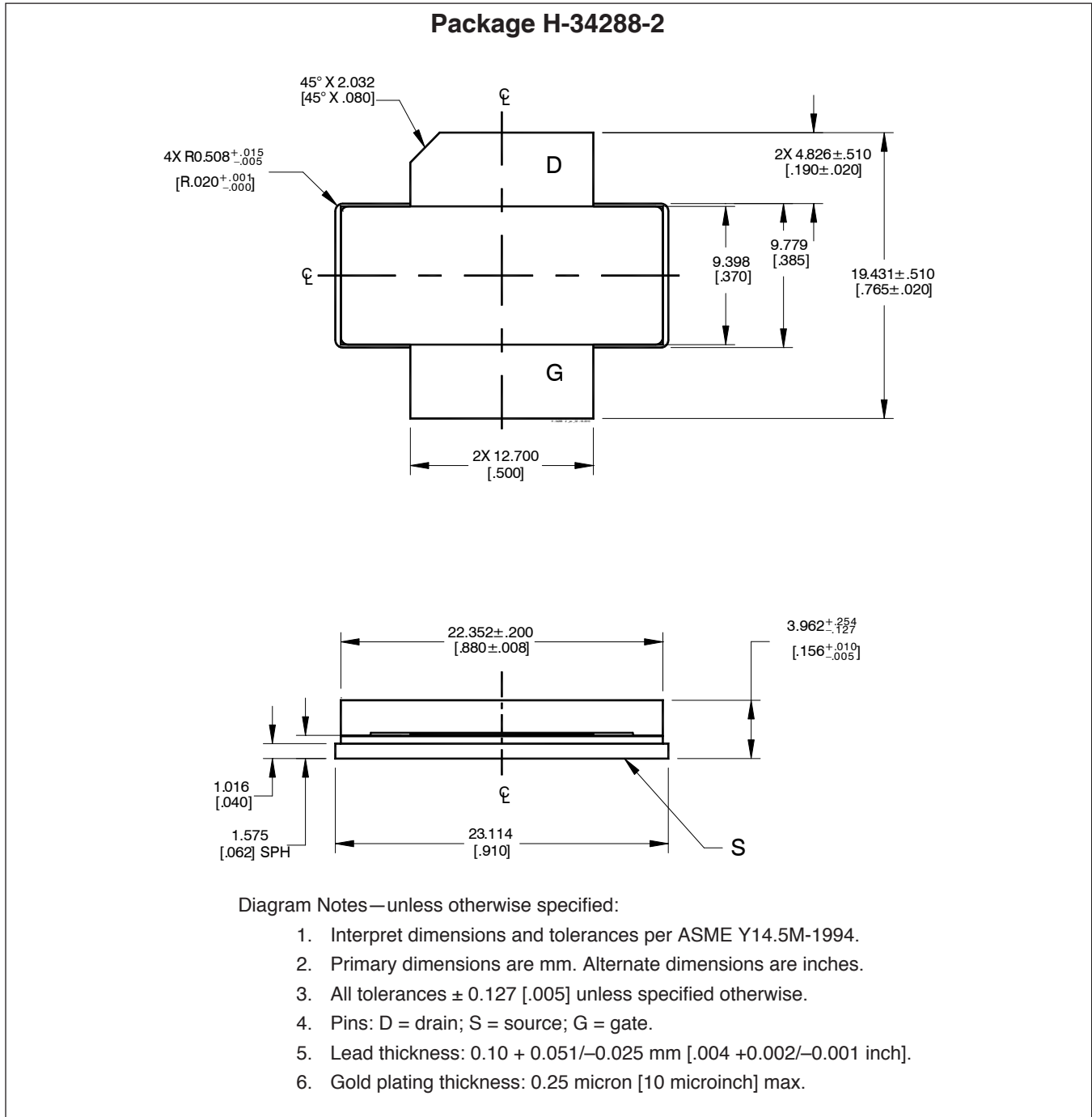
Reference circuit assembly diagram (not to scale)

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 μ F	Digi-Key	PCC1772CT-ND
C4, C7, C15, C20	Capacitor, 0.1 μ F	Digi-Key	PCC104BCT-ND
C5,	Tantalum Capacitor, 10 μ F, 35 V	Digi-Key	399-1655-2-ND
C6	Capacitor, 4.7 μ F, 16 V	Digi-Key	PCS3475CT-ND
C8, C9, C12, C17, C24	Ceramic capacitor, 62 pF	ATC	100B 620
C10, C22, C23	Ceramic capacitor, 3.9 pF	ATC	100B 3R9
C11	Ceramic capacitor, 9.1 pF	ATC	100B 9R1
C13, C18	Capacitor, 2.2 μ F	Digi-Key	445-1447-2-ND
C14, C16, C19, C21	Tantalum Capacitor, 10 μ F, 35 V	Digi-Key	PCS6106TR-ND
L1, L2	Ferrite, 8.9 mm	Digi-Key	240-2511-2-ND
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage Regulator	National Semiconductor	LM7805
R1	Chip resistor, 1.2k Ω	Digi-Key	P1.2KGCT-ND
R2	Chip resistor, 1.3k Ω	Digi-Key	P1.3KGCT-ND
R3, R9	Chip resistor, 2k Ω	Digi-Key	P2KECT-ND
R4	Variable Resistor 2k Ω	Digi-Key	3224W-202ETR-ND
R5, R6, R8	Chip resistor, 10 Ω	Digi-Key	P10ECT-ND
R7	Chip resistor 5.1k Ω	Digi-Key	P5.1KECT-ND

Package Outline Specifications



Package Outline Specifications (cont.)



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Revision History: 2011-04-01 Data Sheet

Previous Version: 2009-03-27, Data Sheet

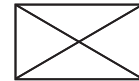
Page	Subjects (major changes since last revision)
1	Updated ESD protection feature
2	Corrected DC Characteristics table
3	Removed CW performance at selected drain voltages graph
4	Removed bias voltage vs. temperature graph

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highpowerRF@infineon.com

To request other information, contact us at:
 +1 877 465 3667 (1-877-GO-LDMOS) USA
 or +1 408 776 0600 International



Edition 2011-04-01

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 Infineon Technologies AG
 81726 Munich, Germany

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