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PTN3356

Flash-based low-power DisplayPort to VGA adapter

Rev. 3 — 13 January 2015 Product data sheet

1. General description

PTN3356 is a flash-based DisplayPort to VGA adapter optimized primarily for motherboard applications, to convert a DisplayPort signal from the chip set to an analog video signal that directly connects to the VGA connector. PTN3356 integrates a DisplayPort receiver, a high-speed triple video digital-to-analog converter that supports a wide range of display resolutions, for example, VGA to WUXGA (see Table 8).

PTN3356 supports two DisplayPort lanes operating at either 2.7 Gbit/s or 1.62 Gbit/s per lane.

PTN3356 supports I^2C-bus over AUX per *DisplayPort standard* (Ref. 1), and bridges the VESA DDC channel to the DisplayPort Interface.

PTN3356 is powered from a 3.3 V power supply and consumes approximately 200 mW of power for video streaming in WUXGA resolution and 410 μW of power in Low-power mode. The VGA output is powered down when there is no valid DisplayPort source data being transmitted. PTN3356 also aids in monitor detection by performing load sensing on RGB lines and reporting sink connection status to the source.

2. Features and benefits

2.1 VESA-compliant DisplayPort converter

- Main Link: 1-lane and 2-lane modes supported
  - HBR (High Bit Rate) at 2.7 Gbit/s per lane
  - RBR (Reduced Bit Rate) at 1.62 Gbit/s per lane
  - BER (Bit Error Rate) better than 10^{-9}
  - DisplayPort Link down-spreading supported
- 1 MHz AUX channel
  - Supports native AUX CH syntax
  - Supports I^2C-bus over AUX CH syntax
- Active HIGH Hot Plug Detect (HPD) signal to the source

2.2 VESA-compliant eDP extensions

- Supports Alternate Scrambler Seed Reset (ASSR)
- Supports Alternate Enhanced Framing mode - Enhanced Framing

2.3 DDC channel output

- I^2C-Over-AUX feature facilitates support of MCCS, DDC/CI, and DDC protocols (see Ref. 2)

2.4 Analog video output

- VSIS 1.2 compliance (Ref. 3) for supported video output modes
- Analog RGB current-source outputs
- 3.3 V VSYNC and HSYNC outputs
- Pixel clock up to 240 MHz
- Triple 8-bit Digital-to-Analog Converter (DAC)
- Direct drive of double terminated 75 Ω load with standard 700 mV (peak-to-peak) signals

2.5 General features

- Monitor presence detection through load detection scheme. Connection/disconnection reported via HPD IRQ and DPCD update.
- Wide set of display resolutions are supported[1]:
  - 1920 × 1440, 60 Hz, 18 bpp, 234 MHz pixel clock rate
  - 2048 × 1152, 60 Hz (reduced blanking), 24 bpp, 162 MHz pixel clock rate
  - 2048 × 1536, 50 Hz (reduced blanking), 24 bpp, 167.2 MHz pixel clock rate
  - WUXGA: 1920 × 1200, 60 Hz, 18 bpp, 193 MHz pixel clock rate
  - WUXGA: 1920 × 1200, 60 Hz (reduced blanking), 24 bpp, 154 MHz pixel clock rate
  - UXGA: 1600 × 1200, 60 Hz, 162 MHz pixel clock rate
  - SXGA: 1280 × 1024, 60 Hz, 108 MHz pixel clock rate
  - XGA: 1024 × 768, 60 Hz, 65 MHz pixel clock rate
  - SVGA: 800 × 600, 60 Hz, 40 MHz pixel clock rate
  - VGA: 640 × 480, 60 Hz, 25 MHz pixel clock rate
  - Any resolution and refresh rates are supported from 25 MHz up to 180 MHz pixel clock rate at 24 bpp, or up to 240 MHz pixel clock rate at 18 bpp
- Bits per color (bpc) supported[1]
  - 6, 8 bits supported
  - 10, 12, 16 bits supported by truncation to 8 MSBs
- All VGA colorimetry formats (RGB) supported
- Power modes (when the application design is as per Figure 4)
  - Active-mode power consumption: ~200 mW at WUXGA, 1920 × 1200, 60 Hz (18 bpc)
  - 410 μW at Low-power mode
- Supports flexible choice of timing reference
  - On-board oscillator with external crystal, ceramic resonator
  - Different frequencies supported: 24 MHz, 25 MHz, 27 MHz
- ESD protection: 7.5 kV HBM
- Single power supply (3.3 V) for easy integration in the platforms
- Commercial temperature range: 0 °C to 85 °C
- 32-pin HVQFN, 5 mm × 5 mm × 0.85 mm (nominal); 0.5 mm pitch; lead-free package

1. Except for color depth beyond 8 bits, display resolutions and refresh rates are only limited to those which a standard 2-lane DisplayPort configuration is able to support over 2.7 Gbit/s per lane of DP Main Link.

3. Applications

- Notebook computers, tablets and desktop PCs
- Dongles, adapters, docking stations

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PTN3356BS/Fx[1]	P3356	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; 5 × 5 × 0.85 mm[2]	SOT617-3

[1] PTN3356BS/Fx uses specific firmware version ('x' = 1, 2, 3, etc., and changes according to firmware version).

[2] Maximum height is 1 mm.

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN3356BS/Fx[1]	PTN3356BS/FxMP	HVQFN32	Reel 13" Q2/T3 *standard mark SMD dry pack	6000	T_{amb} = 0 °C to +85 °C
PTN3356BS/Fx[1]	PTN3356BS/FxZ	HVQFN32	Reel 7" Q2/T3 *standard mark SMD dry pack	500	T_{amb} = 0 °C to +85 °C

[1] PTN3356BS/Fx uses specific firmware version ('x' = 1, 2, 3, etc., and changes according to firmware version).

5. Functional diagram

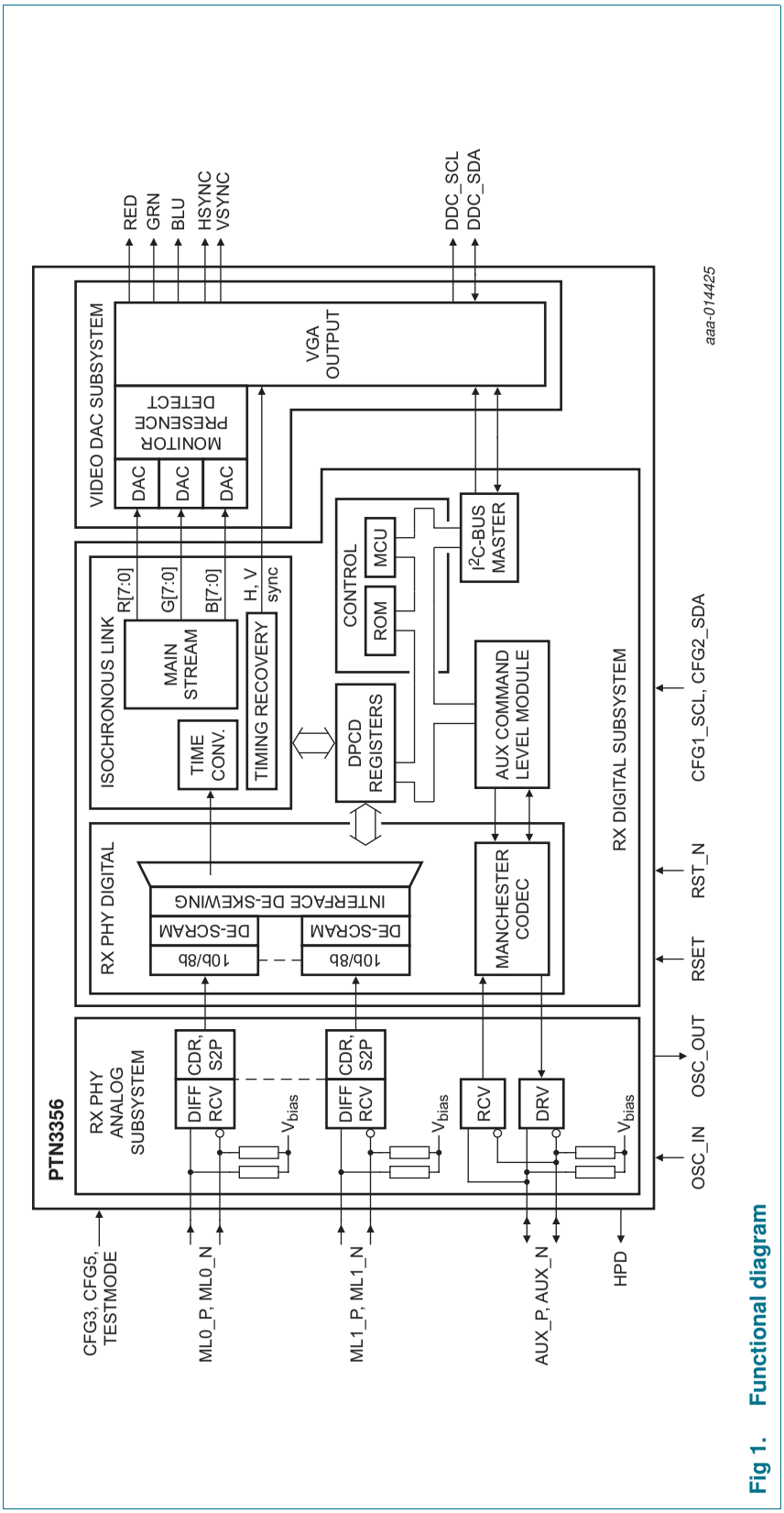
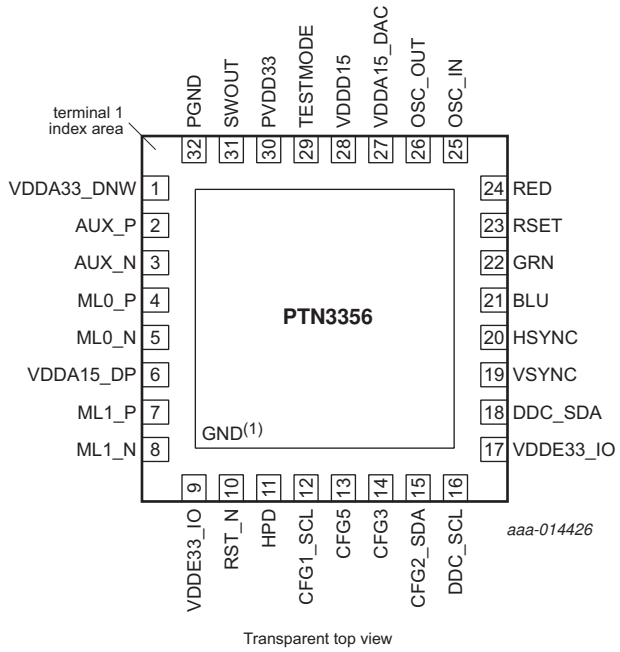


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning



(1) Exposed die pad.

Fig 2. Pin configuration for HVQFN32

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
VDDA33_DNW	1	power	3.3 V power supply
AUX_P	2	self-biasing differential input	DisplayPort AUX channel positive input
AUX_N	3	self-biasing differential input	DisplayPort AUX channel negative input
ML0_P	4	self-biasing differential input	DisplayPort Main Link lane 0 positive input
ML0_N	5	self-biasing differential input	DisplayPort Main Link lane 0 negative input
VDDA15_DP	6	power	1.5 V power supply for DisplayPort PHY; power provided to this pin from SWOUT pin
ML1_P	7	self-biasing differential input	DisplayPort Main Link lane 1 positive input
ML1_N	8	self-biasing differential input	DisplayPort Main Link lane 1 negative input

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
VDDE33_IO	9	power	3.3 V power supply for I/O
RST_N	10	3.3 V digital input	Reset input active LOW; pulled up to $V_{DD(3V3)}$ internally
HPD	11	3.3 V digital I/O	DisplayPort Hot Plug Detection output
CFG1_SCL	12	5 V open-drain I/O	General purpose configuration pin CFG1 or slave I^2C-bus clock
CFG5	13	3.3 V digital I/O	Configuration pin supporting trinary input
CFG3	14	3.3 V digital I/O	Reserved
CFG2_SDA	15	5 V open-drain I/O	General purpose configuration pin CFG2 or slave I^2C-bus data
DDC_SCL	16	5 V open-drain I/O	DDC I^2C-bus clock
VDDE33_IO	17	power	3.3 V power supply for I/O
DDC_SDA	18	5 V open-drain I/O	DDC I^2C-bus data
VSYNC	19	3.3 V 50 Ω digital I/O	Vertical sync
HSYNC	20	3.3 V 50 Ω digital I/O	Horizontal sync
BLU	21	analog output	Blue DAC analog output
GRN	22	analog output	Green DAC analog output
RSET	23	input	Resistor for DAC output reference control
RED	24	analog output	Red DAC analog output
OSC_IN	25	input	Crystal oscillator input
OSC_OUT	26	output	Crystal oscillator output
VDDA15_DAC	27	power	1.5 V power supply for DAC; power provided to this pin from SWOUT pin
VDDD15	28	power	1.5 V power supply for digital core; power provided to this pin from SWOUT pin
TESTMODE	29	input	Test mode selection for CFG/JTAG
PVDD33	30	power	3.3 V power supply for switching regulator
SWOUT	31	power	Switching regulator output
PGND	32	ground	Ground for switching regulator
GND[1]	-	power	central supply ground connection (exposed die pad)

[1] HVQFN32 package die supply ground is connected to exposed center pad. Exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region.

7. Functional description

Referring to Figure 1 “Functional diagram”, the PTN3356 performs protocol conversion from VESA DisplayPort specification to VESA VGA output. At the physical layer, PTN3356 implements the advanced DisplayPort Front-end technology (Auto receive equalization, Clock Data Recovery) to support the objectives of delivering excellent Signal Integrity (SI) performance, and consuming very low power consumption. The PTN3356 integrates a DisplayPort receiver (according to *VESA DisplayPort standard*, Ref. 1) and a high-speed triple 8-bit video digital-to-analog converter that supports a wide range of video resolutions (see Table 8 “Display resolution and pixel clock rate[1]”), up to a pixel clock rate of 240 MHz. The PTN3356 supports one or two DisplayPort Main Link lanes operating at either in 2.7 Gbit/s or 1.62 Gbit/s per lane.

PTN3356 comprises the following functional blocks:

- DP Main Link
- DP AUX CH (Auxiliary Channel)
- DPCD (DisplayPort Configuration Data)
- VGA monitor detection
- Video DAC

The RGB video data with corresponding synchronization references are extracted from the main stream video data. Main stream video attribute information is also extracted. This information is inserted once per video frame during the vertical blanking period by the DP source. The attributes describe the main video stream format in terms of geometry, timing, and color format. The original video clock and video stream are derived from these main link data.

The PTN3356 internal DPCD registers can be accessed by the DP source via the DP AUX channel. The monitor’s DDC control bus may also be controlled via the DP AUX channel. PTN3356 implements the standard DisplayPort I^2C-over-AUX protocol conversion to provide DP source access to the VGA plug DDC-I^2C interface. The PTN3356 passes through sink-side status change (for example, hot-plug events) to the source side, through HPD interrupts and DPCD registers.

7.1 DisplayPort Main Link

The DisplayPort main link consists of two AC-coupled differential pairs. The 50 Ω termination resistors are integrated inside PTN3356.

The PTN3356 supports HBR at 2.7 Gbit/s and RBR at 1.62 Gbit/s per lane.

7.2 DisplayPort auxiliary channel (AUX CH)

The AUX CH is a half-duplex, bidirectional channel between DisplayPort source and sink. It consists of one differential pair transporting self-clocked data at 1 Mbit/s. The PTN3356 integrates the AUX CH replier (or slave), and responds to transactions initiated by the DisplayPort source AUX CH requester (or master).

The AUX CH uses the Manchester-II code for the self-clocked transmission of signals; every ‘zero’ is represented by LOW-to-HIGH transition, and ‘one’ represented by HIGH-to-LOW transition, in the middle of the bit time.

7.3 DPCD registers

DPCD registers that are part of the VESA DisplayPort standard are described in detail in Ref. 1. The following describes the specific implementation by PTN3356 only.

PTN3356 DisplayPort receiver capability and status information about the link are reported by DisplayPort Configuration Data (DPCD) registers, when a DP source issues a read command on the AUX CH. The DP source device can also write to the link configuration field of DPCD to configure and initialize the link. The DPCD is DisplayPort v1.2a compliant.

PTN3356 specific capabilities are made available to DP source in the relevant DPCD read/write registers. In line with the DisplayPort standard (Ref. 1), the specific Link controls are also made available to initialize and maintain the DisplayPort Link.

It is the responsibility of the DP source to issue commands only within the capability of the PTN3356 as defined in the 'Receiver Capability Field' in order to prevent undefined behavior. PTN3356 specific DPCD registers are listed in Table 4.

7.3.1 PTN3356 specific DPCD register settings

Table 4. PTN3356 specific DPCD registers

DPCD register [1]	Description	Power-on Reset value	Read/write over AUX CH
Receiver Capability Field			
0000Ch	I^2C-bus speed control capabilities bit map. Speed control is not supported through DPCD register. Default speed of 50 kbit/s is supported.	00h	read only
0000Dh	eDP_CONFIGURATION_CAP. Bit 0 = ALTERNATE_SCRAMBLER_RESET_CAPABLE. A setting of 1 indicates that this is an eDP device that can use the eDP alternate scrambler reset value of FFFFh. Bit 1 = FRAMING_CHANGE_CAPABLE. A setting of 1 indicates that this is an eDP device that uses only Enhanced Framing independently of the setting by the source of ENHANCED_FRAME_EN. Bit 2 = reserved for eDP. Read 0. Bit 3 = DPCD_DISPLAY_CONTROL_CAPABLE. A setting of 1 indicates that display control registers starting at address 00700h are enabled. Bits 7:4 = reserved for eDP. Read all zeros.	03h	read only
Link Configuration Field			
00109h	I^2C-bus speed control capabilities bit map. Speed control is not supported and the default speed of 50 kbit/s is supported. Writes are ignored and reads would get zeros.	00h	read/write

Table 4. PTN3356 specific DPCD registers *…continued*

DPCD register [1]	Description	Power-on Reset value	Read/write over AUX CH
0010Ah	Bit 0 = ALTERNATE_SCRAMBLER_RESET_ENABLE. Source sets to 1 to select the alternate scrambler reset. Writes ignored if ALTERNATE_SCRAMBLER_RESET_CAPABLE = 0. Power-on default value = 0. Bit 1 = FRAMING_CHANGE_ENABLE. Source sets to 1 to select the framing change. Writes ignored if FRAMING_CHANGE_CAPABLE = 0. Power-on default value = 0. Bits 6:2 = reserved. Read all zeros. Bit 7 = PANEL_SELF_TEST_ENABLE (not supported in PTN3356).	00h	read/write
Branch device specific field			
00500h	BRANCH_IEEE_OUI 7:0 Branch vendor 24-bit IEEE OUI. NXP OUI = 00	00h	read only
00501h	BRANCH_IEEE_OUI 15:8 NXP OUI = 60	60h	read only
00502h	BRANCH_IEEE_OUI 23:16 NXP OUI = 37	37h	read only
00503h	ID string = 3356N2	33h	read only
00504h		33h	read only
00505h		35h	read only
00506h		36h	read only
00507h		4Eh	read only
00508h		32h	read only
00509h	Hardware revision level v1.0	10h	read only
0050Ah	Firmware/software major revision level	01h	read only
0050Bh	Firmware/software minor revision level	02h	read only
0050Ch to 005FFh	RESERVED		read only

[1] Byte fields that are not explicitly listed are by definition reserved ('RES') and their default value is 0h.

7.4 VGA monitor detection

The PTN3356 implements a robust scheme for VGA monitor detection. It senses presence or absence of VGA monitor load termination (75 Ω) by pulsing the RGB lines. The load sensing operation is performed periodically to determine the latest VGA connectivity status. If the VGA monitor is disconnected, then the detection logic informs the host platform via IRQ_HPD signal.

7.5 EDID handling

Figure 3 shows a DisplayPort-to-analog video converter between the DisplayPort source and a VGA monitor. The PTN3356 implements a DP I^2C-Over-AUX protocol, providing for DP source access to the monitor's DDC bus. With this, the monitor's EDID data is made available to DP source for access at any time.

It is the responsibility of the source to choose only video modes which are declared in the EDID and to adjust the DisplayPort link capabilities (link rate and lane count) to provide the necessary video bandwidth. The PTN3356 does not cache or modify the EDID to match the capabilities of the DisplayPort link data.

If the DisplayPort source drives display modes that are not specified in the EDID mode list, the PTN3356 does not detect such conditions, and it depends entirely on the VGA display on what is being displayed.

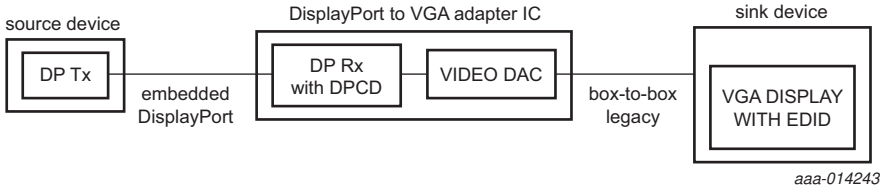


Fig 3. DisplayPort to VGA adapter IC sits between the DisplayPort source and a VGA monitor with EDID

7.6 Triple 8-bit video DACs and VGA outputs

The triple 8-bit video DACs output a 700 mV (peak-to-peak) analog video output signal into 37.5 Ω load, as is the case of a doubly terminated 75 Ω cable. The DAC is capable of supporting the maximum pixel rate supported by a two-lane DP link (240 MHz).

7.6.1 DAC reference resistor

An external reference resistor must be connected between pin RSET and ground. This resistor sets the reference current which determines the analog output level, and is specified as 1.2 kΩ with a 1 % tolerance. This value allows a 0.7 V (peak-to-peak) output into a 37.5 Ω load (for example, double-terminated 75 Ω coaxial cable).

8. Power-up and reset

PTN3356 has built-in power-on reset circuitry which automatically sequences the part through reset and initialization. In addition, there is a dedicated pin (RST_N) to control/effect reset operation externally. This provides flexibility at the platform level for debug or application purpose.

Before link is established, the PTN3356 holds VSYNC and HSYNC signals LOW and blanks the RGB signals.

While the PTN3356 performs power-on initialization,

- The HPD signal is driven LOW, to indicate to the DisplayPort source that the PTN3356 is not ready for AUX channel communication. Once the device is initialized, the HPD level is produced based on CFG1_SCL/CFG2_SDA setting
- The RGB outputs are disabled
- The VSYNC and HSYNC outputs are maintained LOW as long as there is no active video streaming from the DisplayPort source.

9. Configurability and programmability

The PTN3356 delivers flexibility for application usage by providing configurability via two options:

- Configuration pins CFG1_SCL, CFG2_SDA, CFG5, and TESTMODE
- DP-AUX vendor-specific configuration registers

The pins provide limited application board level configurability, whereas vendor-specific configuration registers deliver ultimate flexibility. The configuration pin changes (static, dynamic) are reflected in the IC behavior.

The configuration pin definitions are as follows:

- CFG1_SCL, CFG2_SDA are used for either host I^2C-bus communication or as dedicated configuration pins with binary leveled I/O. PTN3356 is flexible enough to accept either. The use of these configuration pins is defined in Table 7.
- Configuration pin CFG5 selects OSC_IN clock frequency setting. Table 5 captures the pin definition.
- CFG3 is reserved. It is not defined yet.

Table 5. CFG5 pin definition

Configuration input	OSC_IN clock frequency setting
HIGH	24 MHz
LOW	25 MHz
OPEN	27 MHz

The TESTMODE pin is used to indicate selection of JTAG or configuration for CFG1_SCL, CFG2_SDA and CFG5. Table 6 defines the possible combinations of TESTMODE pin.

Table 6. TESTMODE pin definition

Pin value	Mode selection
LOW	Configuration pin functionality is selected; I²C address for CFG1_SCL, CFG2_SDA is 40h.
OPEN	Configuration pin functionality is selected; I²C address for CFG1_SCL, CFG2_SDA is C0h.
HIGH	JTAG functionality is selected.

CFG1_SCL, CFG2_SDA can be used in I²C mode or configuration pin mode. PTN3356 automatically detects the mode in which these pins are used. If they are used as Configuration pins, Table 7 determines the possible and allowed combinations for these pin settings. If they are used as I²C Clock/Data pins, PTN3356 detects toggling of the pins during I²C-bus data transport and receives data properly.

Table 7. CFG1_SCL/CFG2_SDA pin definitions

Pin value	System behavior
00	Compliant HPD behavior
01	Most interoperable (non-compliant) HPD behavior
10	Most interoperable (non-compliant) HPD behavior
11	(Default) Compliant behavior (but configurable via I²C-bus)

More configuration options are available through internal configuration registers. These registers can be accessed by GPU/CPU software driver via DP AUX channel or I²C-bus.

NXP can deliver Windows and DOS based utilities, on explicit request, to upgrade the firmware or configuration registers only for laboratory evaluation and debugging purposes at customer premises.

10. Application design-in information

With its maximum integration features, the PTN3356 has low BOM requirement at the platform application level. Figure 4 illustrates the PTN3356 usage in a system application context. On the DP side, it is connected to DP source and the VGA side, it is connected to VGA connector. The PTN3356 system application requires the following components additionally: supply decoupling capacitors, DC blocking capacitors, pull-up/down resistors, (optional) inductor for DC-to-DC converter, crystal oscillator. For more details on reference design information, contact NXP team.

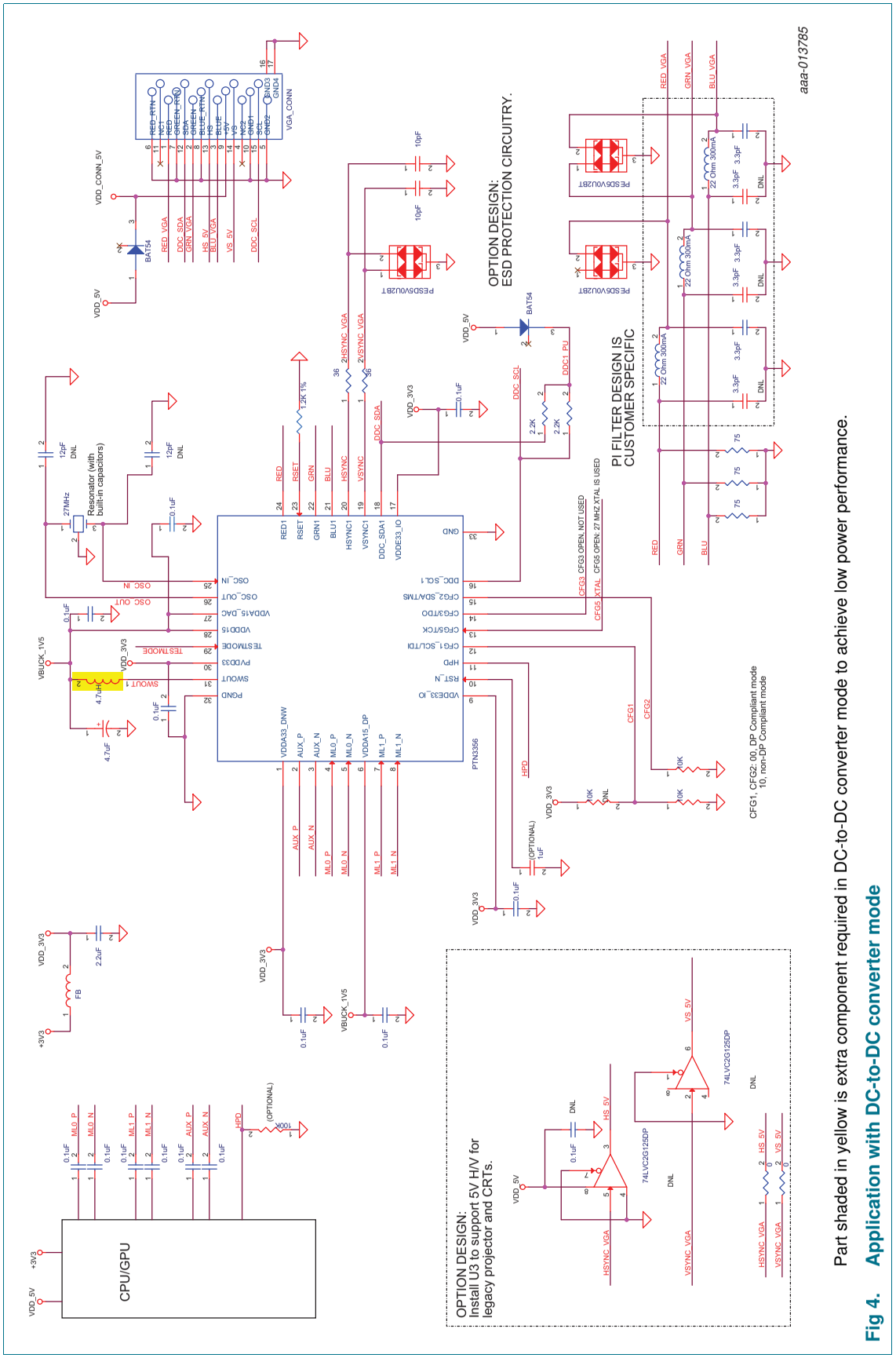


Fig 4. Application with DC-to-DC converter mode

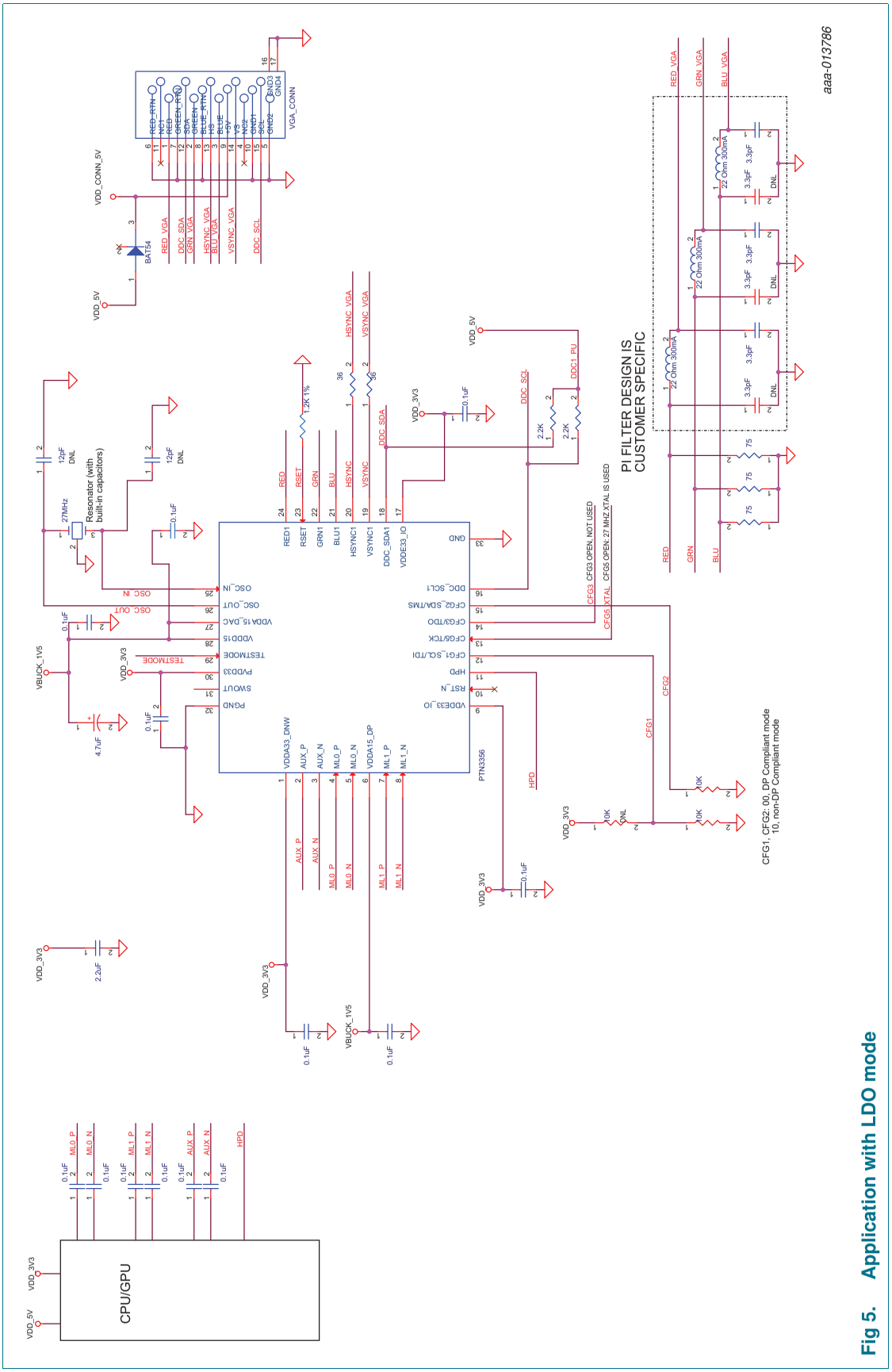


Fig 5. Application with LDO mode

10.1 Display resolution

Table 8 lists some example display resolutions and clock rates that PTN3356 supports. (Refer to Footnote 1 on page 2.)

Table 8. Display resolution and pixel clock rate[1]

Display type	Active video		Total frame		Bits per pixel	Vertical frequency (Hz)	Pixel clock (MHz)	Data rate (Gbit/s)	Standard type
	Horizontal	Vertical	Horizontal total (pixel)	Vertical total (line)					
VGA	640	480	800	525	24	59.94	25.175	0.76	Industry standard
SVGA	800	600	1056	628	24	60.317	40.000	1.20	VESA guidelines
XGA	1024	768	1344	806	24	60.004	65.000	1.95	VESA guidelines
XGA+	1152	864	1600	900	24	75	108.000	3.24	VESA standard
HD	1360	768	1792	795	24	60.015	85.500	2.56	VESA standard
HD/WXGA	1366	768	1792	798	24	59.79	85.501	2.57	VESA standard
HD/WXGA	1280	720	1650	750	24	60	74.250	2.23	CEA standard
WXGA	1280	800	1680	831	24	59.81	83.500	2.50	CVT
WXGA	1280	800	1696	838	24	74.934	106.500	3.19	CVT
WXGA	1280	800	1712	843	24	84.88	122.500	3.68	CVT
SXGA–	1280	960	1800	1000	24	60	108.000	3.24	VESA standard
SXGA	1280	1024	1688	1066	24	60.02	108.000	3.24	VESA standard
SXGA	1280	1024	1688	1066	24	75.025	135.001	4.05	VESA standard
SXGA	1280	1024	1728	1072	24	85.024	157.500	4.72	VESA standard
SXGA+	1400	1050	1864	1089	24	59.978	121.749	3.65	CVT
WXGA+	1440	900	1904	934	24	59.887	106.499	3.19	CVT
HD+	1600	900	1800	1000	24	60 (RB)	108.000	3.24	VESA standard
UXGA	1600	1200	2160	1250	24	60	162.000	4.86	VESA standard
UXGA	1600	1200	2160	1250	24	65	175.500	5.27	VESA standard
WSXGA+	1680	1050	2240	1089	24	59.954	146.249	4.39	CVT
FHD	1920	1080	2200	1125	24	60	148.500	4.46	CEA standard
WUXGA	1920	1200	2592	1245	18	59.885	193.251	4.35	CVT
WUXGA	1920	1200	2080	1235	24	59.95 (RB)	154.000	4.62	CVT RB
2.76M3	1920	1440	2600	1500	18	60	234.000	5.27	VESA standard
QWXGA	2048	1152	2250	1200	24	60 (RB)	162.000	4.86	CVT RB
QXGA	2048	1536	2128	1573	24	49.95 (RB)	167.20	5.02	CVT RB

[1] Contact NXP team for other monitor timings not listed in this table.

The available bandwidth over a 2-lane HBR DisplayPort v1.2a link limits pixel clock rate support to:

- 240 MHz at 6 bpc
- 180 MHz at 8 bpc

10.2 Power supply filter

Sufficient decoupling capacitance to ground should be connected from each V_{DD} pin directly to ground to filter supply noise.

10.3 DAC terminations

Typically, the VGA RGB outputs are (doubly) terminated. Figure 6 shows an example VGA application. A 75 Ω termination is used to terminate inside the motherboard, and another 75 Ω termination is typically used inside the RGB monitor. The load sensing mechanism assumes this double termination. Figure 7 is another example of VGA application with 50 Ω PCB trace impedance with 150 Ω terminations.

In general, it is left to the system integrator to decide on their specific implementation.

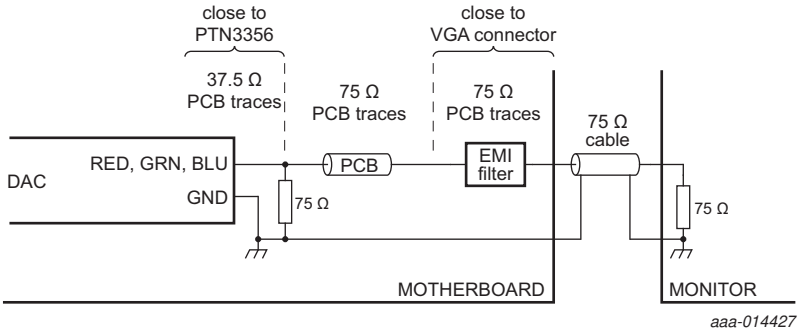


Fig 6. PTN3356 DAC termination example 1

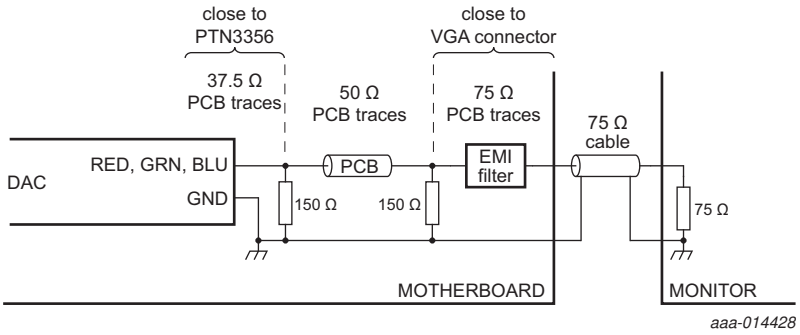


Fig 7. PTN3356 DAC termination example 2

10.4 Timing reference

PTN3356 requires a crystal or ceramic resonator for a stable VGA clock timing reference. Resonators have a higher frequency tolerance than crystals, but have the advantage of integrated capacitors and therefore a small PCB area and potentially lower cost.

Table 9. Required crystal specifications (SMD components)

Crystal parameters	Specifications
Frequency	24 MHz, 25 MHz or 27 MHz
Operation mode	Fundamental
Frequency tolerance	±1 % maximum
Frequency stability over temperature	±0.4 % maximum
Load capacitance (C_L)	18 pF
Shunt capacitance	< 2 pF
Equivalent Series Resistance (ESR)	< 150 Ω

11. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)			−0.3	+4.6	V
V_I	input voltage	3.3 V CMOS inputs		−0.3	$V_{DD(3V3)}$ + 0.5	V
T_{stg}	storage temperature			−65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	7500	V
		CDM	[2]	-	1000	V

[1] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[2] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

12. Recommended operating conditions

Table 11. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)			2.8	3.3	3.6	V
t_r	rise time	supply voltage		-	-	10	ms
V_I	input voltage	3.3 V CMOS inputs		0	3.3	3.6	V
		SDA and SCL inputs with respect to ground		0	5	5.5	V
$R_{ext(RSET)}$	external resistance on pin RSET	between RSET (pin 21) and GND		-	1.20 ± 1 %	-	kΩ
T_{amb}	ambient temperature	commercial grade		0	-	85	°C

13. Characteristics

13.1 Current consumption, power dissipation and thermal characteristics

Table 12. Current consumption, power dissipation and thermal characteristics

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD}	supply current	normal operation, WUXGA / 193 MHz pixel clock; $V_{DD(3V3)}$ = 3.3 V		-	60	-	mA
		Low power D3 mode; $V_{DD(3V3)}$ = 3.3 V		-	124	-	µA
P	power dissipation	normal operation, WUXGA / 193 MHz pixel clock (reduced blanking)					
		Buck converter mode; PTN3356 being used as per Figure 4		-	200	-	mW
		LDO mode; PTN3356 being used as per Figure 5		-	405	-	mW
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air for SOT617-3		-	45	-	K/W

Table 13. Device characteristics

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{startup}$	start-up time	device start-up time from power-on to HPD = HIGH; VGA monitor remains connected at power-on[1]; RST_N = HIGH; supply voltage within operating range to specified operating characteristics		-	-	100	ms
$t_{w(rst)}$	reset pulse width	device is supplied with valid supply voltage		10	-	-	µs
$t_{d(rst)}$	reset delay time	device reset delay time from RST_N toggling (LOW to HIGH) until HPD goes HIGH; VGA monitor remains connected at power-on[1]; supply voltage within operating range to specified operating characteristics		-	-	100	ms

[1] VGA monitor remains connected at power-on — this condition is applicable only when PTN3356 is used in most interoperable (non-compliant) HPD mode (that is, CFG1_SCL/CFG2_SDA is ‘01’ or ‘10’).

13.2 DisplayPort receiver main link

Table 14. DisplayPort receiver main link characteristics[1]

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UI	unit interval	for high bit rate (2.7 Gbit/s per lane)		-	370	-	ps
		for low bit rate (1.62 Gbit/s per lane)		-	617	-	ps
Δf_{DOWN_SPREAD}	link clock down spreading		[2]	0.0	-	0.5	%
$V_{RX\_DIFFp\text{-}p}$	differential input peak-to-peak voltage	at RX package pins					
		for high bit rate	[3]	120	-	-	mV
		for reduced bit rate	[3]	40	-	-	mV
$V_{RX\_DC\_CM}$	RX DC common mode voltage		[4]	0	-	2.0	V
I_{RX_SHORT}	RX short-circuit current limit		[5]	-	-	50	mA
C_{RX}	AC coupling capacitor	on DP Main Link and AUX inputs		75	-	200	nF
$f_{RX\_TRACK\_BW\_HBR}$	jitter closed loop tracking bandwidth (High Bit Rate)		[6]	10	-	20	MHz
$f_{RX\_TRACK\_BW\_RBR}$	jitter closed loop tracking bandwidth (Reduced Bit Rate)		[6]	5.4	-	20	MHz

[1] Ref. 1 supersedes in case of any mismatch of specification items.

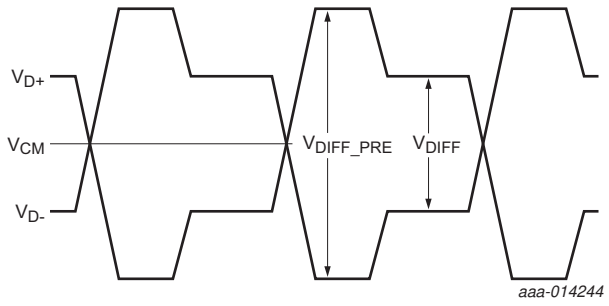
[2] Up to 0.5 % down spread is supported. Modulation frequency range of 30 kHz to 33 kHz must be supported.

[3] Informative; refer to Figure 8 for definition of differential voltage.

[4] Common mode voltage is equal to V_{bias_RX} voltage.

[5] Total drive current of the input bias circuit when it is shorted to its ground.

[6] The measurements are always taken with PRBS7 test signal. Minimum CDR closed loop tracking bandwidth at the receiver when the input is a PRBS7 pattern.



pre-emphasis = $20\text{Log}(V_{DIFF\_PRE} / V_{DIFF})$

Fig 8. Definitions of pre-emphasis and differential voltage

13.3 DisplayPort receiver AUX CH

Table 15. DisplayPort receiver AUX CH characteristics[1]

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UI	unit interval	AUX	[2]	0.4	0.5	0.6	μs
$t_{jit(cc)}$	cycle-to-cycle jitter time	transmitting device	[3]	-	-	0.04	UI
		receiving device	[4]	-	-	0.05	UI
$V_{AUX\_DIFFp-p}$	AUX differential peak-to-peak voltage	transmitting device	[5]	0.39	-	1.38	V
		receiving device	[5]	0.32	-	1.36	V
$R_{AUX\_TERM(DC)}$	AUX CH termination DC resistance	informative		-	100	-	Ω
$V_{AUX\_DC\_CM}$	AUX DC common-mode voltage		[6]	0	-	2.0	V
$V_{AUX\_TURN\_CM}$	AUX turnaround common-mode voltage		[7]	-	-	0.3	V
I_{AUX_SHORT}	AUX short-circuit current limit		[8]	-	-	90	mA
C_{AUX}	AUX AC coupling capacitor		[9]	75	-	200	nF

[1] Ref. 1 supersedes in case of any mismatch of specification items.

[2] Results in the bit rate of 1 Mbit/s including the overhead of Manchester II coding.

[3] Maximum allowable UI variation within a single transaction at connector pins of a transmitting device. Equal to 24 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.

[4] Maximum allowable UI variation within a single transaction at connector pins of a receiving device. Equal to 30 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.

[5] $V_{AUX\_DIFFp-p} = 2 \times |V_{AUX+} - V_{AUX-}|$.

[6] Common-mode voltage is equal to V_{bias_TX} (or V_{bias_RX}) voltage.

[7] Steady-state common-mode voltage shift between transmit and receive modes of operation.

[8] Total drive current of the transmitter when it is shorted to its ground.

[9] The AUX CH AC coupling capacitor placed both on the DisplayPort source and sink devices.

13.4 HPD characteristics

Table 16. HPD characteristics[1]

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output characteristics							
V_{OH}	HIGH-level output voltage	I_{OH} = 2 mA		2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −2 mA		-	-	0.4	V
I_{OSH}	HIGH-level short-circuit output current	drive HIGH; cell connected to ground		-	-	16	mA
I_{OSL}	LOW-level short-circuit output current	drive LOW; cell connected to V_{DD}		-	-	15	mA

[1] Ref. 1 supersedes in case of any mismatch of specification items.

13.5 DDC/I²C characteristics

Table 17. DDC/I²C characteristics

V_{CC} = 4.5 V to 5.5 V[1]. Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input characteristics							
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(3V3)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	+0.3 × $V_{DD(3V3)}$	V
$V_{I(hys)}$	hysteresis of input voltage			0.1 × $V_{DD(3V3)}$	-	-	V
I_{LI}	input leakage current	V_I = 5 V		-	-	10	μA
Output characteristics							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3.0	-	-	mA
$I_{O(sc)}$	short-circuit output current	drive LOW; cell connected to $V_{DD(3V3)}$		-	-	40.0	mA
C_{io}	input/output capacitance	V_I = 3 V or 0 V					
		$V_{DD(3V3)}$ = 3.3 V		-	6	7	pF
		$V_{DD(3V3)}$ = 0 V		-	6	7	pF

[1] V_{CC} is the pull-up voltage for DDC/I²C.

[2] Table 17 applies to CFG1_SCL and CFG2_SDA pins as they operate as I²C-bus I/O.

13.6 DAC

Table 18. DAC characteristics

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$N_{res(DAC)}$	DAC resolution			-	-	8	bit
f_{clk}	clock frequency			-	-	240	MHz
$\Delta I_{o(DAC)}$	DAC output current variation	DAC-to-DAC		-	-	4	%
INL	integral non-linearity			−1	±0.25	+1	LSB
DNL	differential non-linearity			−0.5	±0.1	+0.5	LSB
$V_{o(DAC)max}$	maximum DAC output voltage			665	700	770	mV
$C_{o(DAC)}$	DAC output capacitance			-	3.5	-	pF
	DAC noise injection ratio			−1.5	-	+1.5	%

13.7 HSYNC, VSYNC characteristics

Table 19. HSYNC and VSYNC characteristics

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output characteristics							
V_{OH}	HIGH-level output voltage	I_{OH} = 8 mA; $V_{DD(3V3)}$ = 3.3 V ± 10 %		2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −8 mA		-	-	0.5	V
I_{OSH}	HIGH-level short-circuit output current	drive HIGH; cell connected to ground	[1]	-	-	100	mA
I_{OSL}	LOW-level short-circuit output current	drive LOW; cell connected to V_{DD}	[1]	-	-	100	mA

[1] The parameter values specified are simulated and absolute values.

13.8 Configuration pins CFG3, CFG5, TESTMODE

Table 20. Configuration pins characteristics

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input characteristics							
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage					0.3 × $V_{DD(3V3)}$	V
Weak pull-down characteristics							
I_{pd}	pull-down current	V_I = $V_{DD(3V3)}$		15	30	70	µA
I_{pu}	pull-up current	V_I = 0 V		25	55	90	µA
R_{ext}	external resistance	external resistor used on configuration pins		-	-	10	kΩ

13.9 RST_N

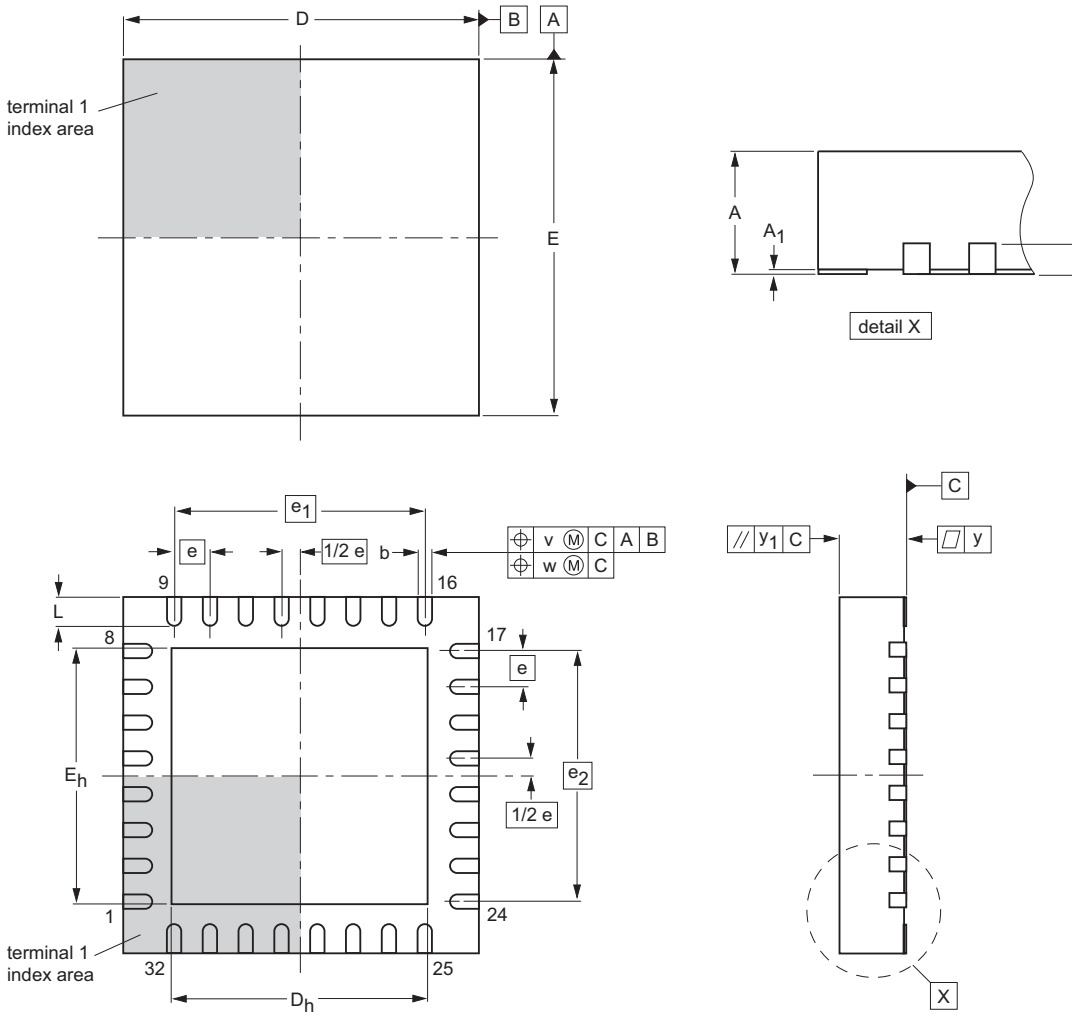
Table 21. RST_N characteristics

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input characteristics							
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3 \times V_{DD(3V3)}$	V
$I_{pu(RST\_N)}$	pull-up current on pin RST_N	V_I = 0 V		25	55	90	µA

14. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit(1)		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Fig 9. Package outline SOT617-3 (HVQFN32)