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PTN3366

Low power HDMI/DVI level shifter with active DDC buffer, supporting 3 Gbit/s operation

Rev. 1.1 — 22 May 2015 Product data sheet

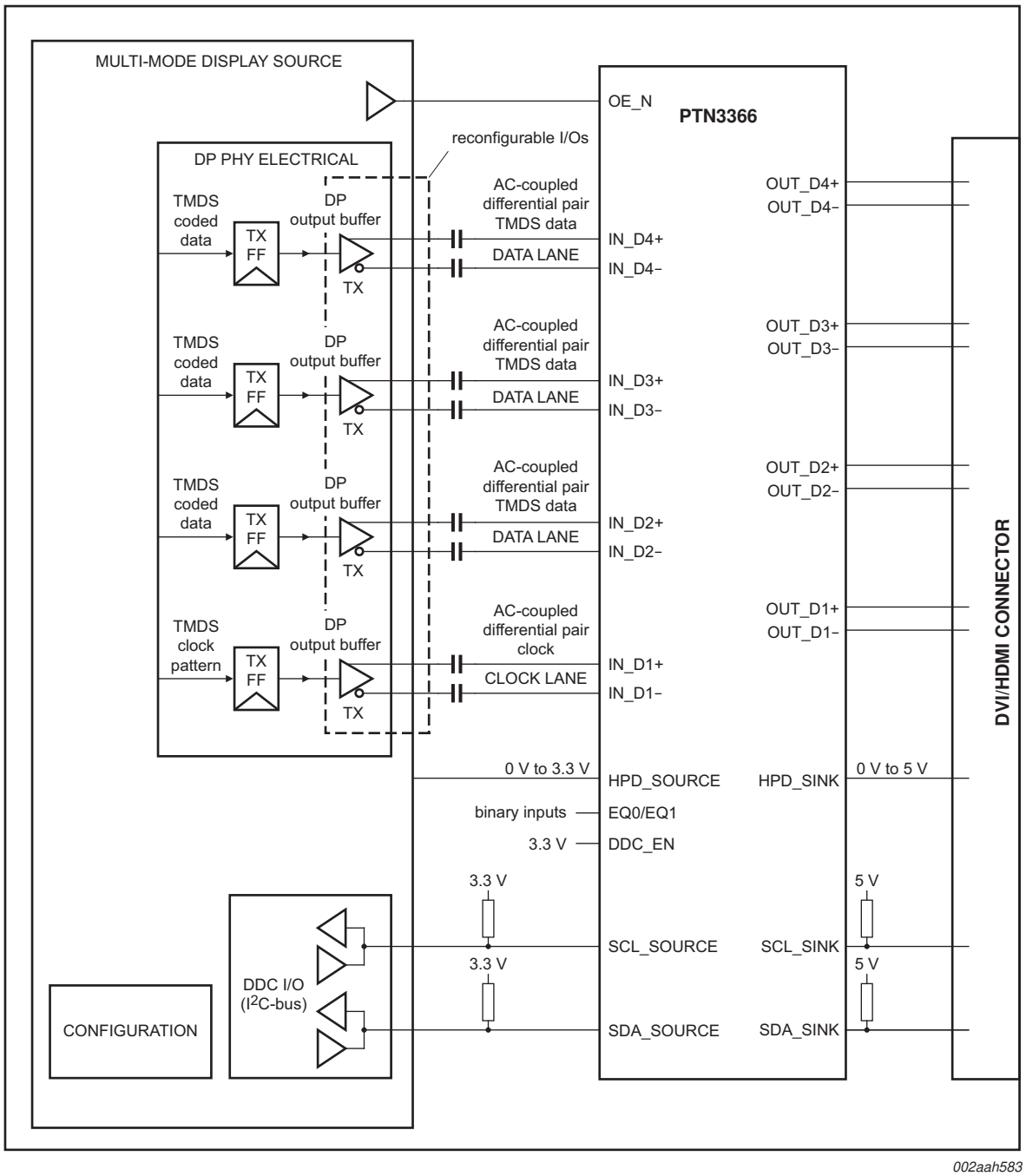
1. General description

PTN3366 is a low power, high-speed level shifter device which converts four lanes of low-swing AC-coupled differential input signals to DVI v1.0 and HDMI v1.4b compliant open-drain current-steering differential output signals, up to 3 Gbit/s per lane to support 36-bit deep color mode, 4K × 2K video format or 3D video data transport. Each of these lanes provides a level-shifting differential active buffer, with built-in Equalization, to translate from low-swing AC-coupled differential signaling on the source side, to TMDS-type DC-coupled differential current-mode signaling terminated into 50 Ω to 3.3 V on the sink side. Additionally, the PTN3366 provides a single-ended active buffer for voltage translation of the HPD signal from 5 V on the sink side to 3.3 V on the source side and provides a channel with active buffering and level shifting of the DDC channel (consisting of a clock and a data line) between 3.3 V source-side and 5 V sink-side. The DDC channel is implemented using active I^2C-bus buffer technology providing redriving and level shifting as well as disablement (isolation between source and sink) of the clock and data lines.

The low-swing AC-coupled differential input signals to the PTN3366 typically come from a display source with multi-mode I/O, which supports multiple display standards, for example, DisplayPort, HDMI and DVI. While the input differential signals are configured to carry DVI or HDMI coded data, they do not comply with the electrical requirements of the DVI v1.0 or HDMI v1.4b specification. By using PTN3366, chip set vendors are able to implement such reconfigurable I/Os on multi-mode display source devices, allowing the support of multiple display standards while keeping the number of chip set I/O pins low. See Figure 1.

The PTN3366 main high-speed differential lanes feature low-swing self-biasing differential inputs which are compliant to the electrical specifications of *DisplayPort Standard v1.2a* and/or *PCI Express Standard v1.1*, and open-drain current-steering differential outputs compliant to DVI v1.0 and HDMI v1.4b electrical specifications. The I^2C-bus channel actively buffers as well as level-translates the DDC signals. The PTN3366 supports standby mode in order to minimize current consumption when Hot Plug Detect signal HPD_SINK is LOW.

PTN3366 is powered from a single 3.3 V power supply consuming a small amount of power (72 mW typical) and is offered in a 32-terminal HVQFN32 package.



Remark: TMDS clock and data lanes can be assigned arbitrarily and interchangeably to IN_D[4:1].

Fig 1. Typical HDMI/DVI level shifter application system diagram

2. Features and benefits

2.1 High-speed TMDS level shifting

- Converts four lanes of low-swing AC-coupled differential input signals to DVI v1.0 and HDMI v1.4b compliant open-drain current-steering differential output signals
- TMDS level shifting operation up to 3 Gbit/s per lane (300 MHz TMDS clock) supporting 4K × 2K 3 Gbit/s and 3D video formats
- Programmable receive equalization
- Integrated 50 Ω termination resistors for self-biasing differential inputs
- Back-current safe outputs to disallow current when device power is off and monitor is on
- Disable feature to turn off TMDS inputs and outputs and to enter low-power condition
- Selectable differential output termination on TMDS channels

2.2 DDC level shifting

- Integrated DDC buffering and level shifting (3.3 V source to 5 V sink side and vice versa)
- Rise time accelerator on connector side DDC ports
- Up to 400 kHz I^2C-bus clock frequency
- Back-power safe sink-side terminals to disallow backdrive current when power is off or when DDC is not enabled

2.3 HPD level shifting

- HPD non-inverting level shift from 0 V on the sink side to 0 V on the source side, or from 5 V on the sink side to 3.3 V on the source side
- Integrated 200 kΩ pull-down resistor on HPD sink input guarantees ‘input LOW’ when no display is plugged in
- Back-power safe design on HPD_SINK to disallow backdrive current when power is off

2.4 General

- Power supply 3.3 V
- ESD resilience to 8 kV HBM, 1 kV CDM
- Power-saving modes
- Back-current-safe design on all sink-side main link, DDC and HPD terminals
- Transparent operation: no retiming or software configuration required
- 32-terminal HVQFN32 package

3. Applications

- PC motherboard/graphics card
- Docking station

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PTN3366BS	P3366	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN3366BS	PTN3366BSMP	HVQFN32	Reel 13” Q2/T3 *standard mark SMD dry pack	6000	T_{amb} = −40 °C to +105 °C

5. Functional diagram

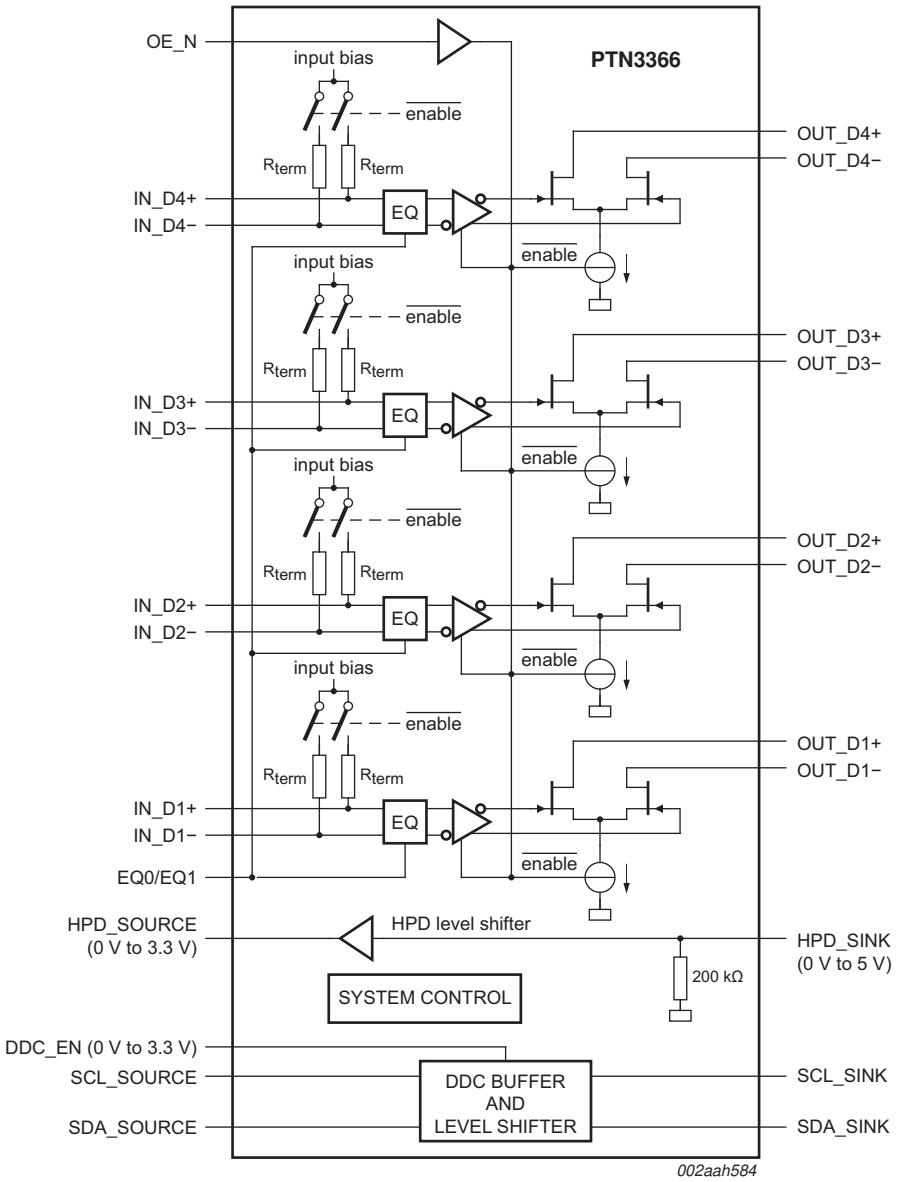
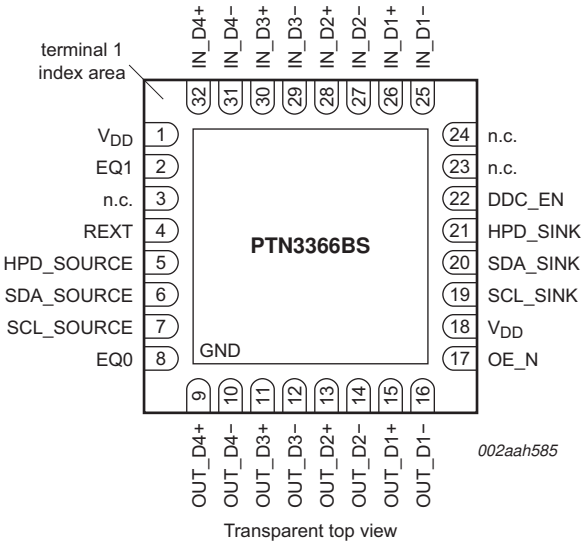


Fig 2. Functional diagram of PTN3366

6. Pinning information

6.1 Pinning



HVQFN32 package supply ground is connected to the exposed center pad. The exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region.

Fig 3. Pin configuration for HVQFN32

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
OE_N, IN_Dx and OUT_Dx signals			
OE_N	17	3.3 V low-voltage CMOS single-ended input	Output Enable and power saving function for high-speed differential level shifter path. When OE_N = HIGH: IN_Dx termination = high-Z OUT_Dx outputs = high-Z; zero output current When OE_N = LOW: IN_Dx termination = 50 Ω OUT_Dx outputs = active
IN_D4+	32	Self-biasing differential input	Low-swing differential input from display source. IN_D4+ makes a differential pair with IN_D4−. The input to this pin must be AC coupled externally.
IN_D4−	31	Self-biasing differential input	Low-swing differential input from display source. IN_D4− makes a differential pair with IN_D4+. The input to this pin must be AC coupled externally.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
IN_D3+	30	Self-biasing differential input	Low-swing differential input from display source. IN_D3+ makes a differential pair with IN_D3−. The input to this pin must be AC coupled externally.
IN_D3−	29	Self-biasing differential input	Low-swing differential input from display source. IN_D3− makes a differential pair with IN_D3+. The input to this pin must be AC coupled externally.
IN_D2+	28	Self-biasing differential input	Low-swing differential input from display source. IN_D2+ makes a differential pair with IN_D2−. The input to this pin must be AC coupled externally.
IN_D2−	27	Self-biasing differential input	Low-swing differential input from display source. IN_D2− makes a differential pair with IN_D2+. The input to this pin must be AC coupled externally.
IN_D1+	26	Self-biasing differential input	Low-swing differential input from display source. IN_D1+ makes a differential pair with IN_D1−. The input to this pin must be AC coupled externally.
IN_D1−	25	Self-biasing differential input	Low-swing differential input from display source. IN_D1− makes a differential pair with IN_D1+. The input to this pin must be AC coupled externally.
OUT_D4+	9	TMDS differential output	HDMI-compliant TMDS output. OUT_D4+ makes a differential pair with OUT_D4−. OUT_D4+ is in phase with IN_D4+.
OUT_D4−	10	TMDS differential output	HDMI-compliant TMDS output. OUT_D4− makes a differential pair with OUT_D4+. OUT_D4− is in phase with IN_D4−.
OUT_D3+	11	TMDS differential output	HDMI-compliant TMDS output. OUT_D3+ makes a differential pair with OUT_D3−. OUT_D3+ is in phase with IN_D3+.
OUT_D3−	12	TMDS differential output	HDMI-compliant TMDS output. OUT_D3− makes a differential pair with OUT_D3+. OUT_D3− is in phase with IN_D3−.
OUT_D2+	13	TMDS differential output	HDMI-compliant TMDS output. OUT_D2+ makes a differential pair with OUT_D2−. OUT_D2+ is in phase with IN_D2+.
OUT_D2−	14	TMDS differential output	HDMI-compliant TMDS output. OUT_D2− makes a differential pair with OUT_D2+. OUT_D2− is in phase with IN_D2−.
OUT_D1+	15	TMDS differential output	HDMI-compliant TMDS output. OUT_D1+ makes a differential pair with OUT_D1−. OUT_D1+ is in phase with IN_D1+.
OUT_D1−	16	TMDS differential output	HDMI-compliant TMDS output. OUT_D1− makes a differential pair with OUT_D1+. OUT_D1− is in phase with IN_D1−.
HPD and DDC signals			
HPD_SINK	21	5 V CMOS single-ended input	0 V to 5 V (nominal) input signal. This signal comes from the DVI or HDMI sink. A HIGH value indicates that the sink is connected; a LOW value indicates that the sink is disconnected. HPD_SINK is pulled down by an integrated 200 kΩ pull-down resistor.
HPD_SOURCE	5	3.3 V CMOS single-ended output	0 V to 3.3 V (nominal) output signal. This is level-shifted version of the HPD_SINK signal.
SCL_SOURCE	7	single-ended 3.3 V open-drain DDC I/O	3.3 V source-side DDC clock I/O. Pulled up by external termination to 3.3 V. 5 V tolerant I/O.
SDA_SOURCE	6	single-ended 3.3 V open-drain DDC I/O	3.3 V source-side DDC data I/O. Pulled up by external termination to 3.3 V. 5 V tolerant I/O.
SCL_SINK	19	single-ended 5 V open-drain DDC I/O	5 V sink-side DDC clock I/O. Pulled up by external termination to 5 V. Provides rise time acceleration for LOW-to-HIGH transitions.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
SDA_SINK	20	single-ended 5 V open-drain DDC I/O	5 V sink-side DDC data I/O. Pulled up by external termination to 5 V. Provides rise time acceleration for LOW-to-HIGH transitions.
DDC_EN	22	3.3 V CMOS input	Enables the DDC buffer and level shifter. When DDC_EN = LOW, buffer/level shifter is disabled. When DDC_EN = HIGH, buffer and level shifter are enabled.
Supply and ground			
V_{DD}	1, 18	3.3 V DC supply	Supply voltage; 3.3 V ± 10 %.
GND[1]	center pad	ground	Supply ground. The exposed center pad must be connected to system ground for proper operation.
Feature control signals			
REXT	4	analog I/O	Current sense port used to provide an accurate current reference for the differential outputs OUT_Dx. For best output voltage swing accuracy, use of a 12.4 kΩ resistor (1 % tolerance) from this terminal to GND is recommended. May also be tied to GND directly (0 Ω). See Section 7.2 for details.
EQ1	2	3.3 V low-voltage CMOS inputs	Equalizer setting input pins. These pins can be board-strapped to one of two decode values: short to GND, short to V_{DD}. See Table 5 for truth table.
EQ0	8		
n.c.	3, 23, 24	-	Not connected; leave this pin open.

[1] HVQFN32 package supply ground is connected to the exposed center pad. The exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Figure 2 “Functional diagram of PTN3366”.

The PTN3366 level shifts four lanes of low-swing AC-coupled differential input signals to DVI and HDMI-compliant open-drain current-steering differential output signals, up to 3 Gbit/s per lane to support 36-bit deep color, 3 Gbit/s and 3D modes. It has integrated 50 Ω termination resistors for AC-coupled differential input signals. An enable signal OE_N can be used to turn off the TMDS inputs and outputs, thereby minimizing power consumption to ultra low level. The TMDS outputs are back-power safe to disallow current flow from a powered sink while the PTN3366 is unpowered.

The PTN3366’s DDC channel provides active level shifting and buffering, allowing 3.3 V source-side termination and 5 V sink-side termination. The sink-side DDC ports are equipped with a rise time accelerator enabling drive of long cables or high bus capacitance. This enables the system designer to isolate bus capacitance to meet/exceed HDMI DDC specification. The PTN3366 offers back-power safe sink-side I/Os to disallow backdrive current from the DDC clock and data lines when power is off or when DDC is not enabled. An enable signal DCC_EN enables the DDC level shifter block.

The PTN3366 also provides voltage translation for the Hot Plug Detect (HPD) signal from 0 V to 5 V on the sink side to 0 V to 3.3 V on the source side.

The PTN3366 does not retime any data. It contains no state machines. No inputs or outputs of the device are latched or clocked. Because the PTN3366 acts as a transparent level shifter, no reset is required.

7.1 Enable and disable features

PTN3366 offers different ways to enable or disable functionality, using the Output Enable (OE_N), and DDC Enable (DDC_EN) inputs. Whenever the PTN3366 is disabled (OEN = HIGH **and** DDC_EN = LOW), the device is in Ultra low power mode and power consumption is ultra low; otherwise the PTN3366 is in active mode and power consumption depends on level of HPD_SINK signal. These two inputs each affect the operation of PTN3366 differently: OE_N controls the TMDS channels, DDC_EN controls only the DDC channel, and HPD_SINK is not affected by either of the control inputs. The following sections and truth table describe their detailed operation.

7.1.1 Hot plug detect

The HPD channel of PTN3366 functions as a level-shifting buffer to pass the HPD logic signal from the display sink device (via input HPD_SINK) on to the display source device (via output HPD_SOURCE). The HPD_SINK level is used to control the power state of the PTN3366. If HPD_SINK is LOW, then PTN3366 is in standby mode. Once HPD_SINK goes HIGH, the PTN3366 can operate and its behavior is controlled further by other control pins — OE_N, DDC_EN.

The HPD channel operates independent of all these control signals.

HPD_SOURCE output follows the HPD_SINK input regardless of the power mode.

7.1.2 Output Enable function (OE_N)

When input OE_N is asserted (active LOW), the IN_Dx and OUT_Dx signals are fully functional. Input termination resistors are enabled and the internal bias circuits are turned on.

When OE_N is de-asserted (inactive HIGH), the OUT_Dx outputs are in a high-impedance state. The IN_Dx input buffers are disabled and IN_Dx termination is disabled. Power consumption is minimized.

Remark: OE_N signal level has no influence on the HPD_SINK input, HPD_SOURCE output, or the SCL and SDA level shifters.

7.1.3 DDC channel enable function (DDC_EN)

The DDC_EN pin is active HIGH and can be used to isolate a badly behaved slave. When DDC_EN is LOW, the DDC channel is turned off. The DDC_EN input should never change state during an I^2C-bus operation. Note that disabling DDC_EN during a bus operation may hang the bus, while enabling DDC_EN during bus traffic would corrupt the I^2C-bus operation. Hence, DDC_EN should only be toggled while the bus is idle. The DDC channel enable (DDC_EN) and TMDS output enable (OE_N) can be controlled independent of each other.

7.1.4 Enable/disable truth table

Table 4. HPD_SINK, OE_N and DDC_EN enabling truth table

Inputs			Channels				Mode
HPD_SINK	OE_N	DDC_EN [1]	IN_Dx	OUT_Dx[2]	DDC[3]	HPD_SOURCE [4]	
LOW	LOW	LOW	high-Z	high-Z	high-Z	LOW	Standby
LOW	LOW	HIGH	high-Z	high-Z	high-Z	LOW	Standby
LOW	HIGH	LOW	high-Z	high-Z	high-Z	LOW	Ultra low power
LOW	HIGH	HIGH	high-Z	high-Z	high-Z	LOW	Standby
HIGH	LOW	LOW	50 Ω termination to $V_{RX(bias)}$	outputs are enabled	high-Z	HIGH	Active; DDC disabled
HIGH	LOW	HIGH	50 Ω termination to $V_{RX(bias)}$	outputs are enabled	SDA_SINK connected to SDA_SOURCE and SCL_SINK connected to SCL_SOURCE	HIGH	Active; DDC enabled
HIGH	HIGH	LOW	high-Z	high-Z	high-Z	HIGH	Ultra low power
HIGH	HIGH	HIGH	50 Ω termination to $V_{RX(bias)}$	high-Z	SDA_SINK connected to SDA_SOURCE and SCL_SINK connected to SCL_SOURCE	HIGH	Standby; DDC enabled

[1] A LOW level on input DDC_EN disables only the DDC channel.

[2] OUT_Dx channels 'enabled' means outputs OUT_Dx toggling in accordance with IN_Dx differential input voltage switching.

[3] DDC channel 'enabled' means SDA_SINK is connected to SDA_SOURCE and SCL_SINK is connected to SCL_SOURCE.

[4] The HPD_SOURCE output logic state always follows the HPD_SINK input logic state.

7.2 Analog current reference

The REXT pin (pin 6) is an analog current sense port used to provide an accurate current reference for the differential outputs OUT_Dx. For best output voltage swing accuracy, use of a 12.4 kΩ resistor (1 % tolerance) connected between this terminal and GND is recommended.

If an external 12.4 kΩ ± 1 % resistor is not used, this pin can be connected to GND or V_{DD} directly (0 Ω). In any of these cases, the output functions normally but at reduced accuracy over voltage and temperature of the following parameters: output levels (V_{OL}), differential output voltage swing, and rise and fall time accuracy.

7.3 Equalizer

The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

Table 5. Equalizer settings

Inputs		Equalization for 3 Gbit/s
EQ1	**EQ0**	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB

7.4 Backdrive current protection

The PTN3366 is designed for backdrive protection on all sink-side TMDS outputs, sink-side DDC I/Os and the HPD_SINK input. This supports user scenarios where the display is connected and powered, but the PTN3366 is unpowered. In these cases, the PTN3366 sinks no more than a negligible amount of leakage current, and blocks the display (sink) termination network from driving the power supply of the PTN3366 or that of the inactive DVI or HDMI source or back into the V_{DD} power supply rail.

7.5 Squelch function

PTN3366 operates only when the input signal level is above certain minimum threshold (as per $V_{RX\_DIFFp\text{-}p}$). If the input falls below that minimum threshold, the outputs are squelched.

7.6 Active DDC buffer with rise time accelerator

The PTN3366 DDC channel, besides providing 3.3 V to 5 V level shifting, includes active buffering and rise time acceleration for reliable DDC applications. While retaining all the operating modes and features of the I^2C-bus system during the level shifts, it permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) line as well as the rise time accelerator on the sink-side port (SCL_SINK and SDA_SINK) enabling the bus to drive a load up to 1400 pF and 400 pF on the source-side port (SCL_SOURCE and SCA_SOURCE). Using the PTN3366 for DVI or HDMI level shifting enables the system designer to isolate bus capacitance to meet/exceed HDMI DDC specification. The SDA and SCL pins are in high-impedance when the PTN3366 is unpowered or when DDC_EN is LOW.

PTN3366 has rise time accelerators on the sink-side port (SCL_SINK and SDA_SINK) only. During positive bus transitions on the sink-side port, a current source is switched on to quickly slew the SCL_SINK and SDA_SINK lines HIGH once the 5 V DDC bus V_{IL} threshold level of around 1.5 V is exceeded, and turns off as the 5 V DDC bus V_{IH} threshold voltage of approximately 3.5 V is approached.

7.7 Power management

PTN3366 implements innovative power management scheme whereby it achieves very low power consumption in both active and standby modes. Based on OE_N, DDC_EN, HPD_SNK, the PTN3366 intelligently optimizes the power consumption and disables outputs (OUT_Dx). Refer to Table 6.

Table 6. Power management schemes

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	HIGH	LOW	high-Z	Standby mode
HIGH	LOW	don't care	high-Z	Ultra low-power mode

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.3	+4.6	V
V_I	input voltage	3.3 V CMOS inputs	−0.3	V_{DD} + 0.5	V
		5.0 V CMOS inputs	−0.3	6.0	V
T_{stg}	storage temperature		−65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	8000	V
		CDM [2]	-	1000	V

[1] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[2] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

9. Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_I	input voltage	3.3 V CMOS inputs	0	-	3.6	V
		5.0 V CMOS inputs	0	-	5.5	V
$V_{I(AV)}$	average input voltage	IN_Dn+, IN_Dn− inputs [1]	-	0	-	V
$R_{ref(ext)}$	external reference resistance	connected between pin REXT (pin 4) and GND [2]	-	12.4 ± 1 %	-	kΩ
T_{amb}	ambient temperature	operating in free air	−40	-	+105	°C

[1] Input signals to these pins must be AC-coupled.

[2] Operation without external reference resistor is possible but results in reduced output voltage swing accuracy. For details, see Section 7.2.

9.1 Current consumption

Table 9. Current consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	OE_N = LOW; Active mode	-	22	-	mA
		OE_N = LOW; HPD_SINK = LOW; Standby mode	-	25	-	μA
		OE_N = HIGH, HPD_SINK = don't care **and** DDC_EN = LOW; Ultra low-power mode	-	-	10	μA

10. Characteristics

10.1 Differential inputs

Table 10. Differential input characteristics for IN_Dx signals

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UI	unit interval[1]	nominal value at 3.0 Gbit/s [2]	-	333	-	ps
		nominal value at 250 Mbit/s [2]	-	4000	-	ps
$V_{RX\_DIFFp\text{-}p}$	differential input peak-to-peak voltage	[3]	0.15	-	1.2	V
t_{RX_EYE}	receiver eye time	minimum eye width at IN_Dx input pair	0.8	-	-	UI
$V_{i(cm)M(AC)}$	peak common-mode input voltage (AC)	includes all frequencies above 30 kHz [4]	-	-	100	mV
Z_i	input impedance	DC input impedance	40	50	60	Ω
$V_{RX(bias)}$	bias receiver voltage		1.0	1.8	1.95	V
$Z_{I(se)}$	single-ended input impedance	inputs in high-Z state [5]	100	-	-	kΩ
RL_{in}	input return loss	differential input; active mode				
		f = 100 MHz	-	−20	-	dB
		f = 1.5 GHz	-	−16	-	dB
		f = 3.0 GHz	-	−11	-	dB

[1] UI (unit interval) = t_{bit} (bit time).

[2] UI is determined by the display mode. Nominal bit rate ranges from 250 Mbit/s to 3 Gbit/s per lane.

[3] $V_{RX\_DIFFp\text{-}p} = 2 \times |V_{RX\_D+} - V_{RX\_D-}|$. Applies to IN_Dx signals.

[4] $V_{i(cm)M(AC)} = |V_{RX\_D+} + V_{RX\_D-}| / 2 - V_{RX(cm)}$.
$V_{RX(cm)}$ = DC (avg) of $|V_{RX\_D+} + V_{RX\_D-}| / 2$.

[5] Differential inputs switch to a high-impedance state when OE_N is HIGH.

10.2 Differential outputs

The level shifter's differential outputs are designed to meet HDMI version 1.4b and DVI version 1.0 specifications.

Table 11. Differential output characteristics for OUT_Dx signals

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH(se)}$	single-ended HIGH-level output voltage	[1]	V_{TT} − 0.01	V_{TT}	V_{TT} + 0.01	V
$V_{OL(se)}$	single-ended LOW-level output voltage	[2]	V_{TT} − 0.60	V_{TT} − 0.50	V_{TT} − 0.40	V
$\Delta V_{O(se)}$	single-ended output voltage variation	logic 1 and logic 0 state applied respectively to differential inputs IN_Dx; $R_{ref(ext)}$ connected; see Table 8 [3]	400	500	600	mV
I_{OZ}	OFF-state output current	single-ended	-	-	10	μA
t_r	rise time	20 % to 80 %	75	-	150	ps
t_f	fall time	80 % to 20 %	75	-	150	ps
t_{sk}	skew time	intra-pair [4]	-	15	-	ps
		inter-pair [5]	-	-	250	ps
$t_{jit(add)}$	added jitter time	jitter contribution for TMDS signaling at 3.4 Gbit/s; PRBS7 pattern; EQ0 = LOW; EQ1 = LOW; refer to Figure 4 [6]	-	13	-	ps

[1] V_{TT} is the DC termination voltage in the HDMI or DVI sink. V_{TT} is nominally 3.3 V.

[2] The open-drain output pulls down from V_{TT}.

[3] Swing down from TMDS termination voltage (3.3 V ± 10 %).

[4] This differential skew budget is in addition to the skew presented between IN_D+ and IN_D− paired input pins.

[5] This lane-to-lane skew budget is in addition to skew between differential input pairs.

[6] Jitter budget for differential signals as they pass through the level shifter.

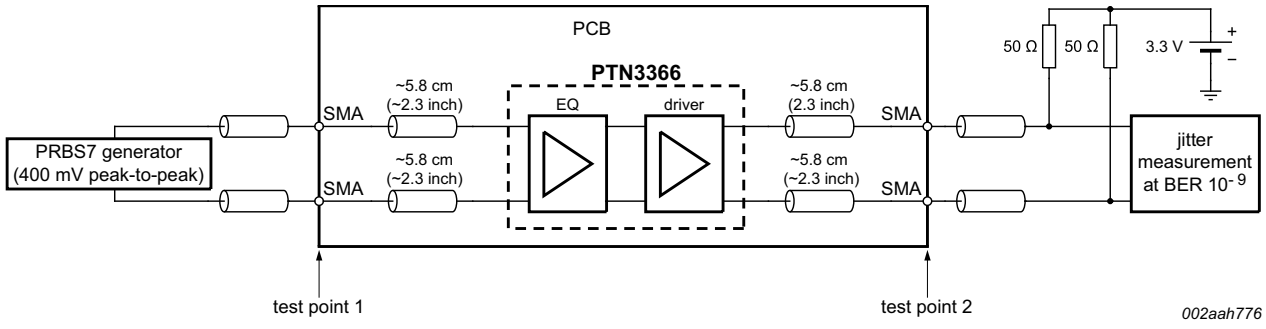


Fig 4. Setup for added jitter measurement

10.3 HPD_SINK input, HPD_SOURCE output

Table 12. HPD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	HPD_SINK [1]	2.0	5.0	5.3	V
V_{IL}	LOW-level input voltage	HPD_SINK	0	-	0.8	V
I_{LI}	input leakage current	HPD_SINK	-	-	40	μA
V_{OH}	HIGH-level output voltage	HPD_SOURCE	2.5	-	V_{DD}	V
V_{OL}	LOW-level output voltage	HPD_SOURCE	0	-	0.2	V
t_{PD}	propagation delay	from HPD_SINK to HPD_SOURCE; 50 % to 50 % [2]	-	-	200	ns
t_t	transition time	HPD_SOURCE rise/fall; 10 % to 90 % [3]	1	-	20	ns
R_{pd}	pull-down resistance	HPD_SINK input pull-down resistor [4]	150	210	270	kΩ

[1] Low-speed input changes state on cable plug/unplug.

[2] Time from HPD_SINK changing state to HPD_SOURCE changing state. Includes HPD_SOURCE rise/fall time.

[3] Time required to transition from V_{OH} to V_{OL} or from V_{OL} to V_{OH}.

[4] Guarantees HPD_SINK is LOW when no display is plugged in.

10.4 OE_N, DDC_EN, EQ0, EQ1

Table 13. OE_N, DDC_EN input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-		V
V_{IL}	LOW-level input voltage			-	0.8	V
I_{LI}	input leakage current	OE_N pin [1]	-	-	10	μA

[1] Measured with input at V_{IH} maximum and V_{IL} minimum.

10.5 DDC characteristics

Table 14. DDC characteristics

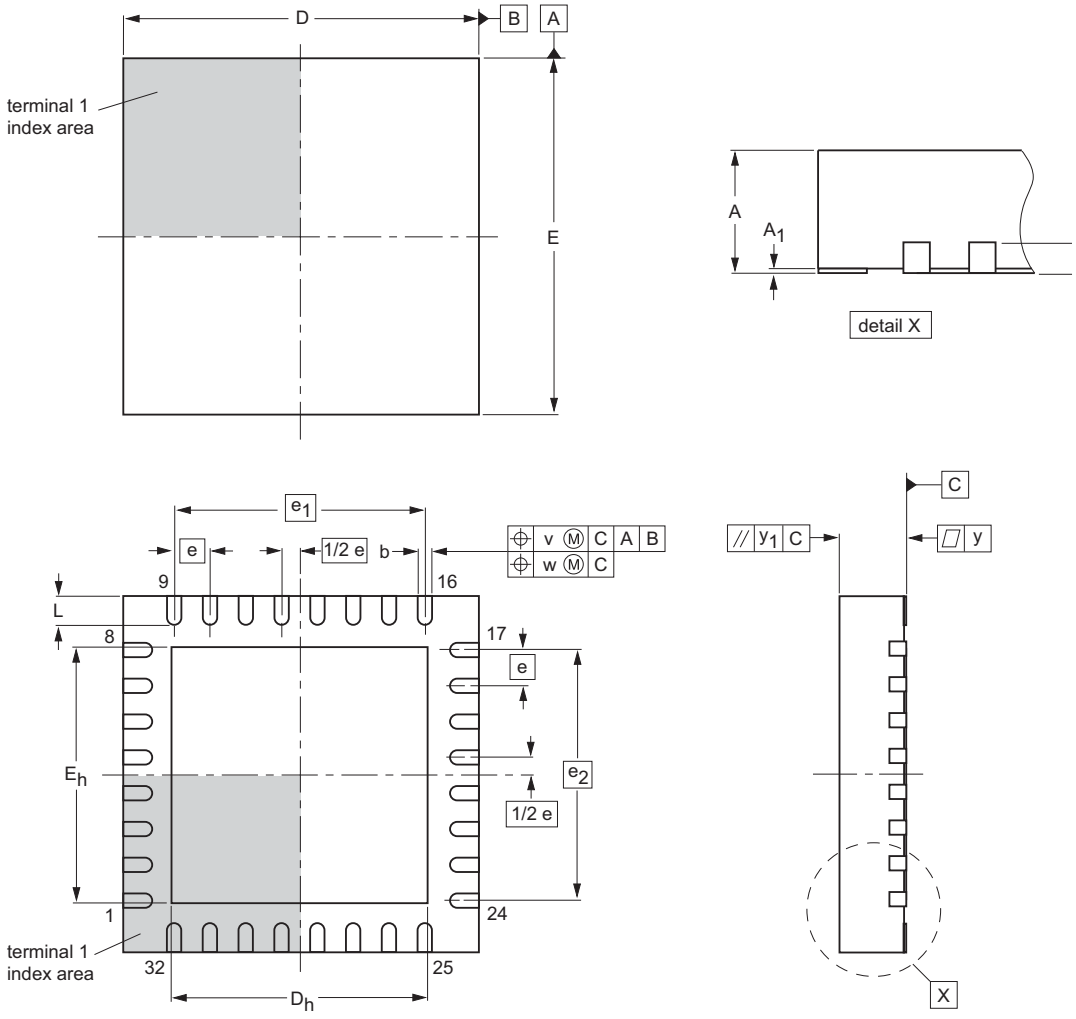
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input and output SCL_SOURCE and SDA_SOURCE, V_{CC1} = 2.8 V to 3.6 V[1]						
V_{IH}	HIGH-level input voltage		0.7 × V_{CC1}	-	3.6	V
V_{IL}	LOW-level input voltage		−0.5	-	+0.4	V
I_{LI}	input leakage current	V_I = 3.6 V	-	-	10	μA
I_{IL}	LOW-level input current	V_I = 0.2 V	-	-	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 100 μA or 6 mA	0.47	0.52	0.6	V
V_{OL}−V_{IL}	difference between LOW-level output and LOW-level input voltage	guaranteed by design to prevent contention	-	70	-	mV
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{DD} = 3.3 V	-	6	7	pF
		V_I = 3 V or 0 V; V_{DD} = 0 V	-	6	7	pF
Input and output SDA_SINK and SCL_SINK, V_{CC2} = 4.5 V to 5.5 V[2]						
V_{IH}	HIGH-level input voltage		0.7 × V_{CC2}	-	5.5	V
V_{IL}	LOW-level input voltage		−0.5	-	+1	V
I_{LI}	input leakage current	V_I = 5.5 V	-	-	10	μA
I_{IL}	LOW-level input current	V_I = 0.2 V	-	-	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA	-	0.1	0.2	V
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{DD} = 3.3 V	-	-	7	pF
		V_I = 3 V or 0 V; V_{DD} = 0 V	-	6	7	pF
$I_{trt(pu)}$	transient boosted pull-up current	V_{CC2} = 4.5 V; slew rate = 1.25 V/μs	-	4	-	mA

[1] V_{CC1} is the pull-up voltage for DDC source.

[2] V_{CC2} is the pull-up voltage for DDC sink.

11. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit(1)		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Fig 5. Package outline SOT617-3 (HVQFN32)

12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 6) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15 and 16

Table 15. SnPb eutectic process (from J-STD-020D)

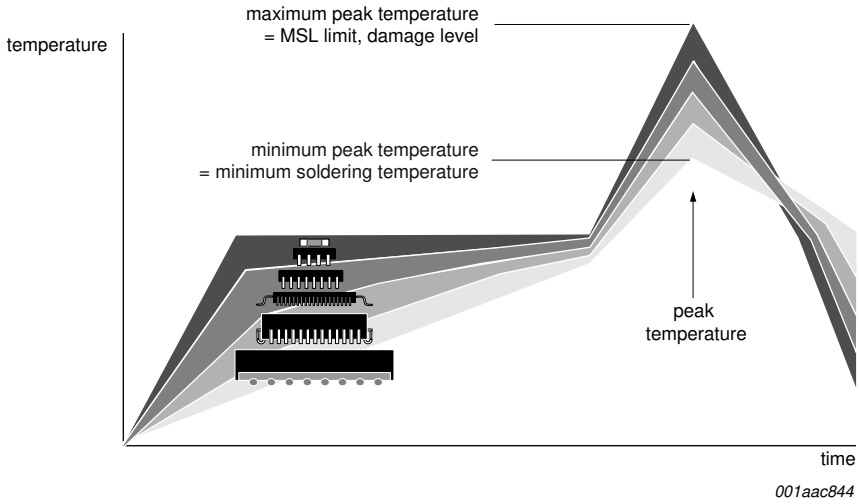
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 6.



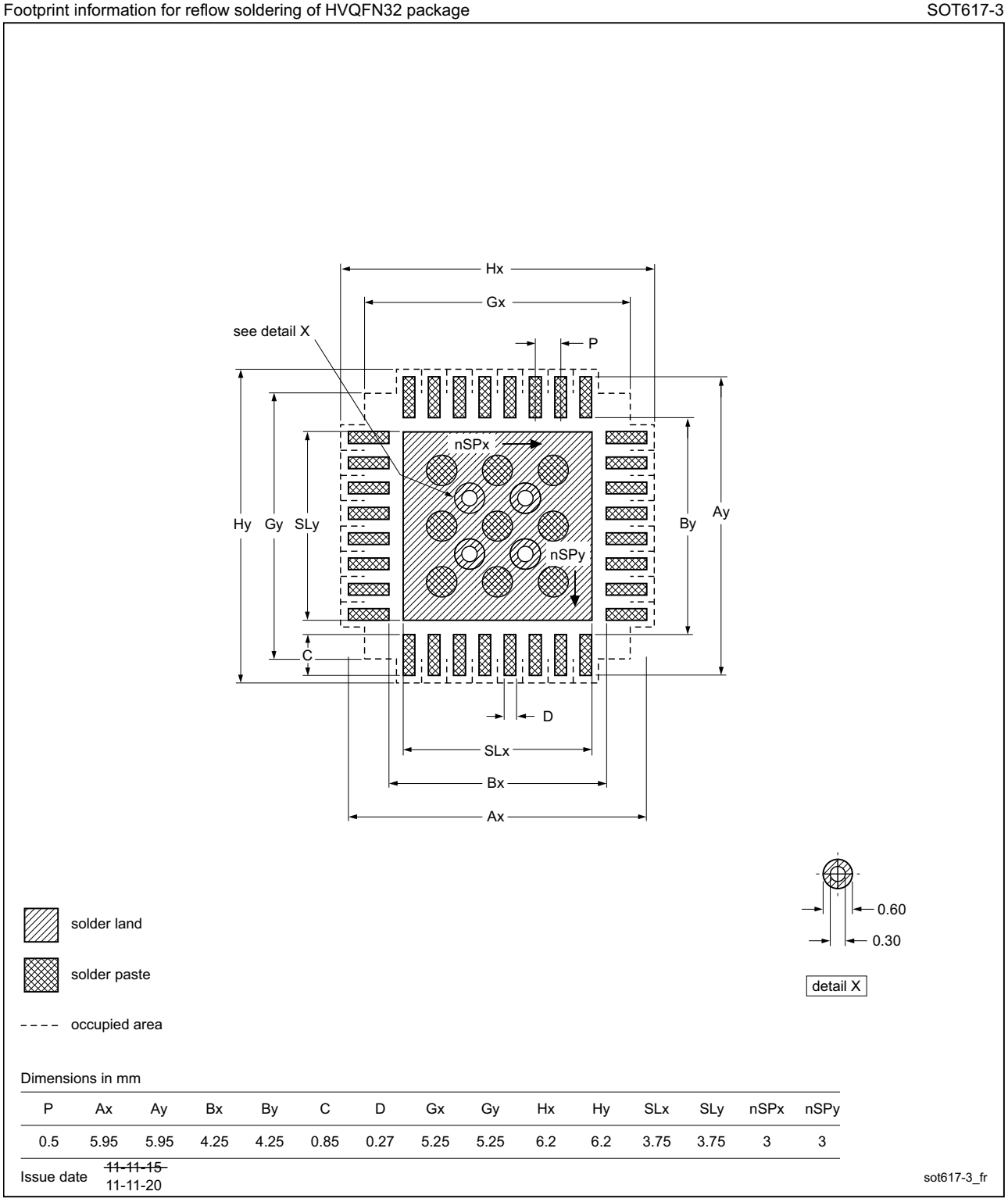
MSL: Moisture Sensitivity Level

Fig 6. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Soldering: PCB footprints

Footprint information for reflow soldering of HVQFN32 package SOT617-3



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

sot617-3_fr

Fig 7. PCB footprint for SOT617-3 (HVQFN32); reflow soldering

14. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CEC	Consumer Electronics Control
DDC	Data Display Channel
DP	Dry Pack
DVI	Digital Visual Interface
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I^2C-bus	Inter-IC bus
I/O	Input/Output
NMOS	Negative-channel Metal-Oxide Semiconductor
SMD	Surface Mount Device
TMDS	Transition Minimized Differential Signaling
VESA	Video Electronic Standards Association

15. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN3366 v.1.1	20150522	Product data sheet	-	PTN3366 v.1
Modification:	• Changed document status to Company Public.			
PTN3366 v.1	20130820	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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