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# PTN3392

## 2-lane DisplayPort to VGA adapter IC

Rev. 5 — 5 June 2014

Product data sheet

## 1. General description

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The PTN3392 is a DisplayPort to VGA adapter IC designed to connect a DisplayPort source to a VGA sink. The PTN3392 integrates a DisplayPort receiver and a high-speed triple video digital-to-analog converter that supports display resolutions from VGA to WUXGA (see [Table 5](#)). The PTN3392 supports either one or two DisplayPort v1.1a lanes operating at either 2.7 Gbit/s or 1.62 Gbit/s per lane. The PTN3392 has 'Flash-over-AUX' capability enabling simple firmware upgradability in the field.

The PTN3392 supports I<sup>2</sup>C-bus over AUX per *DisplayPort v1.1a specification* ([Ref. 1](#)), and bridges the VESA DDC channel to the DisplayPort Interface.

The PTN3392 is designed for single supply and minimizes application costs. It can be powered directly from the DisplayPort source side 3.3 V supply without a need for additional core voltage regulator. The VGA output is powered down when there is no valid DisplayPort source data being transmitted. The PTN3392 also aids in monitor detection by performing load sensing and reporting sink connection status to the source.

## 2. Features and benefits

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### 2.1 VESA-compliant DisplayPort v1.1a converter

- Main Link: 1-lane and 2-lane modes supported
  - ◆ HBR (High Bit Rate) at 2.7 Gbit/s per lane
  - ◆ RBR (Reduced Bit Rate) at 1.62 Gbit/s per lane
  - ◆ BER (Bit Error Rate) better than 10<sup>-9</sup>
  - ◆ Down-spreading SSC (Spread Spectrum Clocking) supported
- 1 MHz AUX channel
  - ◆ Supports native AUX CH syntax
  - ◆ Supports I<sup>2</sup>C-bus over AUX CH syntax
- Hot Plug Detect (HPD) signal to the source
- Cost-effective design optimized for VGA application

### 2.2 DDC channel output

- Supports 100 kbit/s I<sup>2</sup>C-bus speed, declared in DPCD register
  - ◆ Support of I<sup>2</sup>C-bus speed control by DisplayPort source via DPCD registers, facilitating use of longer VGA cables
- I<sup>2</sup>C Over Aux feature facilitates full support of MCCS, DDC-CI, and DDC protocols (see [Ref. 2](#))



## 2.3 Analog video output

- VSIS 1.2 compliance ([Ref. 3](#)) for all supported video output modes
- Analog RGB current-source outputs
- VSYNC and HSYNC outputs
- Pixel clock up to 240 MHz
- Triple 8-bit Digital-to-Analog Converter (DAC)
- Direct drive of double terminated 75  $\Omega$  load with standard 700 mV (peak-to-peak) signals

## 2.4 General features

- Supports 'Flash-over-AUX' field upgradability
- Monitor presence detection. Connection/disconnection reported via HPD IRQ and DPCD update.
- All display resolutions from VGA to WUXGA are supported<sup>1</sup>, including e.g.:
  - ◆ WUXGA: 6 bits, 1920 × 1200, 60 Hz, 193 MHz pixel clock rate
  - ◆ WUXGA: 1920 × 1200, 60 Hz, reduced blanking, 154 MHz pixel clock rate
  - ◆ UXGA: 1600 × 1200, 60 Hz, 162 MHz pixel clock rate
  - ◆ SXGA: 1280 × 1024, 60 Hz, 108 MHz pixel clock rate
  - ◆ XGA: 1024 × 768, 60 Hz, 65 MHz pixel clock rate
  - ◆ SVGA: 800 × 600, 60 Hz, 40 MHz pixel clock rate
  - ◆ VGA: 640 × 480, 60 Hz, 25 MHz pixel clock rate
  - ◆ Any resolution and refresh rates are supported up to 8 bit color
- Bits per color (bpc) supported<sup>1</sup>
  - ◆ 6, 8 bits supported
  - ◆ 10, 12, 16 bits supported by truncation to 8 MSBs
- All VGA colorimetry formats (RGB) supported
- Power modes
  - ◆ Active-mode power consumption:
    - ~600 mW at UXGA / 162 MHz pixel clock
    - ~500 mW at SXGA / 108 MHz pixel clock
  - ◆ ~40 mW at Low-power mode or before link training started
- On-board crystal oscillator for use with external 27 MHz crystal
- ESD protection
  - ◆ 7 kV ESD HBM JEDEC
  - ◆ 8 kV ESD HBM IEC 61000-4-2 ([Ref. 4](#))
- 3.3 V  $\pm$  10 % power supply
- Commercial temperature range: 0 °C to 85 °C
- 48-pin HVQFN, 7 mm × 7 mm × 0.85 mm (nominal); 0.5 mm pitch; lead-free package

1. Except for color depth beyond 8 bits, display resolutions and refresh rates are only limited to those which a standard 2-lane DisplayPort configuration is able to support.

### 3. Applications

- Dongle PC accessory
  - ◆ Dongle connected to PC DisplayPort output and connected to RGB monitor via VGA cable
  - ◆ PTN3392 is powered by the DP\_PWR pin on the DisplayPort connector
- Desktop and notebook computers
- Notebook docking stations

### 4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PTN3392BS <sup>[1]</sup>	PTN3392BS	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; 7 × 7 × 0.85 mm	SOT619-1
PTN3392BS/FX <sup>[2]</sup>	PTN3392BS	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; 7 × 7 × 0.85 mm	SOT619-1

[1] PTN3392BS uses latest firmware version.

[2] PTN3392BS/FX uses specific firmware version ('X' = 1, 2, 3, etc., and changes according to firmware version).

#### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN3392BS <sup>[1]</sup>	PTN3392BS,518	HVQFN48	Reel 13" Q1/T1 *standard mark SMD dry pack	4000	T <sub>amb</sub> = 0 °C to +85 °C
PTN3392BS/FX <sup>[2]</sup>	PTN3392BS/FX,518 <sup>[3]</sup>	HVQFN48	Reel 13" Q1/T1 *standard mark SMD dry pack	4000	T <sub>amb</sub> = 0 °C to +85 °C
	PTN3392BS/FXY <sup>[3]</sup>	HVQFN48	Reel 13" Q1/T1 *standard mark SMD dry pack	4000	T <sub>amb</sub> = 0 °C to +85 °C

[1] PTN3392BS uses latest firmware version.

[2] PTN3392BS/FX uses specific firmware version ('X' = 1, 2, 3, etc., and changes according to firmware version).

[3] PTN3392BS/FX,518 is orderable part number for firmware versions 1, 2, or 3.  
PTN3392BS/FXY is orderable part number for firmware versions 4 or higher.

5. Functional diagram

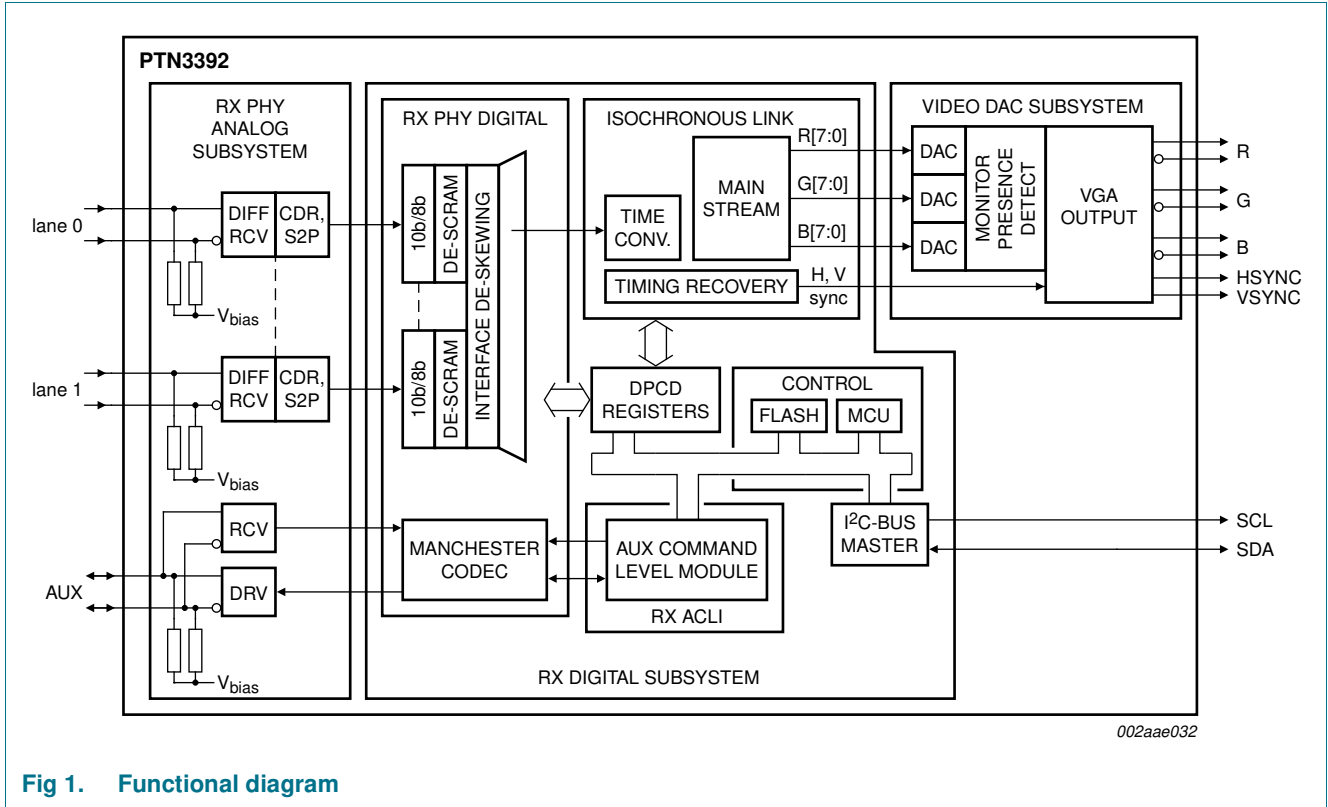
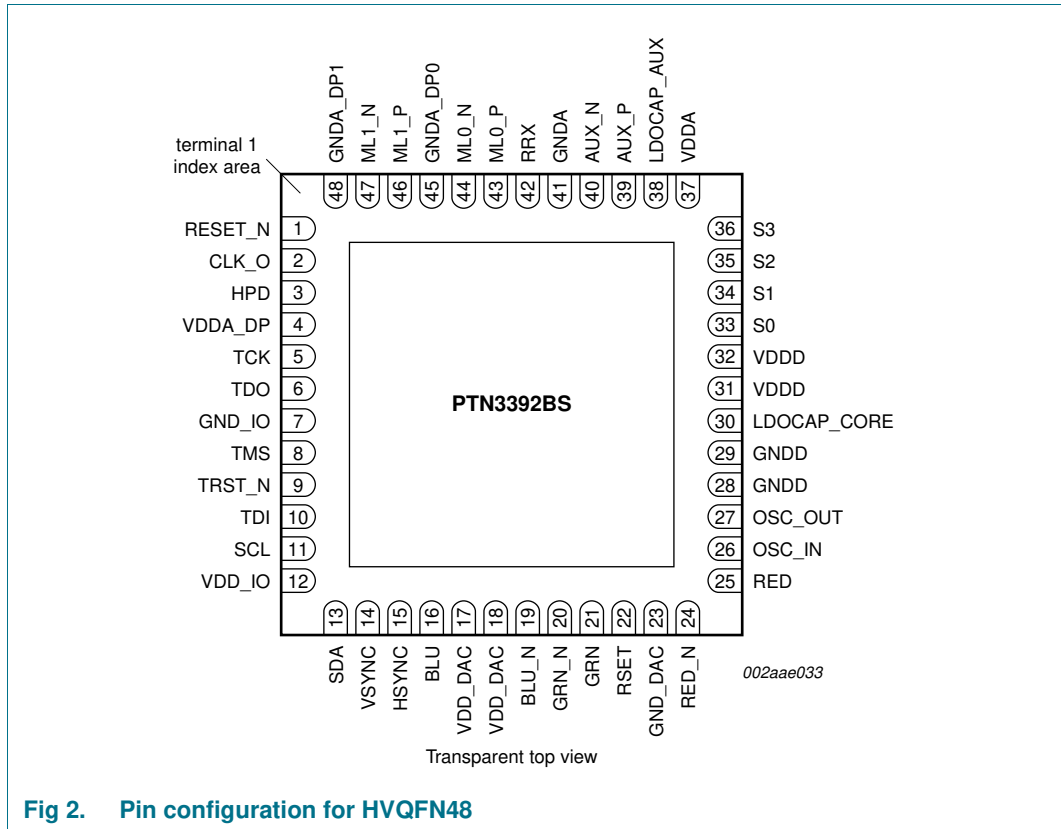


Fig 1. Functional diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
VDDD	32, 31	power	digital core 3.3 V supply
VDDA	37	power	analog AUX, bias and PLL 3.3 V supply voltage
VDDA_DP	4	power	analog 3.3 V supply for DisplayPort receiver module
VDD_IO	12	power	I/O 3.3 V supply voltage
VDD_DAC	17, 18	power	analog 3.3 V supply for DAC
GND_IO <sup>[1]</sup>	7	power	I/O supply ground
GND_DAC <sup>[1]</sup>	23	power	analog ground for DAC
GND_A_DP0 <sup>[1]</sup>	45	power	analog ground for DisplayPort Lane0
GND_A_DP1 <sup>[1]</sup>	48	power	analog ground for DisplayPort Lane1
GND_A <sup>[1]</sup>	41	power	analog AUX, bias and PLL supply ground
GNDD <sup>[1]</sup>	28, 29	power	digital core supply ground

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
<b>DisplayPort</b>			
ML0_P	43	self-biasing differential input	DisplayPort main lane signal lane 0, positive
ML0_N	44	self-biasing differential input	DisplayPort main lane signal lane 0, negative
ML1_P	46	self-biasing differential input	DisplayPort main lane signal lane 1, positive
ML1_N	47	self-biasing differential input	DisplayPort main lane signal lane 1, negative
AUX_P	39	self-biasing differential input/output	DisplayPort auxiliary channel signal, positive
AUX_N	40	self-biasing differential input/output	DisplayPort auxiliary channel signal, negative
HPD	3	3.3 V TTL single-ended output	Hot-plug detect
<b>RGB DAC outputs</b>			
BLU	16	analog output	'blue' current analog output
BLU_N	19	analog output	'blue' current complementary analog output
GRN	21	analog output	'green' current analog output
GRN_N	20	analog output	'green' current complementary analog output
RED	25	analog output	'red' current analog output
RED_N	24	analog output	'red' current complementary analog output
RSET	22	analog input/output	DAC full-scale current control resistor. Pull down to ground by an external 1.2 k $\Omega$ $\pm$ 1 % resistor.
<b>DDC</b>			
SCL	11	single-ended 5 V open-drain DDC I/O	5 V sink-side DDC clock I/O. Pulled up by 1.2 k $\Omega$ external resistor to 5 V.
SDA	13	single-ended 5 V open-drain DDC I/O	5 V sink-side DDC data I/O. Pulled up by 1.2 k $\Omega$ external resistor to 5 V.
<b>Monitor-side sync</b>			
HSYNC	15	single-ended 3.3 V TTL output	horizontal sync signal to monitor; serial resistance of 36 $\Omega$ is recommended.
VSYNC	14	single-ended 3.3 V TTL output	vertical sync signal to monitor; serial resistance of 36 $\Omega$ is recommended.
<b>JTAG</b>			
TCK	5	input	JTAG clock input
TDO	6	output	JTAG data output
TMS	8	input	JTAG mode select input
TRST_N	9	input	JTAG reset (active LOW) input
TDI	10	input	JTAG data input

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
<b>Strap pins, S[3:0]</b>			
S0	33	input	Open (internal pull-down) = logic 0: Implement VGA-side monitor detect according to <i>VESA DisplayPort Standard v1.1a</i> sections 7 and 8 ( <a href="#">Ref. 1</a> ). Refer to <a href="#">Section 7.4.1</a> for S0 = 0 behavior. HIGH (external pull-up) = logic 1: Set HPD HIGH upon VGA monitor detection; set HPD LOW upon VGA monitor detachment. Refer to <a href="#">Section 7.4.2</a> for S0 = 1 behavior. Default S0 = 0 for standard compliance.
S1	34	input	reserved; leave open-circuit (default internal pull-down)
S2	35	input	Open (internal pull-down) = logic 0 to set default I <sup>2</sup> C speed to 50 kbit/s for PTN3392BS/F3, 100 kbit/s for PTN3392BS/F1, PTN3392BS/F2. HIGH (external pull-up) = logic 1, to set default I <sup>2</sup> C speed to 10 kbit/s. This pin may be left open-circuit (internal pull-down) or tied to V <sub>DD</sub> according to the desired default I <sup>2</sup> C speed. See more explanation in <a href="#">Table 4</a> about S2 pin setting and DPCD register 00109h.
S3	36	input	reserved; leave open-circuit (default internal pull-down)
<b>Miscellaneous</b>			
RESET_N	1	input	Hardware reset input (active LOW); internal pull-up. A capacitor must be connected between this pin and ground. A 1 μF capacitor is recommended.
CLK_O	2	output	DisplayPort receiver test clock output
LDOCAP_CORE	30	power	1.8 V digital core supply decoupling
OSC_IN	26	input	crystal oscillator input
OSC_OUT	27	output	crystal oscillator output
LDOCAP_AUX	38	power	1.8 V AUX supply decoupling
RRX	42	input	Receiver termination resistance control. A 12 kΩ resistor must be connected between this pin and LDOCAP_AUX (pin 38).

- [1] HVQFN48 package die supply ground is connected to both GND pins and exposed center pad. GND pins 7, 23, 28, 29, 41, 45, 48, and exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region.



## 7. Functional description

Referring to [Figure 1 “Functional diagram”](#), the PTN3392 converts the DisplayPort AC-coupled high-speed differential signaling protocol into a VESA VSIS 1.2 compliant analog VGA signaling. The PTN3392 integrates a DisplayPort receiver (according to *VESA DisplayPort v1.1a specification*, [Ref. 1](#)) and a high-speed triple 8-bit video digital-to-analog converter that supports display resolution from VGA to WUXGA (see [Table 5 “Display resolution and pixel clock rate”](#)), up to a pixel clock rate of 240 MHz. The PTN3392 supports one or two DisplayPort v1.1a Main Link lanes operating at either in 2.7 Gbit/s or 1.62 Gbit/s per lane. The PTN3392 can drive up to 100 feet of analog video cable.

The DisplayPort receiver comprises the following functional blocks:

- Main Link
- AUX CH (Auxiliary Channel)
- DPCD (DisplayPort Configuration Data)
- Monitor detection
- EDID handling
- Video DAC

The RGB video data with corresponding synchronization references is extracted from the main stream video data. Main stream video attribute information is also extracted. This information is inserted once per video frame during the vertical blanking period by the DisplayPort source. The attributes describe the main video stream format in terms of geometry, timing, and color format. The original clock and video stream are derived from these main link data.

The PTN3392 internal DPCD registers can be accessed by the source via the auxiliary channel. The monitor's DDC control bus may also be controlled via the auxiliary channel. A bridging conversion block translates the input DisplayPort auxiliary channel signals from the source side to the DDC signals on the sink side. The PTN3392 passes through sink-side status change (e.g., hot-plug events) to the source side, through HPD interrupts and DPCD registers.

### 7.1 DisplayPort Main Link

The DisplayPort main link consists of doubly terminated, AC-coupled differential pair. The 50  $\Omega$  internally calibrated termination resistors are integrated inside PTN3392.

The PTN3392 supports HBR at 2.7 Gbit/s and RBR at 1.62 Gbit/s per lane.

### 7.2 DisplayPort auxiliary channel

The AUX CH is a half-duplex, bidirectional channel between DisplayPort transmitter and receiver. It consists of one differential pair transporting self-clocked data at 1 Mbit/s. The PTN3392 integrates the AUX CH replier (or slave), and responds to transactions initiated by the DisplayPort source AUX CH requester (or master).

The AUX CH uses the Manchester-II code for the self-clocked transmission of signals; every 'zero' is represented by LOW-to-HIGH transition, and 'one' represented by HIGH-to-LOW transition, in the middle of the bit time.

### 7.3 DPCD registers

DPCD registers that are part of the VESA DisplayPort v1.1a are described in detail in [Ref. 1](#). The following paragraphs only describe the specific implementation by PTN3392.

The PTN3392 DisplayPort receiver capability and status information about the link are reported by DisplayPort Configuration Data (DPCD) registers, when a DisplayPort source issues a read command on the AUX CH. The DisplayPort source device can also write to the link configuration field of DPCD to configure and initialize the link. The DPCD is DisplayPort v1.1a compliant.

It is the responsibility of the host to only issue commands within the capability of the PTN3392 as defined in the ‘Receiver Capability Field’ in order to prevent undefined behavior. PTN3392 specific DPCD registers are listed in [Table 4](#).

#### 7.3.1 PTN3392 specific DPCD register settings

Table 4. PTN3392 specific DPCD registers

DPCD register <a href="#">[1]</a>	Description	Power-on Reset value	Read/write over AUX CH
<b>Receiver Capability Field</b>			
0000Bh	RECEIVE_PORT1_CAP_1. ReceiverPort1 Capability_1.	00h	read only
0000Ch	I <sup>2</sup> C-bus speed control capabilities bit map. The bit values in this register are assigned to I <sup>2</sup> C-bus speeds as follows: Bits 7:0 0000 0001b = 1 kbit/s; supported by PTN3392 0000 0010b = 3 kbit/s; supported by PTN3392 0000 0100b = 10 kbit/s; supported by PTN3392 0000 1000b = 100 kbit/s; supported by PTN3392 0001 0000b = 400 kbit/s; not supported by PTN3392 0010 0000b = 1 Mbit/s; not supported by PTN3392 0100 0000b = reserved 1000 0000b = 50 kbit/s; supported by PTN3392BS/F3 1000 0000b = reserved in PTN3392BS/F1, PTN3392BS/F2	8Fh	read only

Table 4. PTN3392 specific DPCD registers ...continued

DPCD register [1]	Description	Power-on Reset value	Read/write over AUX CH
<b>Link Configuration Field</b>			
00109h	<p>I<sup>2</sup>C-bus speed control/status bit map. Bit values in this register are assigned to I<sup>2</sup>C-bus speeds as follows:</p> <p>Bits 7:0</p> <p>0000 0001b = 1 kbit/s; supported by PTN3392</p> <p>0000 0010b = 3 kbit/s; supported by PTN3392</p> <p>0000 0100b = 10 kbit/s; supported by PTN3392</p> <p>0000 1000b = 100 kbit/s; supported by PTN3392</p> <p>0001 0000b = 400 kbit/s; not supported by PTN3392</p> <p>0010 0000b = 1 Mbit/s; not supported by PTN3392</p> <p>0100 0000b = reserved</p> <p>1000 0000b = 50 kbit/s; supported by PTN3392BS/F3</p> <p>1000 0000b = reserved in PTN3392BS/F1, PTN3392BS/F2</p> <p>Default value: 1000 0000b (50 kbit/s) for PTN3392BS/F3</p> <p>Default value: 0000 1000b (100 kbit/s) for PTN3392BS/F1, PTN3392BS/F2</p> <p>See also behavior of pin S2 in <a href="#">Table 3</a>.</p>	S2 setting	read/write
<b>Automated testing sub-field (optional)</b>			
00218h to 0027Fh	Not supported.		
<b>Branch device-specific field</b>			
00500h	BRANCH_IEEE_OUI 7:0 Branch vendor 24-bit IEEE OUI. NXP OUI = 00	00h	read only
00501h	BRANCH_IEEE_OUI 15:8 NXP OUI = 60	60h	read only
00502h	BRANCH_IEEE_OUI 23:16 NXP OUI = 37	37h	read only
00503h	ID string = 3392N2	33h	read only
00504h		33h	read only
00505h		39h	read only
00506h		32h	read only
00507h		4Eh	read only
00508h		32h	read only
00509h	Hardware revision level v1.2	12h	read only
0050Ah, 0050Bh	Major revision level (example: <b>v1.38</b> ), Minor revision level (example: v1. <b>38</b> )	01h, 26h	read only
0050Ch to 005FFh	RESERVED		read only

[1] Byte fields that are not explicitly listed are by definition reserved ('RES') and their default value is 0h.

## 7.3.2 I<sup>2</sup>C over AUX CH registers

### 7.3.2.1 I<sup>2</sup>C-bus speed control register (read only, 0000Ch)

Bit or bits are set to indicate I<sup>2</sup>C-bus speed control capabilities.

DisplayPort source reads register 0000Ch and sets the I<sup>2</sup>C-bus speed according to the DPCD register 00109h setting. The PTN3392 then adapts its I<sup>2</sup>C-bus bit rate to the speed set by the DisplayPort source.

### 7.3.2.2 I<sup>2</sup>C-bus speed control/status register (read/write, 00109h)

Bit values in this register are assigned to I<sup>2</sup>C-bus speeds.

Prior to software writing to this register, PTN3392 defaults to the I<sup>2</sup>C-bus speed (either 50 kbit/s or 10 kbit/s) selected by the S2 pin ([Table 3](#)).

On read, the PTN3392 returns a value set to indicate the speed currently in use.

On write, software provides a mask to limit the speeds to be enabled:

- The PTN3392 uses the slowest speed enabled by the mask and the PTN3392 speed capabilities.
- If the result of the mask with the speed capabilities is 0000 0000b, then the PTN3392 keeps the S2 setting I<sup>2</sup>C-bus speed that it is using before the software write (i.e., no change).

Some specific examples are listed below for clarification purposes:

- If the source writes 1111 1111b, the PTN3392 uses the lowest speed of 1 kbit/s.
- If the source writes 0000 1100b, the PTN3392 uses the lower of 10 kbit/s and 100 kbit/s, i.e., 10 kbit/s.
- If the source writes 0011 0000b, the PTN3392 would stay using the same I<sup>2</sup>C-bus speed that it is using before the software write (i.e., no change).

For DDC communication, the PTN3392 generates defer responses to the source while the I<sup>2</sup>C-bus transfer is taking place as specified in the *DisplayPort standard v1.1a*. Note that when the I<sup>2</sup>C-bus bit rate is set to 1 kbit/s, each bit takes 1 ms. One byte including I<sup>2</sup>C\_ACK takes 9 ms. Given this, the DisplayPort source should expect over 20 I<sup>2</sup>C\_DEFER's when requesting to read a byte over I<sup>2</sup>C-bus at the slowest rate.

### 7.4 Monitor detection

The PTN3392 assumes 75 Ω double termination, as shown in [Figure 6](#). The load sensing circuit of the PTN3392 senses a 37.5 Ω or 75 Ω termination respectively, when the monitor is connected or disconnected. The load-sensing circuit is active during the vertical blanking period (never during the horizontal retrace period), so that there is no disturbance to the screen image caused by the load-sensing circuit.

Upon detection of an RGB monitor being connected, the PTN3392 dynamically updates DPCD register 00200h and 00204h, to indicate the presence of a sink device being connected (see [Section 7.3](#)). After updating the DPCD register 00200h, the PTN3392 generates an IRQ request on HPD.

The PTN3392 implements two different ways to handle the HPD signal. The HPD behavior is governed by the S0 pin value after the reset and initialization sequence is completed (see [Figure 3](#)).

- If S0 is tied LOW, HPD is driven HIGH irrespective of whether a VGA monitor is detected.
- If S0 pin is tied HIGH, HPD is only driven HIGH when a monitor is detected.

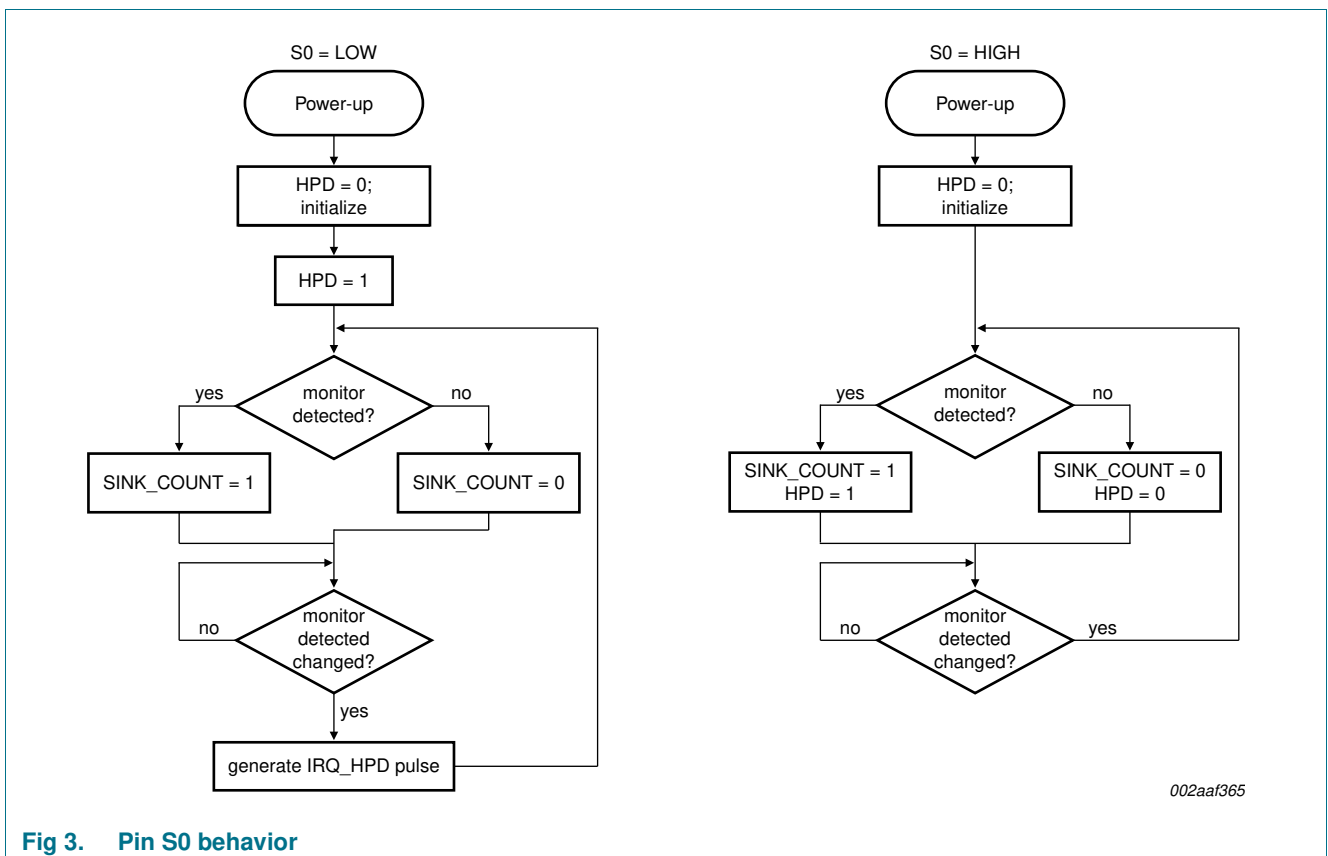


Fig 3. Pin S0 behavior

**7.4.1 S0 = logic 0**

If S0 is left open-circuit (internal pull-down) (DisplayPort v1.1a compliant behavior), PTN3392 behaves as stated in *VESA DisplayPort v1.1a*, sections 7 and 8. PTN3392 will keep HPD LOW during its internal initialization sequence after power-up. It will then update DPCD register SINK\_COUNT to the expected value, depending if a VGA monitor is detected or not, and will then assert HPD HIGH whatever is the value of SINK\_COUNT register. Each time PTN3392 detects a change in the VGA monitor connection status, it updates the SINK\_COUNT register accordingly, set DOWNSTREAM\_PORT\_STATUS\_CHANGED register bit to 1 and generate IRQ\_HPDPulse to signal the source about the status change. Refer to [Figure 3](#), S0 = LOW flowchart.

**7.4.2 S0 = logic 1**

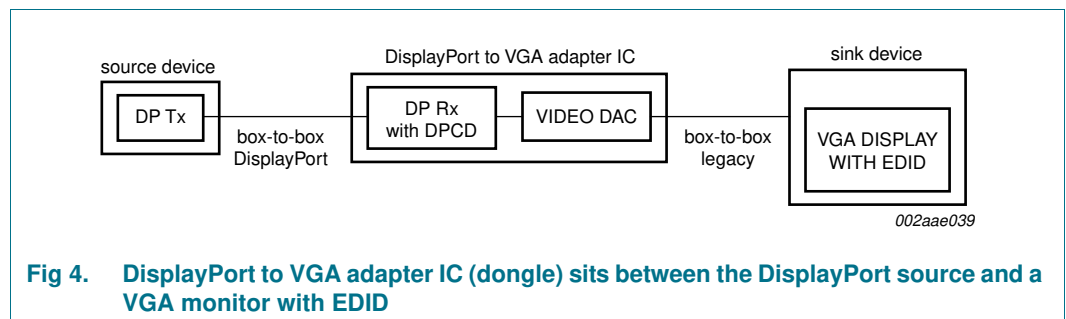
If S1 is tied to HIGH with external pull-up (best interoperability behavior), the PTN3392 will keep HPD LOW during its internal initialization sequence after power-up. It then waits for a VGA monitor to be connected downstream before asserting HPD HIGH to force source waiting for a VGA monitor before starting protocol negotiations. If a VGA monitor is disconnected during normal operations, PTN3392 asserts HPD LOW so that the source considers that no sink device is connected anymore. Refer to [Figure 3](#), S0 = HIGH flowchart.

**7.5 EDID handling**

[Figure 4](#) shows a DisplayPort-to-analog video converter (or dongle) situated between the DisplayPort source and a VGA monitor. The PTN3392 converts a DP I<sup>2</sup>C Over AUX request to I<sup>2</sup>C on the monitor's DDC bus. The monitor's EDID read data is then returned to the DP source via an I<sup>2</sup>C Over AUX response issued by the PTN3392.

It is the responsibility of the source to choose only video modes which are declared in the EDID and to adjust the DisplayPort link capabilities (link rate and lane count) to provide the necessary video bandwidth. The PTN3392 does not cache or modify the EDID to match the capabilities of the DisplayPort link data.

If the DisplayPort source drives display modes that are not specified in the EDID mode list, the PTN3392 does not detect such conditions, and displays at its output what it is presented by the DisplayPort source.



**Fig 4. DisplayPort to VGA adapter IC (dongle) sits between the DisplayPort source and a VGA monitor with EDID**

## 7.6 Triple 8-bit video DACs and VGA outputs

The triple 8-bit video DACs output a 700 mV (peak-to-peak) analog video output signal into 37.5  $\Omega$  load, as is the case of a doubly terminated 75  $\Omega$  cable. The DAC is capable of supporting the maximum pixel rate supported by a two-lane DP link (240 MHz).

The PTN3392 generates the RGB video timing and synchronization signals, RGB signals are then sent to the DACs for conversion to analog signals.

### 7.6.1 DAC reference resistor

An external reference resistor must be connected between pin RSET and analog ground. This resistor sets the reference current which determines the analog output level, and is specified as 1.2 k $\Omega$  with a 1 % tolerance. This value allows a 0.7 V (peak-to-peak) output into a 37.5  $\Omega$  load, such as a double-terminated 75  $\Omega$  coaxial cable.

## 8. Power-up and reset

PTN3392 has built-in power-on reset circuitry which automatically sequences the part through reset and initialization.

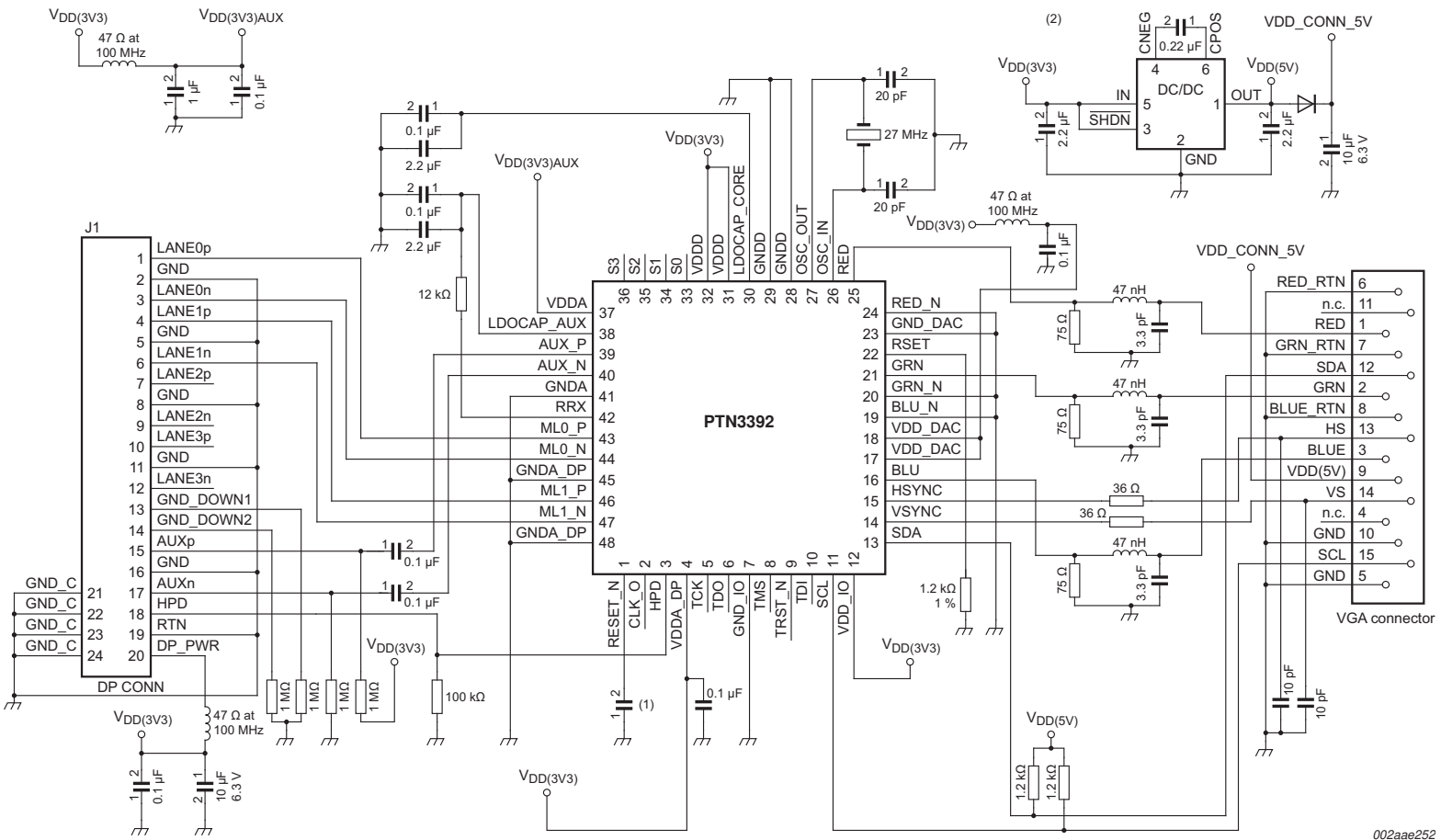
For proper behavior, a capacitor should be connected from the RESET\_N pin to ground to slow down the internal reset pulse; 1  $\mu$ F capacitance is recommended.

Before link is established, the PTN3392 holds VSYNC and HSYNC signals LOW and blanks the RGB signals.

While the PTN3392 performs initialization,

- The HPD signal is driven LOW, to indicate to the DisplayPort source that the PTN3392 is not ready for link communication
- The RED, GRN, BLU and complementary outputs (RED\_N, GRN\_N, BLU\_N) are disabled
- The VSYNC and HSYNC outputs are driven LOW

9. Application design-in information



002aae252

- (1) 1  $\mu$ F is recommended.
- (2) Example of external DC-to-DC regulator.

Fig 5. Application diagram



## 9.1 Display resolution

[Table 5](#) lists some example display resolutions and clock rates that PTN3392 supports. (Refer to [Footnote 1 on page 2.](#))

**Table 5.** Display resolution and pixel clock rate<sup>[1]</sup>

Display type	Active video		Total frame		Bits per pixel	Vertical frequency (Hz)	Pixel clock (MHz)	Data rate (Gbit/s)	Standard type
	Horizontal	Vertical	Horizontal total (pixel)	Vertical total (line)					
VGA	640	480	800	525	24	59.94	25.175	0.76	Industry standard
SVGA	800	600	1056	628	24	60.317	40.000	1.20	VESA guidelines
XGA	1024	768	1344	806	24	60.004	65.000	1.95	VESA guidelines
XGA+	1152	864	1600	900	24	75	108.000	3.24	VESA standard
HD	1360	768	1792	795	24	60.015	85.500	2.56	VESA standard
HD/WXGA	1366	768	1792	798	24	59.79	85.501	2.57	VESA standard
HD/WXGA	1280	720	1650	750	24	60	74.250	2.23	CEA standard
WXGA	1280	800	1680	831	24	59.81	83.500	2.50	CVT
WXGA	1280	800	1696	838	24	74.934	106.500	3.19	CVT
WXGA	1280	800	1712	843	24	84.88	122.500	3.68	CVT
SXGA-	1280	960	1800	1000	24	60	108.000	3.24	VESA standard
SXGA	1280	1024	1688	1066	24	60.02	108.000	3.24	VESA standard
SXGA	1280	1024	1688	1066	24	75.025	135.001	4.05	VESA standard
SXGA	1280	1024	1728	1072	24	85.024	157.500	4.72	VESA standard
SXGA+	1400	1050	1864	1089	24	59.978	121.749	3.65	CVT
WXGA+	1440	900	1904	934	24	59.887	106.499	3.19	CVT
HD+	1600	900	1800	1000	24	60	108.000	3.24	VESA standard
UXGA	1600	1200	2160	1250	24	60	162.000	4.86	VESA standard
UXGA	1600	1200	2160	1250	24	65	175.500	5.27	VESA standard
WSXGA+	1680	1050	2240	1089	24	59.954	146.249	4.39	CVT
FHD	1920	1080	2200	1125	24	60	148.500	4.46	CEA standard
WUXGA	1920	1200	2592	1245	18	59.885	193.251	4.35	CVT
WUXGA	1920	1200	2080	1235	24	59.95	154.000	4.62	CVT RB
	1920	1440	2600	1500	18	60	234.000	5.27	CVT RB
QWXGA	2048	1152	2250	1200	24	60	162.000	4.86	VESA standard
QXGA	2048	1536	2144	1555	24	49.266	164.249	4.93	CVT

[1] Contact NXP team for other monitor timings not listed in this table.

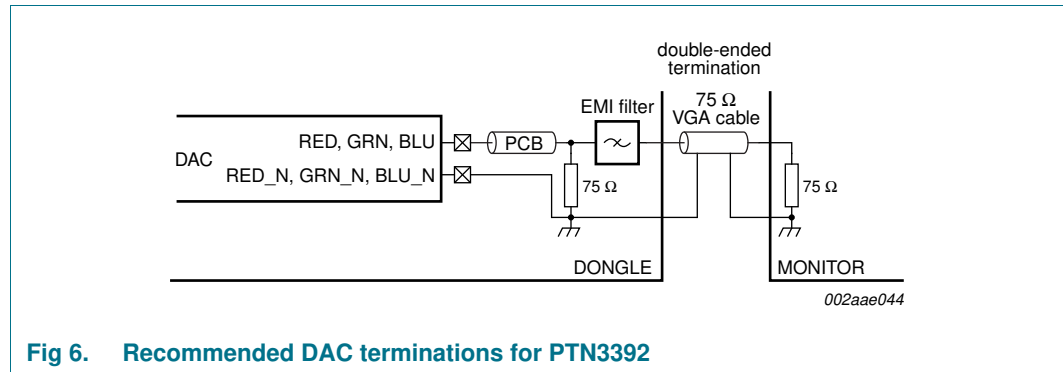
The available bandwidth over a 2-lane HBR DisplayPort v1.1a link limits pixel clock rate support to:

- 240 MHz at 6 bpc
- 180 MHz at 8 bpc

### 9.2 Power supply filter

All supply pins can be tied to a single 3.3 V power source. Sufficient decoupling capacitance to ground should be connected from each  $V_{DD}$  pin directly to ground to filter supply noise. (Refer to [Figure 5 “Application diagram”](#).)

### 9.3 DAC terminations



**Fig 6. Recommended DAC terminations for PTN3392**

We recommend the DAC outputs to use 75  $\Omega$  double termination. [Figure 6](#) shows an example of VGA dongle application. A 75  $\Omega$  termination is used to terminate inside the dongle, and another 75  $\Omega$  termination is typically used inside the RGB monitor. The load sensing mechanism assumes this double termination.

## 10. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA}$	analog supply voltage		-0.3	+3.8	V
$V_{DDD}$	digital supply voltage		-0.3	+4.6	V
$V_i$	input voltage	3.3 V CMOS inputs	-0.3	$V_{DD} + 0.5$	V
$T_{stg}$	storage temperature		-65	+150	$^{\circ}C$
$V_{ESD}$	electrostatic discharge voltage	HBM	[1]	7000	V
		CDM	[2]	1000	V
		IEC contact discharge to signal pins (to GND)	[3]	8000	V

- [1] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.
- [2] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.
- [3] IEC 61000-4-2, Level 4 ([Ref. 4](#)).

## 11. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DDA</sub>	analog supply voltage		3.0	3.3	3.6	V
V <sub>DD</sub>	digital supply voltage		3.0	3.3	3.6	V
V <sub>I</sub>	input voltage	3.3 V CMOS inputs	0	3.3	3.6	V
		SDA and SCL inputs with respect to ground	0	5	5.5	V
V <sub>I(AV)</sub>	average input voltage	DC value at ML_LANE0+, ML_LANE0-, ML_LANE1+, ML_LANE1-, AUX_CH+, AUX_CH- inputs <a href="#">[1]</a>	-	0	-	V
R <sub>ext(RSET)</sub>	external resistance on pin RSET	between RSET (pin 22) and GND	-	1.2 ± 1 %	-	kΩ
T <sub>amb</sub>	ambient temperature	commercial grade	0	-	85	°C

[1] Input signals to these pins must be AC-coupled.

## 12. Characteristics

### 12.1 Current consumption, power dissipation and thermal characteristics

Table 8. Current consumption, power dissipation and thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>DD</sub>	supply current	normal operation, UXGA / 162 MHz pixel clock	-	180	-	mA
I <sub>DD(stb)</sub>	standby supply current	Standby mode	-	12	-	mA
P	power dissipation	normal operation, UXGA / 162 MHz pixel clock	-	600	-	mW
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air for SOT619-1	-	35	-	K/W
R <sub>PU</sub>	pull-up resistance	RESET_N pin; 0 V ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	44	66	95	kΩ
R <sub>pd</sub>	pull-down resistance	S0 to S3 pins; 0 V ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	44	66	95	kΩ

## 12.2 DisplayPort receiver main link

**Table 9. DisplayPort receiver main link characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UI	unit interval	for high bit rate (2.7 Gbit/s per lane) <a href="#">[1]</a>	-	370	-	ps
		for low bit rate (1.62 Gbit/s per lane) <a href="#">[1]</a>	-	617	-	ps
$\Delta f_{\text{DOWN\_SPREAD}}$	link clock down spreading	<a href="#">[2]</a>	0.0	-	0.5	%
$V_{\text{RX\_DIFFp-p}}$	differential input peak-to-peak voltage	at RX package pins				
		for high bit rate <a href="#">[3]</a>	120	-	-	mV
		for reduced bit rate <a href="#">[3]</a>	40	-	-	mV
$t_{\text{RX\_EYE\_CONN}}$	receiver eye time at RX-side connector pins	for high bit rate <a href="#">[4]</a>	0.51	-	-	UI
		for reduced bit rate <a href="#">[4][5]</a>	0.25	-	-	UI
$t_{\text{RX\_EYE\_CHIP}}$	receiver eye time at RX package pins	for high bit rate <a href="#">[4]</a>	0.47	-	-	UI
		for reduced bit rate <a href="#">[4][5]</a>	0.22	-	-	UI
$t_{\text{RX\_EYE\_m-mJT\_CHP}}$	time between jitter median and maximum median deviation (package pins)	for high bit rate <a href="#">[4]</a>	-	-	0.265	UI
		for reduced bit rate <a href="#">[4][5]</a>	-	-	0.39	UI
$V_{\text{RX\_DC\_CM}}$	RX DC common mode voltage	<a href="#">[6]</a>	0	-	2.0	V
$I_{\text{RX\_SHORT}}$	RX short-circuit current limit	<a href="#">[7]</a>	-	-	50	mA
$L_{\text{RX\_SKEW}}$	total skew	inter-pair; lane-to-lane skew at RX package pins <a href="#">[8]</a>	-	-	5200	ps
		lane intra-pair skew at RX package pins;				
		for high bit rate <a href="#">[9]</a>	-	-	100	ps
		for reduced bit rate <a href="#">[9]</a>	-	-	300	ps
$f_{\text{RX\_TRACKING\_BW}}$	jitter tracking bandwidth	<a href="#">[10]</a>	20	-	-	MHz

[1] Range is nominal  $\pm 350$  ppm. DisplayPort link RX does not require local crystal for link clock generation.

[2] Up to 0.5 % down spread is supported. Modulation frequency range of 30 kHz to 33 kHz must be supported.

[3] Informative; refer to [Figure 7](#) for definition of differential voltage.

[4]  $t_{\text{RX\_EYE\_m-mJT\_CHP}}$  specifies the total allowable Deterministic Jitter (DJ).

[5]  $1 - t_{\text{RX\_EYE\_CONN}}$  specifies the allowable Total Jitter (TJ).

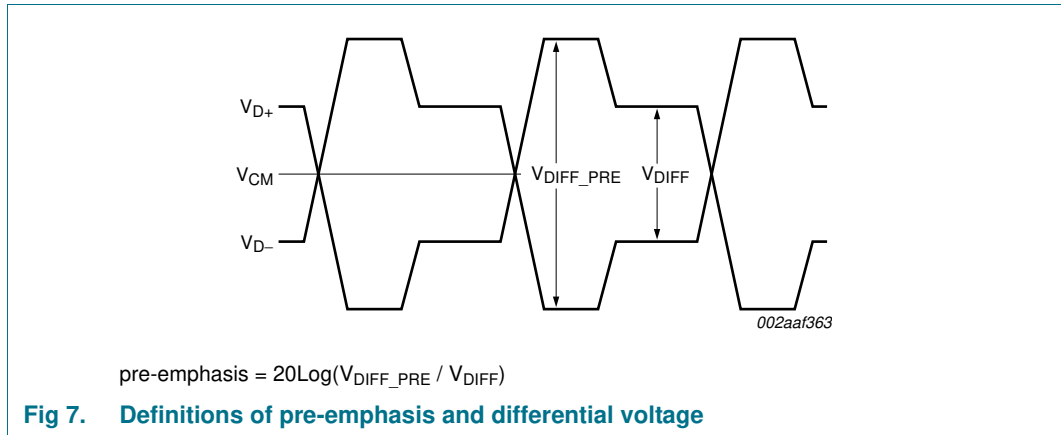
[6] Common mode voltage is equal to  $V_{\text{bias\_RX}}$  voltage.

[7] Total drive current of the input bias circuit when it is shorted to its ground.

[8] Maximum skew limit between different RX lanes of a DisplayPort link.

[9] Maximum skew limit between D+ and D- of the same lane.

[10] Minimum CDR tracking bandwidth at the receiver when the input is repetition of D10.2 symbols without scrambling.



### 12.3 DisplayPort receiver AUX CH

**Table 10. DisplayPort receiver AUX CH characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UI	unit interval	AUX	[1] 0.4	0.5	0.6	μs
N <sub>PRECHARGE_PULSES</sub>	number of precharge pulses		[2] 10	-	16	
t <sub>AUX_BUS_PARK</sub>	AUX CH bus park time		[3] 10	-	-	ns
t <sub>jitter(cc)</sub>	cycle-to-cycle jitter time	transmitting device	[4] -	-	0.04	UI
		receiving device	[5] -	-	0.05	UI
V <sub>AUX_DIFFp-p</sub>	AUX differential peak-to-peak voltage	transmitting device	[6] 0.39	-	1.38	V
		receiving device	[6] 0.32	-	1.36	V
R <sub>AUX_TERM(DC)</sub>	AUX CH termination DC resistance	informative	-	100	-	Ω
V <sub>AUX_DC_CM</sub>	AUX DC common-mode voltage		[7] 0	-	2.0	V
V <sub>AUX_TURN_CM</sub>	AUX turnaround common-mode voltage		[8] -	-	0.4	V
I <sub>AUX_SHORT</sub>	AUX short-circuit current limit		[9] -	-	90	mA
C <sub>AUX</sub>	AUX AC coupling capacitor		[10] 75	-	200	nF

- [1] Results in the bit rate of 1 Mbit/s including the overhead of Manchester II coding.
- [2] Each pulse is a '0' in Manchester II code.
- [3] Period after the AUX CH STOP condition for which the bus is parked.
- [4] Maximum allowable UI variation within a single transaction at connector pins of a transmitting device. Equal to 24 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.
- [5] Maximum allowable UI variation within a single transaction at connector pins of a receiving device. Equal to 30 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.
- [6]  $V_{\text{AUX\_DIFFp-p}} = 2 \times |V_{\text{AUX+}} - V_{\text{AUX-}}|$ .
- [7] Common-mode voltage is equal to V<sub>bias\_TX</sub> (or V<sub>bias\_RX</sub>) voltage.
- [8] Steady-state common-mode voltage shift between transmit and receive modes of operation.
- [9] Total drive current of the transmitter when it is shorted to its ground.
- [10] The AUX CH AC coupling capacitor placed both on the DisplayPort source and sink devices.

## 12.4 HPD characteristics

Table 11. HPD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Output characteristics</b>						
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = 2 mA	2	-	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = -2 mA	-	-	0.8	V
I <sub>OSH</sub>	HIGH-level short-circuit output current	drive HIGH; cell connected to ground	-	-	129	mA
I <sub>OSL</sub>	LOW-level short-circuit output current	drive LOW; cell connected to V <sub>DD</sub>	-	-	126	mA

## 12.5 DDC characteristics

Table 12. DDC characteristics

V<sub>CC</sub> = 4.5 V to 5.5 V.<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input characteristics</b>						
V <sub>IH</sub>	HIGH-level input voltage		2	-	5.5	V
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.8	V
V <sub>I(hys)</sub>	hysteresis of input voltage		0.1 × V <sub>DD</sub>	-	-	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V	-	-	±1	μA
<b>Output characteristics</b>						
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3.0	-	-	mA
I <sub>O(sc)</sub>	short-circuit output current	drive LOW; cell connected to V <sub>DD</sub>	-	-	40.0	mA
C <sub>io</sub>	input/output capacitance	V <sub>I</sub> = 3 V or 0 V; V <sub>DD</sub> = 3.3 V	-	6	7	pF
		V <sub>I</sub> = 3 V or 0 V; V <sub>DD</sub> = 0 V	-	6	7	pF

[1] V<sub>CC</sub> is the pull-up voltage for DDC.

## 12.6 DAC

Table 13. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N <sub>res(DAC)</sub>	DAC resolution		-	-	8	bit
f <sub>clk</sub>	clock frequency		-	-	240	MHz
ΔI <sub>o(DAC)</sub>	DAC output current variation	DAC-to-DAC	-	-	4	%
INL	integral non-linearity		-1	±0.5	+1	LSB
DNL	differential non-linearity		-1	-	+1	LSB
V <sub>o(DAC)</sub>	DAC output voltage		0	-	1.25	V
C <sub>o(DAC)</sub>	DAC output capacitance		-	3.5	-	pF
α <sub>ct(DAC)</sub>	DAC crosstalk	between DAC outputs	-	-54	-	dB

## 12.7 HSYNC, VSYNC characteristics

Table 14. HSYNC and VSYNC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Output characteristics</b>						
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = 8 mA	2	-	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = -8 mA	-	-	0.8	V
I <sub>OSH</sub>	HIGH-level short-circuit output current	drive HIGH; cell connected to ground [1]	-	-	129.0	mA
I <sub>OSL</sub>	LOW-level short-circuit output current	drive LOW; cell connected to V <sub>DD</sub> [1]	-	-	126.0	mA

[1] The parameter values specified are simulated and absolute values.

## 12.8 Strap pins S[3:0]

Table 15. Strap pins S[3:0] characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input characteristics</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.7 × V <sub>DD</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage				0.3 × V <sub>DD</sub>	V
<b>Weak pull-down characteristics</b>						
I <sub>pd</sub>	pull-down current	V <sub>I</sub> = V <sub>DD</sub>	25.0	50.0	95.0	μA

## 12.9 JTAG and RESET\_N

Table 16. JTAG and RESET\_N characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input characteristics</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.7 × V <sub>DD</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage				0.3 × V <sub>DD</sub>	V
<b>Output characteristics</b>						
V <sub>OH</sub>	HIGH-level output voltage	RESET_N; I <sub>OH</sub> = 4 mA	2	-	-	V
		JTAG; I <sub>OH</sub> = 2 mA	2	-	-	V
V <sub>OL</sub>	LOW-level output voltage	RESET_N; I <sub>OL</sub> = -4 mA	-	-	0.8	V
		JTAG; I <sub>OL</sub> = -2 mA	-	-	0.8	V

### 13. Package outline

**HVQFN48: plastic thermal enhanced very thin quad flat package; no leads;**  
**48 terminals; body 7 x 7 x 0.85 mm**

SOT619-1

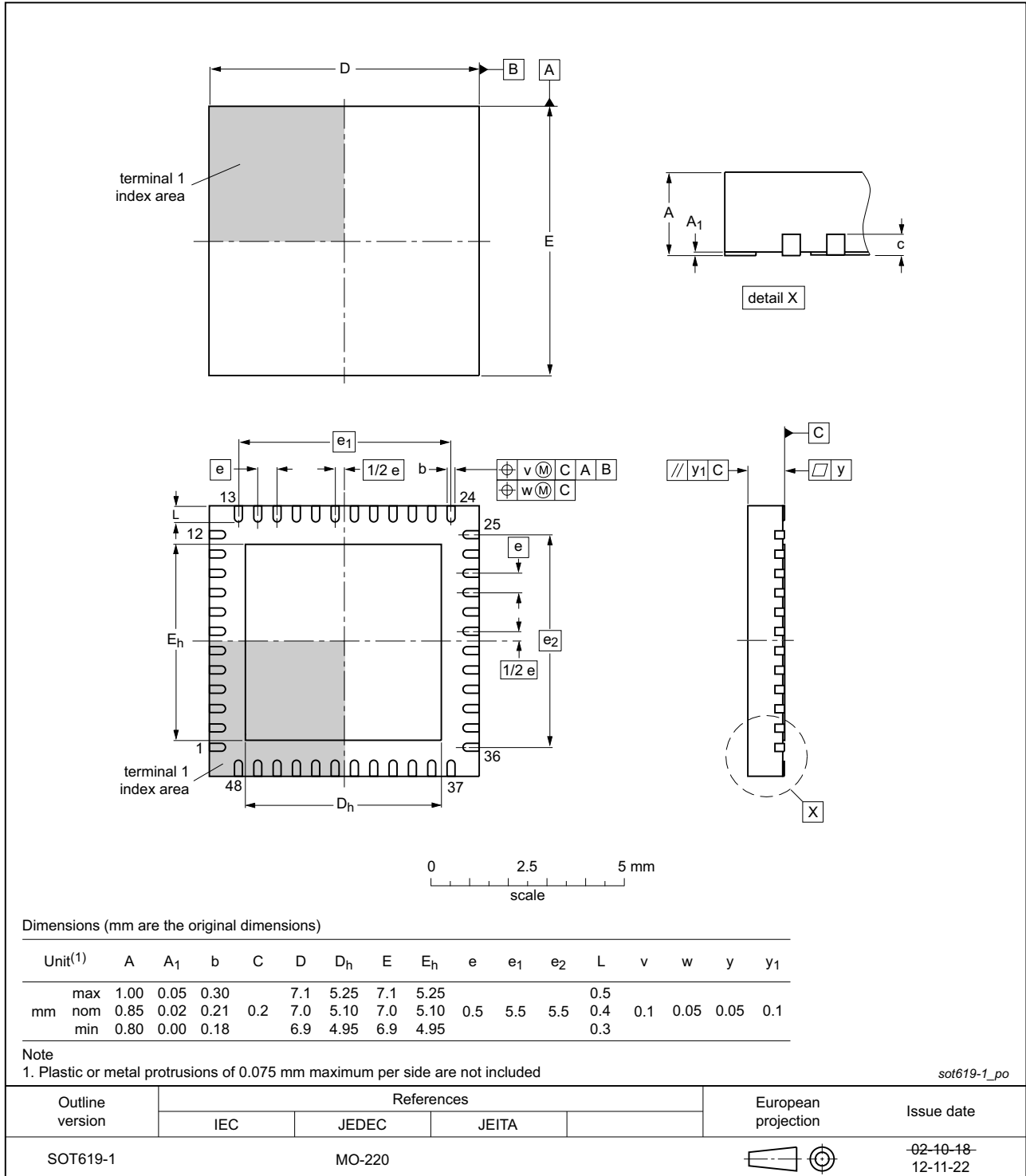


Fig 8. Package outline SOT619-1 (HVQFN48)



## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 9](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 17](#) and [18](#)

**Table 17. SnPb eutectic process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 18. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 9](#).