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PTN3460

eDP to LVDS bridge IC

Rev. 4 — 12 March 2014 Product data sheet

1. General description

PTN3460 is an (embedded) DisplayPort to LVDS bridge device that enables connectivity between an (embedded) DisplayPort (eDP) source and LVDS display panel. It processes the incoming DisplayPort (DP) stream, performs DP to LVDS protocol conversion and transmits processed stream in LVDS format.

PTN3460 has two high-speed ports: Receive port facing DP Source (for example, CPU/GPU/chip set), Transmit port facing the LVDS receiver (for example., LVDS display panel controller). The PTN3460 can receive DP stream at link rate 1.62 Gbit/s or 2.7 Gbit/s and it can support 1-lane or 2-lane DP operation. It interacts with DP source via DP Auxiliary (AUX) channel transactions for DP link training and setup.

It supports single bus or dual bus LVDS signaling with color depths of 18 bits per pixel or 24 bits per pixel and pixel clock frequency up to 112 MHz. The LVDS data packing can be done either in VESA or JEIDA format. Also, the DP AUX interface transports I^2C-over-AUX commands and support EDID-DDC communication with LVDS panel. To support panels without EDID ROM, the PTN3460 can emulate EDID ROM behavior avoiding specific changes in system video BIOS.

PTN3460 provides high flexibility to optimally fit under different platform environments. It supports three configuration options: multi-level configuration pins, DP AUX interface, and I^2C-bus interface.

PTN3460 can be powered by either 3.3 V supply only or dual supplies (3.3 V/1.8 V) and is available in the HVQFN56 7 mm × 7 mm package with 0.4 mm pitch.

2. Features and benefits

2.1 Device features

- Embedded microcontroller and on-chip Non-Volatile Memory (NVM) allow for flexibility in firmware updates
- LVDS panel power-up (/down) sequencing control
- Firmware controlled panel power-up (/down) sequence timing parameters
- No external timing reference needed
- EDID ROM emulation to support panels with no EDID ROM
  - Supports EDID structure v1.3
  - On-chip EDID emulation up to seven different EDID data structures
- eDP complying PWM signal generation or PWM signal pass through from eDP source

2.2 DisplayPort receiver features

- Compliant to DP v1.2 and v1.1a
- Compliant to eDP v1.2 and v1.1
- Supports Main Link operation with 1 or 2 lanes (default mode is 2-lane operation)
- Supports Main Link rate: Reduced Bit Rate (1.62 Gbit/s) and High Bit Rate (2.7 Gbit/s)
- Supports 1 Mbit/s AUX channel
  - Supports Native AUX and I^2C-over-AUX transactions
- Supports down spreading to minimize EMI
- Integrated 50 Ω termination resistors provide impedance matching on both Main Link lanes and AUX channel
- High performance Auto Receive Equalization enabling optimal channel compensation, device placement flexibility and power saving at CPU/GPU
- Supports eDP authentication options: Alternate Scrambler Seed Reset (ASSR) and Alternate Framing
- Supports Fast Link training and Full Link training
- Supports DisplayPort symbol error rate measurements

2.3 LVDS transmitter features

- Compatible with ANSI/TIA/EIA-644-A-2001 standard
- Supports RGB data packing as per JEIDA and VESA data formats
- Supports pixel clock frequency from 25 MHz to 112 MHz
- Supports single LVDS bus operation up to 112 mega pixels per second
- Supports dual LVDS bus operation up to 224 mega pixels per second
- Supports color depth options: 18 bpp, 24 bpp
- Programmable center spreading of pixel clock frequency to minimize EMI
- Supports 1920 × 1200 at 60 Hz resolution in dual LVDS bus mode
- Programmable LVDS signal swing to pre-compensate for channel attenuation or allow for power saving
- Supports PCB routing flexibility by programming for:
  - LVDS bus swapping
  - Channel swapping
  - Differential signal pair swapping
- Supports Data Enable polarity programming
- DDC control for EDID ROM access – I^2C-bus interface up to 400 kbit/s

2.4 Control and system features

- Device programmability
  - Multi-level configuration pins enabling wider choice
  - I^2C-bus slave interface supporting Standard-mode (100 kbit/s) and Fast-mode (400 kbit/s)
- Power management
  - Low-power state: DP AUX command-based Low-power mode (SET POWER)
  - Deep power-saving state via a dedicated pin

2.5 General

- Power supply: with on-chip regulator
  - 3.3 V ± 10 % (integrated regulator switched on)
  - 3.3 V ± 10 %, 1.8 V ± 5 % (integrated regulator switched off)
- ESD: 8 kV HBM, 1 kV CDM
- Operating temperature range: 0 °C to 70 °C
- HVQFN56 package 7 mm × 7 mm, 0.4 mm pitch; exposed center pad for thermal relief and electrical ground

3. Applications

- AIO platforms
- Notebook platforms
- Netbooks/net tops

4. System context diagram

Figure 1 illustrates the PTN3460 usage.

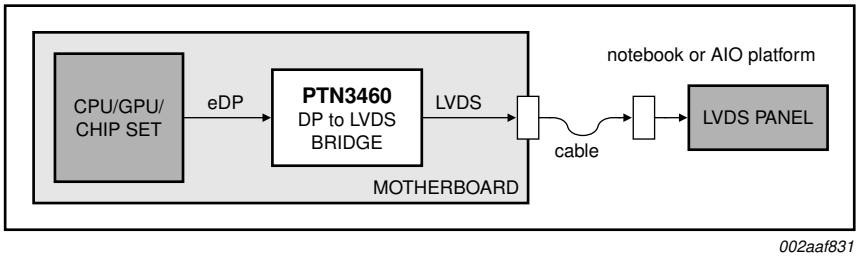


Fig 1. PTN3460 context diagram

5. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PTN3460BS/Fx[1][2]	PTN3460BS[3]	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 7 × 7 × 0.85 mm[4]; 0.4 mm pitch	SOT949-2

[1] PTN3460BS/Fx is firmware-specific, where the 'x' indicates the firmware version.

[2] Notes on firmware and marking:

a) Firmware versions are not necessarily backwards compatible.

b) Box/reel labels will indicate the firmware version via the orderable part number (for example, labeling will indicate PTN3460BS/F1 for firmware version 1). A sample label is illustrated in Figure 8.

[3] Topside marking is limited to PTN3460BS and will not indicate the firmware version.

[4] Maximum package height is 1 mm.

6. Block diagram

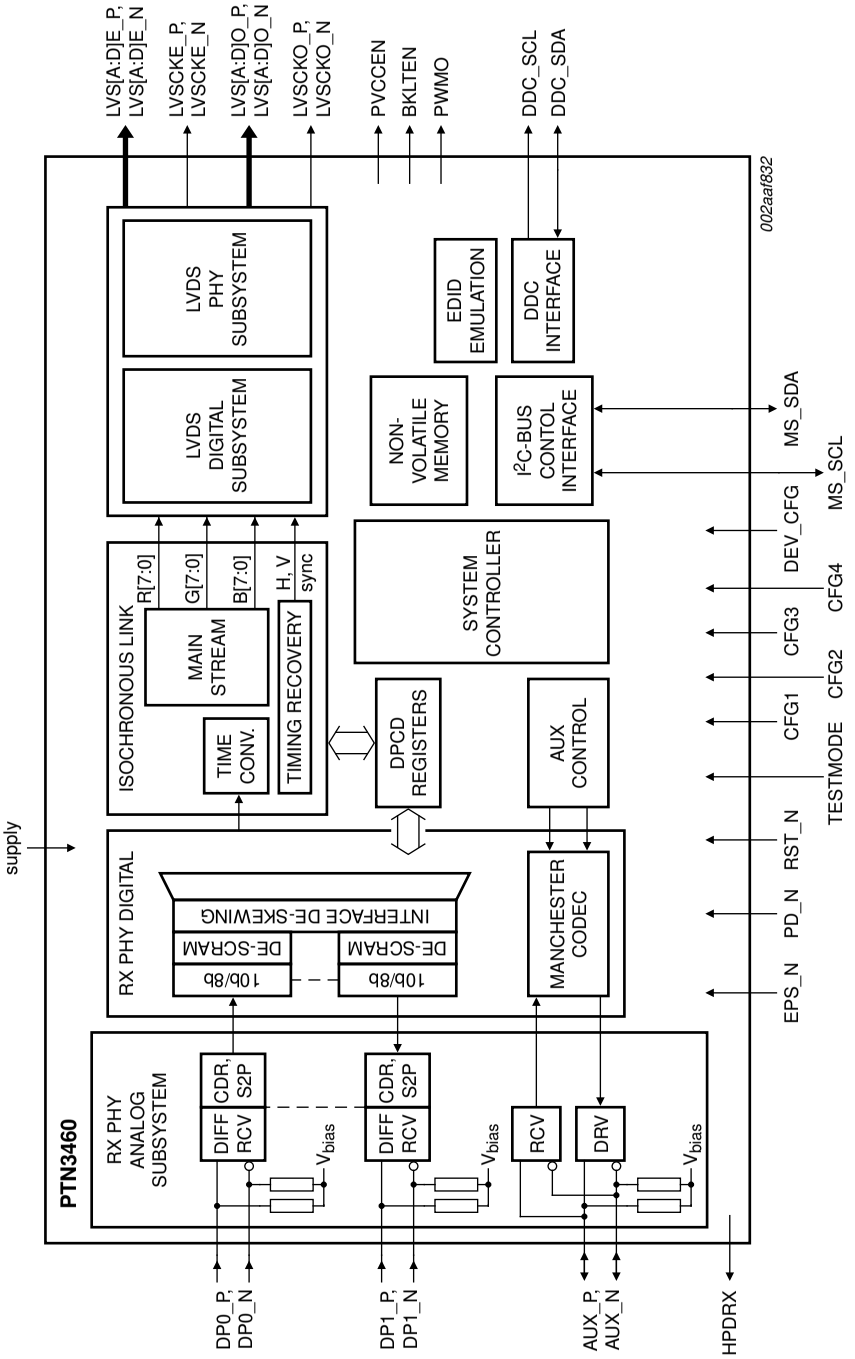
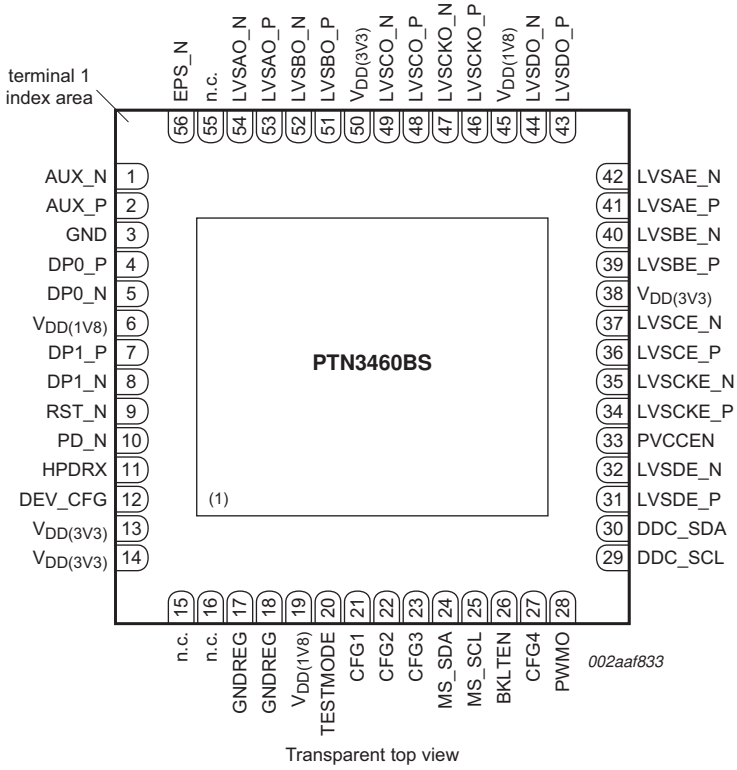


Fig 2. Block diagram of PTN3460

7. Pinning information

7.1 Pinning



(1) Center pad is connected to PCB ground plane for electrical grounding and thermal relief.

Fig 3. Pin configuration for HVQFN56

Refer to Section 13 “Package outline” for package and pin dimensions.

7.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
DisplayPort interface signals			
DP0_P	4	self-biasing differential input	Differential signal from DP source. DP0_P makes a differential pair with DP0_N. The input to this pin must be AC-coupled externally.
DP0_N	5	self-biasing differential input	Differential signal from DP source. DP0_N makes a differential pair with DP0_P. The input to this pin must be AC-coupled externally.
DP1_P	7	self-biasing differential input	Differential signal from DP source. DP1_P makes a differential pair with DP1_N. The input to this pin must be AC-coupled externally.
DP1_N	8	self-biasing differential input	Differential signal from DP source. DP1_N makes a differential pair with DP1_P. The input to this pin must be AC-coupled externally.
AUX_P	2	self-biasing differential I/O	Differential signal towards DP source. AUX_P makes a differential pair with AUX_N. The pin must be AC-coupled externally.
AUX_N	1	self-biasing differential I/O	Differential signal towards DP source. AUX_N makes a differential pair with AUX_P. The pin must be AC-coupled externally.
HPDRX	11	single-ended 3.3 V CMOS output	Hot Plug Detect signal to DP source.
LVDS interface signals			
LVSAE_P	41	LVDS output	Even bus, Channel A differential signal to LVDS receiver. LVSAE_P makes a differential pair with LVSAE_N.
LVSAE_N	42	LVDS output	Even bus, Channel A differential signal to LVDS receiver. LVSAE_N makes a differential pair with LVSAE_P.
LVSBE_P	39	LVDS output	Even bus, Channel B differential signal to LVDS receiver. LVSBE_P makes a differential pair with LVSBE_N.
LVSBE_N	40	LVDS output	Even bus, Channel B differential signal to LVDS receiver. LVSBE_N makes a differential pair with LVSBE_P.
LVSCE_P	36	LVDS output	Even bus, Channel C differential signal to LVDS receiver. LVSCE_P makes a differential pair with LVSCE_N.
LVSCE_N	37	LVDS output	Even bus, Channel C differential signal to LVDS receiver. LVSCE_N makes a differential pair with LVSCE_P.
LVSCKE_P	34	LVDS clock output	Even bus, clock differential signal to LVDS receiver. LVSCKE_P makes a differential pair with LVSCKE_N.
LVSCKE_N	35	LVDS clock output	Even bus, clock differential signal to LVDS receiver. LVSCKE_N makes a differential pair with LVSCKE_P.
LVSDE_P	31	LVDS output	Even bus, Channel D differential signal to LVDS receiver. LVSDE_P makes a differential pair with LVSDE_N.
LVSDE_N	32	LVDS output	Even bus, Channel D differential signal to LVDS receiver. LVSDE_N makes a differential pair with LVSDE_P.
LVSAO_P	53	LVDS output	Odd bus, Channel A differential signal to LVDS receiver. LVSAO_P makes a differential pair with LVSAO_N.
LVSAO_N	54	LVDS output	Odd bus, Channel A differential signal to LVDS receiver. LVSAO_N makes a differential pair with LVSAO_P.
LVSBO_P	51	LVDS output	Odd bus, Channel B differential signal to LVDS receiver. LVSBO_P makes a differential pair with LVSBO_N.
LVSBO_N	52	LVDS output	Odd bus, Channel B differential signal to LVDS receiver. LVSBO_N makes a differential pair with LVSBO_P.

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
LVSCO_P	48	LVDS output	Odd bus, Channel C differential signal to LVDS receiver. LVSCO_P makes a differential pair with LVSCO_N.
LVSCO_N	49	LVDS output	Odd bus, Channel C differential signal to LVDS receiver. LVSCO_N makes a differential pair with LVSCO_P.
LVSCKO_P	46	LVDS clock output	Odd bus, clock differential signal to LVDS receiver. LVSCKO_P makes a differential pair with LVSCKO_N.
LVSCKO_N	47	LVDS clock output	Odd bus, clock differential signal to LVDS receiver. LVSCKO_N makes a differential pair with LVSCKO_P.
LVSDO_P	43	LVDS output	Odd bus, Channel D differential signal to LVDS receiver. LVSDO_P makes a differential pair with LVSDO_N.
LVSDO_N	44	LVDS output	Odd bus, Channel D differential signal to LVDS receiver. LVSDO_N makes a differential pair with LVSDO_P.
DDC_SDA	30	open-drain DDC data I/O	DDC data signal connection to display panel. Pulled-up by external termination resistor (5 V tolerant).
DDC_SCL	29	open-drain DDC clock I/O	DDC clock signal connection to display panel. Pulled-up by external termination resistor (5 V tolerant).
Panel and backlight interface signals			
PVCCEN	33	CMOS output	Panel power (V_{CC}) enable output.
PWMO	28	CMOS output	PWM output signal to display panel.
BKLTEN	26	CMOS output	Backlight enable output.
Control interface signals			
PD_N	10	CMOS input	Chip power-down input (active LOW). If PD_N is LOW, then the device is in Deep power-down completely, even if supply rail is ON; for the device to be able to operate, the PD_N pin must be HIGH.
RST_N	9	CMOS input	Chip reset pin (active LOW); internally pulled-up. The pin is meant to reset the device and all its internal states/logic; all internal registers are taken to default value after RST_N is applied and made HIGH. If RST_N is LOW, the device stays in reset condition and for the device to be able to operate, RST_N must be HIGH.
DEV_CFG	12	CMOS I/O	I^2C-bus address/mode selection pin.
TESTMODE	20	CMOS input	If TESTMODE is left open or pulled HIGH, CFG[4:1] operate as JTAG pins. If TESTMODE is pulled LOW, these pins serve as configuration pins.
CFG1	21	input	Behavior defined by TESTMODE pin. If TESTMODE is left open or pulled HIGH, this pin functions as JTAG TEST CLOCK input. If TESTMODE is pulled LOW, this pin acts as configuration input.
CFG2	22	input	Behavior defined by TESTMODE pin. If TESTMODE is left open or pulled HIGH, this pin functions as JTAG MODE SELECT input. If TESTMODE is pulled LOW, this pin acts as configuration input.
CFG3	23	input	Behavior defined by TESTMODE pin. If TESTMODE is left open or pulled HIGH, this pin functions as JTAG TEST DATA INPUT. If TESTMODE is pulled LOW, this pin acts as configuration input.
CFG4	27	I/O	Behavior defined by TESTMODE pin value. If TESTMODE is left open or pulled HIGH, this pin functions as JTAG TEST DATA OUTPUT. If TESTMODE is pulled LOW, this pin acts as configuration input.

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
MS_SDA	24	open-drain (I^2C) data input/output	I^2C-bus data signal connection to I^2C-bus master or slave. Pulled up by external resistor.
MS_SCL	25	open-drain (I^2C) clock input/output	I^2C-bus clock signal connection to I^2C-bus master or slave. Pulled up by external resistor.
n.c.	55	-	not connected; reserved.
EPS_N	56	input	Can be left open or pulled HIGH for 3.3 V supply only option relying on internal regulator for 1.8 V generation. Should be pulled down to GND for dual supply (3.3 V/1.8 V) option.
Supply, ground and decoupling			
$V_{DD(3V3)}$	13, 14, 38, 50	power	3.3 V supply input.
$V_{DD(1V8)}$	6, 45	power	1.8 V supply input.
$V_{DD(1V8)}$	19	power	1.8 V regulator supply output.
n.c.	15, 16	power	Not connected.
GND	3	power	Ground.
GNDREG	17, 18	power	Ground for regulator.
GND	center pad	power	The center pad must be connected to motherboard GND plane for both electrical ground and thermal relief.

8. Functional description

PTN3460 is an (Embedded) DisplayPort to LVDS bridge IC that processes the incoming DisplayPort (DP) stream, performs DP to LVDS protocol conversion and transmits processed stream in LVDS format. Refer to Figure 2 “Block diagram of PTN3460”.

The PTN3460 consists of:

- DisplayPort receiver
- LVDS transmitter
- System control and operation

The following sections describe individual sub-systems and their capabilities in more detail.

8.1 DisplayPort receiver

PTN3460 implements a DisplayPort receiver consisting of 2-lane Main Link and AUX channel.

With its advanced signal processing capability, it can handle Fast Link training or Full Link training scheme. PTN3460 implements a high-performance Auto Receive Equalizer and Clock Data Recovery (CDR) algorithm, with which it identifies and selects an optimal operational setting for given channel environment. Given that the device is targeted primarily for embedded Display connectivity, both Display Authentication and Copy Protection Method 3a (Alternate Scrambler Seed Reset) and Method 3b (Enhanced Framing) are supported, as per *eDP 1.2*.

The PTN3460 DPCD registers can be accessed by DP source through AUX channel. It supports both Native AUX transactions and I^2C-over-AUX transactions.

Native AUX transactions are used to access PTN3460 DisplayPort Configuration Data (DPCD) registers (e.g., to facilitate Link training, check error conditions, etc.) and I^2C-over-AUX transactions are used to perform any required access to DDC bus (e.g., EDID reads).

Given that the HPDRX pin is internally connected to GND through an integrated pull-down resistor (> 100 kΩ), the DP source will see HPDRX pin as LOW indicating that the DisplayPort receiver is not ready when the device is not powered. This helps avoid raising false events to the source. After power-up, PTN3460 continues to drive HPDRX pin LOW until completion of internal initialization. After this, PTN3460 generates HPD signal to notify DP source and take corrective action(s).

8.1.1 DP Link

PTN3460 is capable of operating either in DP 2-lane or 1-lane mode. The default is 2-lane mode of operation (in alignment with PTN3460 DCPD register 00002h, MAX_LANE_COUNT = 2).

There are two ways to enable 1-lane operation in an application:

- Connect both DP lanes of PTN3460 to the DP source. This enables the DP source to decide/use only required number of lanes based on display resolution.
- Connect only 1 lane (DP0_P, DP0_N) to DP source and modify the DPCD register 00002h, MAX_LANE_COUNT to ‘1’ through NXP I^2C configuration utility to modify the internal configuration table. Please consult NXP for more details regarding the Flash-over-AUX and DOS utilities.

8.1.2 DPCD registers

DPCD registers are described in VESA DisplayPort v1.1a/1.2 specifications in detail and PTN3460 supports DPCD version 1.2.

PTN3460 configuration registers can be accessed through DP AUX channel from the GPU/CPU, if required. They are defined under vendor-specific region starting at base address 0x00510h. So any configuration register can be accessed at DPCD address obtained by adding the register offset and base address.

PTN3460 supports down spreading on DP link and this is reflected in DPCD register MAX_DOWNSPREAD at address 0003h. Further, the DP source could control down spreading and inform PTN3460 via DOWNSPREAD_CTRL register at DPCD register 00107h.

The key aspect is that the system designer must take care that the Input video payload fits well within both DP link bandwidth and LVDS bandwidth (for a given pixel frequency, SSC depths) when clock spreading is enabled. Also, another aspect for the system designer is to ensure LVDS (panel) TCONs are capable of handling SSC modulated LVDS signaling.

8.2 LVDS transmitter

The LVDS interface can operate either in Single or Dual LVDS Bus mode at pixel clock frequencies over the range of 25 MHz to 112 MHz and color depths of 18 bpp or 24 bpp. Each LVDS bus consists of 3/4 differential data pairs and one clock pair. PTN3460 can packetize RGB video data, HSYNC, VSYNC, DE either in VESA or JEIDA format. To enable system EMI reduction, the device can be programmed for center spreading of LVDS channel clock outputs.

The LVDS interface can be flexibly configured using multi-level configuration pins (CFG1, CFG2, CFG3, CFG4) or via register interface. The configuration pins and the corresponding definitions are described in Table 3 through Table 6. Nevertheless, as the configuration pins are designed for general purpose, their definitions can be modified and they can be used for any other purposes. However, this can be achieved through firmware upgrade only.

Table 3. CFG1 configuration options

Configuration input setting	Number of LVDS links
LOW	single LVDS bus
HIGH	dual LVDS bus

Table 4. CFG2 configuration options

3-level configuration input setting	Data format	Number of bits per pixel (bpp)
LOW	VESA	24 bpp
open	JEIDA	24 bpp
HIGH	JEIDA or VESA	18 bpp

Table 5. CFG3 configuration options[1]

3-level configuration input setting	LVDS clock frequency spread depth control
LOW	0 %
open	1 %
HIGH	0.5 %

[1] LVDS center spreading modulation frequency is kept at 32.9 kHz.

Table 6. CFG4 configuration options

3-level configuration input setting	LVDS output swing (typical value)
pull-down resistor[1] to GND	250 mV
open	300 mV
pull-up resistor[1] to $V_{DD(3V3)}$	400 mV

[1] Pull-up/down resistor value in the range of 1 kΩ to 10 kΩ.

The VESA and JEIDA data format definitions are described in Table 7 to Table Table 13.

Table 7. LVDS single bus, 18 bpp, VESA or JEIDA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2

Table 8. LVDS single bus, 24 bpp, VESA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

Table 9. LVDS dual bus, 18 bpp, VESA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2

Table 10. LVDS dual bus, 24 bpp, VESA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

Table 11. LVDS single bus, 24 bpp, JEIDA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel B	bit 3	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 7	bit 6	bit 5	bit 4
LVDS odd differential channel D	don't care	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0

Table 12. LVDS dual bus, 18 bpp, JEIDA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2

Table 13. LVDS dual bus, 24 bpp, JEIDA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel B	bit 3	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 7	bit 6	bit 5	bit 4
LVDS odd differential channel D	don't care	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0
LVDS even differential channel A	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel B	bit 3	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 7	bit 6	bit 5	bit 4
LVDS even differential channel D	don't care	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0

PTN3460 delivers great flexibility by supporting more programmable options via I^2C-bus or AUX interface. Please refer to Section 8.3.8 for more details.

8.3 System control and operation

With its combination of embedded microcontroller, non-volatile memory, DPCD AUX and I²C-bus interfaces, PTN3460 delivers significant value for customer applications by providing higher degree of control and programmability.

By default, all user controllable registers can be accessed through DPCD AUX interface. This interface is always enabled. This AUX interface delivers seamless access of PTN3460 registers to system/platform (GPU) firmware driver. Nevertheless, use of I²C-bus interface for configuring PTN3460 is left to the choice of system integrator.

DEV_CFG (pin 12) sets up I²C-bus configuration mode:

- Pull-down resistor to GND — PTN3460 operates as I²C-bus slave, low address (0x40h)
- Open — PTN3460 operates as I²C-bus slave, high address (0xC0h)
- Pull-up resistor to $V_{DD(3V3)}$ — PTN3460 operates as I²C-bus master capable of reading from external EEPROM

8.3.1 Reset, power-down and power-on initialization

The device has a built-in reset circuitry that generates internal reset signal after power-on. All the internal registers and state machines are initialized and the registers take default values. In addition, PTN3460 has a dedicated control pin RST_N. This serves the same purpose as power-on reset, but without power cycling of the device/platform.

PTN3460 starts up in a default condition after power-on or after RST_N is toggled from LOW to HIGH. The configuration pins are sampled at power-on, or external reset, or when returning from Deep Sleep.

PTN3460 goes into Deep power-saving when PD_N is LOW. This will trigger a power-down sequence. To leave Deep power-saving state, the system needs to drive PD_N back to HIGH. If PD_N pin is open, the device will not enter Deep power-saving state. Once the device is in Deep power-saving condition, the HPDRX pin will go LOW automatically and this can be used by the system to remove the 3.3 V supply, if required.

Remark: The device will not respect the Panel power-down sequence if PD_N is asserted LOW while video is being streamed to the display. So the system is not supposed to toggle PD_N and RST_N pins asynchronously while the LVDS output is streaming video to the display panel, but instead follow the panel powering sequence as described in Section 8.3.3.

8.3.2 LVDS panel control

PTN3460 implements eDPv1.2 specific DPCD registers that concern panel power, backlight and PWM controls and the DP source can issue AUX commands to initiate panel power-up/down sequence as required. Also, PTN3460 supports LVDS panel control pins — backlight enable, panel power enable and PWM — that can be set via AUX commands.

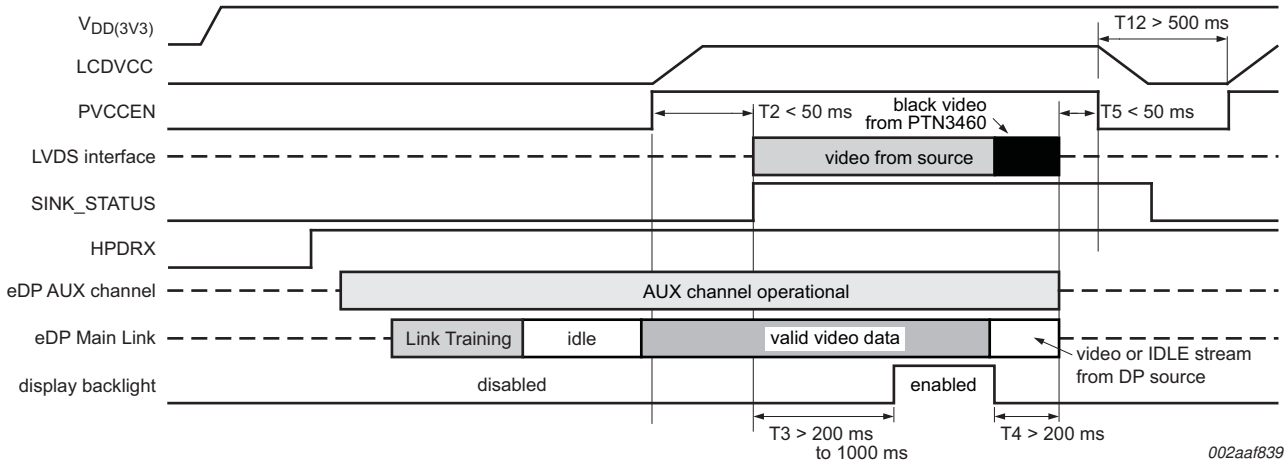
- **PVCCEN pin** — the signal output is set based on SET_POWER DPCD register 00600h and SET_POWER_CAPABLE bit of EDP_GENERAL_CAPABILITY_REGISTER_1 DPCD register 00701h and detection and handling of video data stream by PTN3460
- **BKLTEN pin** — the signal output is set based on BACKLIGHT_PIN_ENABLE_CAPABLE bit of EDP_GENERAL_CAPABILITY_REGISTER_1 DPCD register 00701h and BACKLIGHT_ENABLE bit of EDP_DISPLAY_CONTROL_REGISTER DPCD register 00720h
- **PWMO pin** — the PWM signal generated by PTN3460 based on controls set in DPCD registers. In addition, PTN3460 can pass through PWM signal from eDP source as well. Please refer to Ref. 2 for more information.

All the panel control enable and signal outputs from PTN3460 are aligned with panel power-on sequence timing including LVDS video output generation. It is important to note that the Panel power must be delivered by the system platform and it should be gated by PVCCEN signal.

8.3.3 Panel power sequencing

Figure 4 illustrates an example of panel power-up/power-down sequence for PTN3460.

Depending on the source behavior and PTN3460 firmware version, the powering sequence/timing could have some slight differences.



T2: Time interval between panel power enable signal (PVCCEN) going HIGH and video data/clock driven on LVDS interface.

T3: Time interval between valid video data/clock on LVDS interface and backlight enable signal (BKLTEN) going HIGH.

T4: Time interval between backlight enable signal (BKLTEN) made LOW and stopping of video data/clock on LVDS interface.

T5: Time interval between stopping of video data/clock on LVDS interface and panel power enable signal (PVCCEN) made LOW.

T12: Time interval for which PVCCEN is held LOW before it can be made HIGH.

Fig 4. Panel power-up/power-down sequence example

When working with eDP capable DP sources, PTN3460 supports the following (for specific sequence, refer to Figure 4):

- After power-on/startup, HPDRX is asserted HIGH, DP source will start AUX communication for initialization, perform Link Training and starts the video data stream. Once presence of video data is detected, PTN3460 will assert PVCCEN to HIGH, synchronize to video stream, output LVDS data and assert rise the Sink_status lock as indicated in DPCD register (0x00205h). PTN3460 will wait for Backlight enabling delay (T3) to avoid visual artifacts and program the BKLTEN HIGH.
- While transitioning out of Active state by receiving DPCD 0x600 to set PTN3460 in D3 mode, PTN3460 will disable BKLTEN prior to cutting off Video streaming to avoid visible artifacts following specific panel specifications. PTN3460 will assert PVCCEN to LOW after T5 delay as long as either if the video stream is stopped or video synchronization is lost. This is to avoid driving the LVDS panel with illegal stream for long periods of time. It is good practice for sources to keep video data or at least DP-idle stream active during T4 + T5.
- When PTN3460 is in Low-power state (DisplayPort D3 power state), the LVDS differential I/Os are weakly pulled down to 0 V. In this state, PVCCEN and BKLTEN are pulled LOW.
- When PD_N is LOW, which sets PTN3460 in Deep power-saving state, the BKLTEN pin is set to LOW. LVDS differential I/Os are pulled LOW via the weak pull-downs.

8.3.4 Termination resistors

The device provides integrated and calibrated 50 Ω termination resistors on both DisplayPort Main Link lanes and AUX channel.

8.3.5 Reference clock input

PTN3460 does not require an external clock. It relies fully on the clock derived internally from incoming DP stream or on-chip clock generator.

8.3.6 Power supply

PTN3460 can be flexibly supplied with either 3.3 V supply only or dual supplies (3.3 V/1.8 V). When supplied with 3.3 V supply only, the integrated regulator is used to generate 1.8 V for internal circuit operation. In this case, the EPS_N pin must be pulled HIGH or left open. For optimal power consumption, dual supply option (3.3 V and 1.8 V) is recommended.

8.3.7 Power management

In tune with the system application needs, PTN3460 implements aggressive techniques to support system power management and conservation. The device can exist in one of the three different states as described below:

- **Active state** when the device is fully operational.
- **Low-power state** when DP source issues AUX SET_POWER command on DPCD register 00600h. In this state, AUX and HPD circuits are operational but the main DP Link and LVDS Bus are put to high-impedance condition. The device will transition back to Active state when the DP source sets the corresponding DPCD register bits to ‘DisplayPort D0/Normal Operation mode’. The I^2C-bus interface will not be operational in this state.
- **Deep power-saving state**: In this state PTN3460 is put to ultra low-power condition. This is effected when PD_N is LOW. To get back to Active state, PD_N must be made HIGH. The external interfaces (like I^2C, AUX, DP, LVDS, configuration pins) will not be operational.

8.3.8 Register interface — control and programmability

PTN3460 has a register interface that can be accessed by CPU/GPU or System Controller to choose settings suitably for the System application needs. The registers can be read/written either via DP AUX or I^2C-bus interface. It is left to system integrator choice to use an interface to configure PTN3460.

PTN3460 provides greater level of configurability of certain parameters (e.g., LVDS output swing, spreading depth, etc.) via registers beyond what is available through pins. The register settings override the pin values. All registers must be configured during power-on initialization after HPDRX is HIGH. The registers and bit definitions are described in *“I^2C-bus utility and programming guide for firmware and EDID update”* (Ref. 3).

8.3.9 EDID handling

The DP source issues EDID reads using I^2C-over-AUX transactions and PTN3460, in turn, reads from the panel EDID ROM and passes back to the source. To support seamless functioning of panels without EDID ROM, the PTN3460 can be programmed to emulate EDID ROM and delivers internally stored EDID information to the source. Given

that EDID is specific to panels, PTN3460 enables system integrator to program EDID information into embedded memory through DP AUX and I^2C-bus interfaces. The supported EDID ROM emulation size is 896 bytes (seven EDID data structures, each of 128 bytes).

9. Application design-in information

Figure 5 illustrates PTN3460 usage in a system context. The eDP inputs are connected to DP source port on CPU/GPU and the LVDS outputs are connected to LVDS panel TCON.

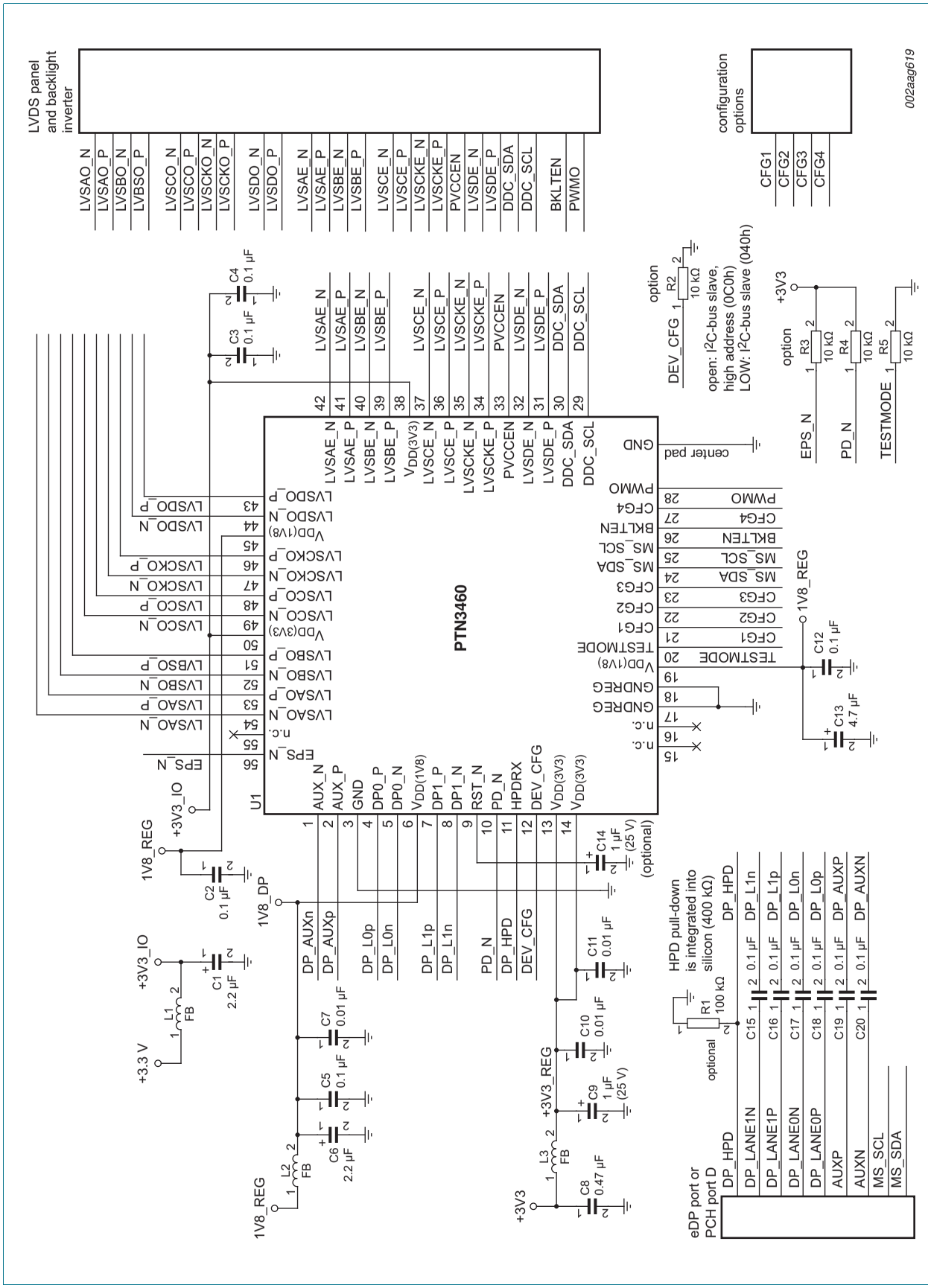


Fig 5. Application diagram

10. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	[1]	−0.3	+4.6	V
V_I	input voltage	3.3 V CMOS inputs [1]	−0.3	V_{DD} + 0.5	V
T_{stg}	storage temperature		−65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM [2]	-	8000	V
		CDM [3]	-	1000	V

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged-Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged-Device Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.

11. Recommended operating conditions

Table 15. Operating conditions

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DD(1V8)}$	supply voltage (1.8 V)		1.7	1.8	1.9	V
V_I	input voltage	3.3 V CMOS inputs	0	3.3	3.6	V
		open-drain I/O with respect to ground (e.g., DDC_SCL, DDC_SDA, MS_SDA, MS_SCL)	0	5	5.5	V
T_{amb}	ambient temperature	operating in free air	0	-	70	°C

12. Characteristics

12.1 Device characteristics

Table 16. Device characteristics

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	device start-up time from power-on and RST_N = HIGH; supply voltage within operating range to specified operating characteristics	-	-	90	ms
$t_{w(rst)}$	reset pulse width	device is supplied with valid supply voltage	10	-	-	µs
$t_{d(rst)}$	reset delay time[1]	device is supplied with valid supply voltage	-	-	90	ms
$t_{d(pwrsave-act)}$	delay time from power-save to active	time between PD_N going HIGH and HPD raised HIGH by PTN3460; RST_N is HIGH. Device is supplied with valid supply voltage.	-	-	90	ms

[1] Time for device to be ready after rising edge of RST_N.

12.2 Power consumption

Table 17. Power consumption

At operating free-air temperature of 25 °C and under nominal supply value (unless otherwise noted).

Symbol	Parameter	Conditions	Single supply mode EPS_N = HIGH or open			Dual supply mode EPS_N = LOW			Unit
			Min	Typ	Max	Min	Typ	Max	
P_{cons}	power consumption	Active mode; [1] 1440 × 900 at 60 Hz; 24 bits per pixel; dual LVDS bus	-	430	-	-	290	-	mW
		Active mode; [1] 1600 × 900 at 60 Hz; 24 bits per pixel; dual LVDS bus	-	448	-	-	305	-	mW
		Active mode; [1] 1920 × 1200 at 60 Hz; 24-bits per pixel; dual LVDS bus	-	570	-	-	380	-	mW
		D3 mode/Power-saving mode; when PTN3460 is set to Power-saving mode via 'SET_POWER' AUX command by eDP source; AUX and HPDRX circuitry are only kept active	-	27	-	-	15	-	mW
		Deep power-saving/Shutdown mode; when PD_N is LOW and the device is supplied with valid supply voltage	-	5	-	-	2	-	mW

[1] For Active mode power consumption, LVDS output swing of 300 mV is considered.

12.3 DisplayPort receiver characteristics

Table 18. DisplayPort receiver main channel characteristics

Over operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UI	unit interval	high bit rate (2.7 Gbit/s per lane) [1]	-	370	-	ps
		reduced bit rate (1.62 Gbit/s per lane) [1]	-	617	-	ps
Δf_{DOWN_SPREAD}	link clock down spreading	[2]	0	-	0.5	%
C_{RX}	AC coupling capacitor		75	-	200	nF
$V_{RX\_DIFFp\text{-}p}$	differential input peak-to-peak voltage	at receiver package pins				
		high bit rate (2.7 Gbit/s per lane) [3]	120	-	-	mV
		reduced bit rate (1.62 Gbit/s per lane) [3]	40	-	-	mV
$V_{RX\_DC\_CM}$	RX DC common mode voltage	[4]	0	-	2.0	V
I_{RX_SHORT}	RX short-circuit current limit	[5]	-	-	50	mA
$f_{RX\_TRACKING\_BW}$	jitter tracking bandwidth	[6]	20	-	-	MHz
$G_{eq(max)}$	maximum equalization gain	at 1.35 GHz	-	15	-	dB

[1] Range is nominal ±350 ppm. DisplayPort channel RX does not require local crystal for channel clock generation.

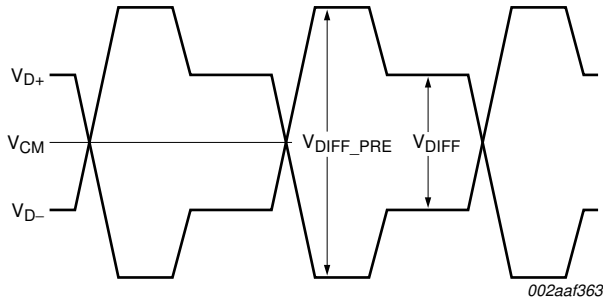
[2] Up to 0.5 % down spreading is supported. Modulation frequency range of 30 kHz to 33 kHz is supported.

[3] Informative; refer to Figure 6 for definition of differential voltage.

[4] Common-mode voltage is equal to V_{bias_RX} voltage.

[5] Total drive current of the input bias circuit when it is shorted to its ground.

[6] Minimum CDR tracking bandwidth at the receiver when the input is repetition of D10.2 symbols without scrambling.



pre-emphasis = 20Log(V_{DIFF_PRE} / V_{DIFF})

Fig 6. Definition of pre-emphasis and differential voltage

12.4 DisplayPort AUX characteristics

Table 19. DisplayPort AUX characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UI	unit interval		[1]	0.4	0.5	0.6	μs
$t_{jit(cc)}$	cycle-to-cycle jitter time	transmitting device	[2]	-	-	0.04	UI
		receiving device	[3]	-	-	0.05	UI
$V_{AUX\_DIFFp-p}$	AUX differential peak-to-peak voltage	transmitting device	[4]	0.39	-	1.38	V
		receiving device	[4]	0.32	-	1.36	V
$R_{AUX\_TERM(DC)}$	AUX CH termination DC resistance	informative		-	100	-	Ω
$V_{AUX\_DC\_CM}$	AUX DC common-mode voltage		[5]	0	-	2.0	V
$V_{AUX\_TURN\_CM}$	AUX turnaround common-mode voltage		[6]	-	-	0.3	V
I_{AUX_SHORT}	AUX short-circuit current limit		[7]	-	-	90	mA
C_{AUX}	AUX AC coupling capacitor		[8]	75	-	200	nF

[1] Results in the bit rate of 1 Mbit/s including the overhead of Manchester II coding.

[2] Maximum allowable UI variation within a single transaction at connector pins of a transmitting device. Equal to 24 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.

[3] Maximum allowable UI variation within a single transaction at connector pins of a receiving device. Equal to 30 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.

[4] $V_{AUX\_DIFFp-p} = 2 \times |V_{AUX\_P} - V_{AUX\_N}|$.

[5] Common-mode voltage is equal to V_{bias_TX} (or V_{bias_RX}) voltage.

[6] Steady-state common-mode voltage shift between transmit and receive modes of operation.

[7] Total drive current of the transmitter when it is shorted to its ground.

[8] The AUX channel AC-coupling capacitor placed both on the DisplayPort source and sink devices.

12.5 LVDS interface characteristics

Table 20. LVDS interface characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	R_L = 100 Ω; CFG4 pin is open and LVDS interface control 2 register in default value	250	300	350	mV
$\Delta V_{o(dif)}$	differential output voltage variation	R_L = 100 Ω; change in differential output voltage between complementary output states	-	-	50	mV
V_{cm}	common-mode voltage	R_L = 100 Ω	1.125	1.2	1.375	V
I_{OS}	output short-circuit current	R_L = 100 Ω	-	-	24	mA
I_{OZ}	OFF-state output current	output 3-state circuit current; R_L = 100 Ω; LVDS outputs are 3-stated; receiver biasing at 1.2 V	-	-	20	μA
t_r	rise time	R_L = 100 Ω; from 20 % to 80 %	-	-	390	ps
t_f	fall time	R_L = 100 Ω; from 80 % to 20 %	-	-	390	ps
t_{sk}	skew time	intra-pair skew between differential pairs	-	-	50	ps
		inter-pair skew between 2 adjacent LVDS channels	-	-	200	ps
m	modulation index	for center spreading				
		minimum modulation depth	-	0	-	%
		maximum modulation depth	-	2.5	-	%
f_{mod}	modulation frequency	center spreading	30	-	100	kHz

12.6 Control inputs and outputs

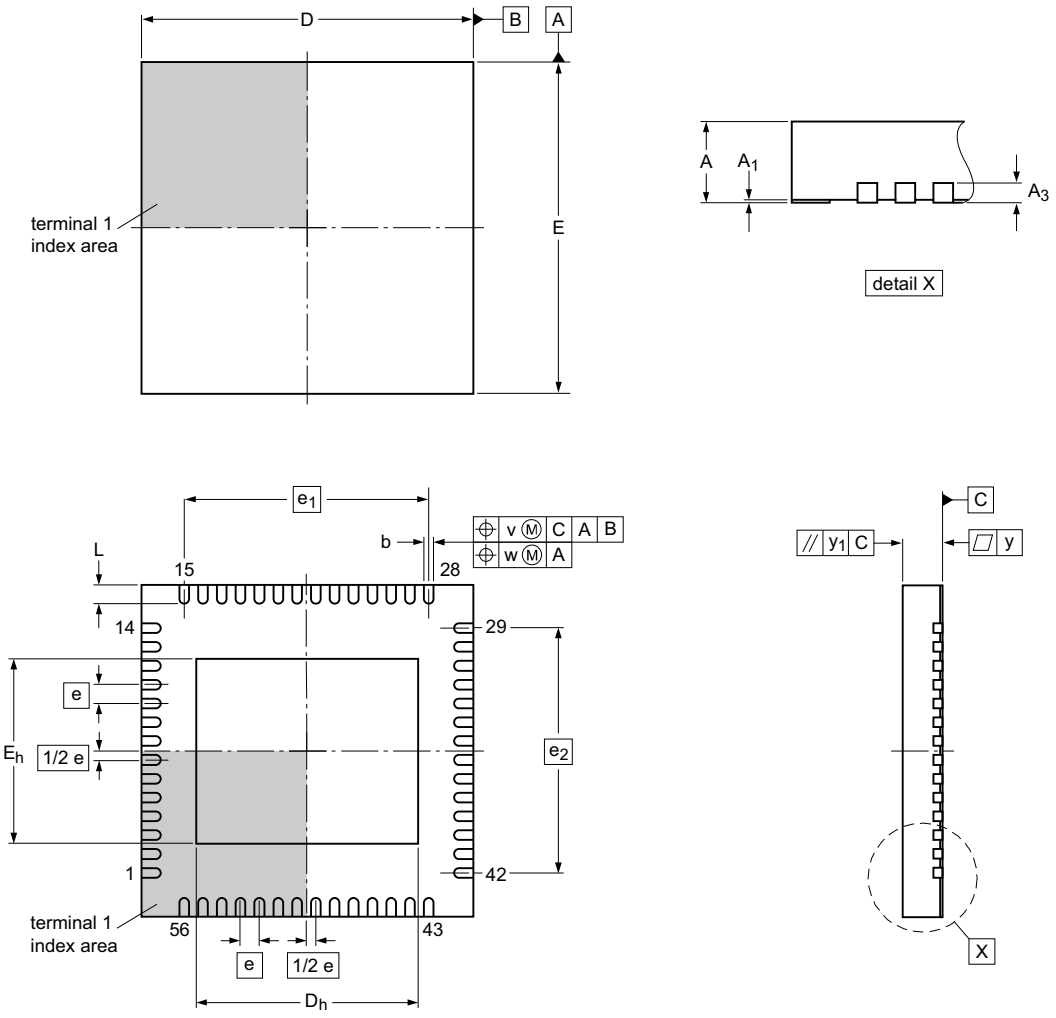
Table 21. Control input and output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Signal output pins — PVCCEN, BKLTEN, HPDRX, PWMO						
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	-	-	0.4	V
Control input pins — RST_N, PD_N, TESTMODE, DEV_CFG, CFG[4:1]						
V_{IH}	HIGH-level input voltage		$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(3V3)}$	V
Control input pin — EPS_N						
V_{IH}	HIGH-level input voltage		$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.2V_{DD(3V3)}$	V
DDC_SDA, DDC_SCL, MS_SDA, MS_SCL[1]						
V_{IH}	HIGH-level input voltage		$0.7V_{DD(3V3)}$	-	5.25	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(3V3)}$	V
I_{OL}	LOW-level output current	static output; V_{OL} = 0.4 V	3.0	-	-	mA

[1] For DDC_SCL, DDC_SDA, MS_SCL, MS_SDA characteristics, please refer to *UM10204, "I²C-bus specification and user manual"* (Ref. 11).

13. Package outline

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads;
56 terminals; body 7 x 7 x 0.85 mm SOT949-2



Dimensions

Unit		$A^{(1)}$	A_1	A_3	b	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05		0.30	7.1	4.85	7.1	4.05				0.5				
mm	nom	0.85	0.02	0.2	0.21	7.0	4.70	7.0	3.90	0.4	5.2	5.2	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00		0.18	6.9	4.55	6.9	3.75				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot949-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT949-2		MO-220				~~11-09-06~~ 11-09-16

Fig 7. Package outline SOT949-2 (HVQFN56)

14. Packing information

Figure 8 is an example of the label that would be placed on the product shipment box and the tape/reel.

002aag652

Fig 8. Packing label example

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.