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PTN36241G

SuperSpeed USB 3.0 redriver

Rev. 1.1 — 9 August 2016 Product data sheet

1. General description

PTN36241G is a very small, low power SuperSpeed USB 3.0 redriver IC that enhances signal quality by performing receive equalization on the deteriorated input signal followed by transmit de-emphasis maximizing system link performance for mobile applications. With its superior differential signal conditioning and enhancement capability, the device delivers significant flexibility and performance scaling for various systems with different PCB trace and cable channel conditions and still benefit from optimum power consumption.

PTN36241G is a dual-channel device that supports data signaling rate of 5 Gbit/s through each channel. The data flow of one channel is facing the USB host, and another channel is facing the USB peripheral or device. Each channel consists of a high-speed Transmit (Tx) differential lane and a high-speed Receive (Rx) differential lane.

PTN36241G has built-in advanced power management capability that enables significant power savings under various different USB 3.0 Low-power modes (U2/U3). It can detect link electrical conditions and can dynamically activate/de-activate internal circuitry and logic. The device performs these actions without host software intervention and conserves power.

PTN36241G is powered from a 1.8 V supply and is available in a small X2QFN12 package (1.25 mm × 2.1 mm × 0.35 mm) with 0.4 mm pitch.

2. Features and benefits

- Supports USB 3.0 specification (SuperSpeed only)
- Compliant to SuperSpeed USB 3.0 standard
- Support of two channels
- Pin out data flow matches USB 3.0 Micro-AB/Micro-B receptacle pin assignments
- Two control pins to select optimized signal conditions
  - Receive equalization on each channel to recover from InterSymbol Interference (ISI) and high-frequency losses, with provision to choose equalization gain settings per channel
  - Transmit de-emphasis on each channel delivers pre-compensation suited to channel conditions
  - Output swing adjustment
- Integrated termination resistors provide impedance matching on both transmit and receive sides
- Automatic receiver termination detection
- Low active power: 189 mW/105 mA (typical) for V_{DD} = 1.8 V

- Power-saving states:
  - 1.8 mW/1 mA (typical) when in U2/U3 states
  - 0.9 mW/0.5 mA (typical) when no connection detected
  - 3.6 μW/2 μA (typical) when in Deep power-saving state
- Excellent differential and common return loss performance
  - 14 dB differential and 15 dB common-mode return loss for 10 MHz to 1250 MHz
- Flow-through pinout to ease PCB layout and minimize crosstalk effects
- Hot Plug capable
- Power supply: V_{DD} = 1.8 V (typical)
- Compliant with JESD 78 Class II
- Very thin X2QFN12 package: 1.25 mm × 2.1 mm × 0.35 mm, 0.4 mm pitch
- ESD protection exceeds 7000 V HBM per JDS-001-2012 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating temperature range: −40 °C to 85 °C

3. Applications

- Smart phones, tablets
- Active cables
- Notebook/netbook/nettop platforms
- Docking stations and AIO platforms
- USB 3.0 peripherals such as flat panel display, consumer/storage devices, printers or USB 3.0 capable hubs/repeaters

4. System context diagrams

Figure 1 illustrates PTN36241G usage.

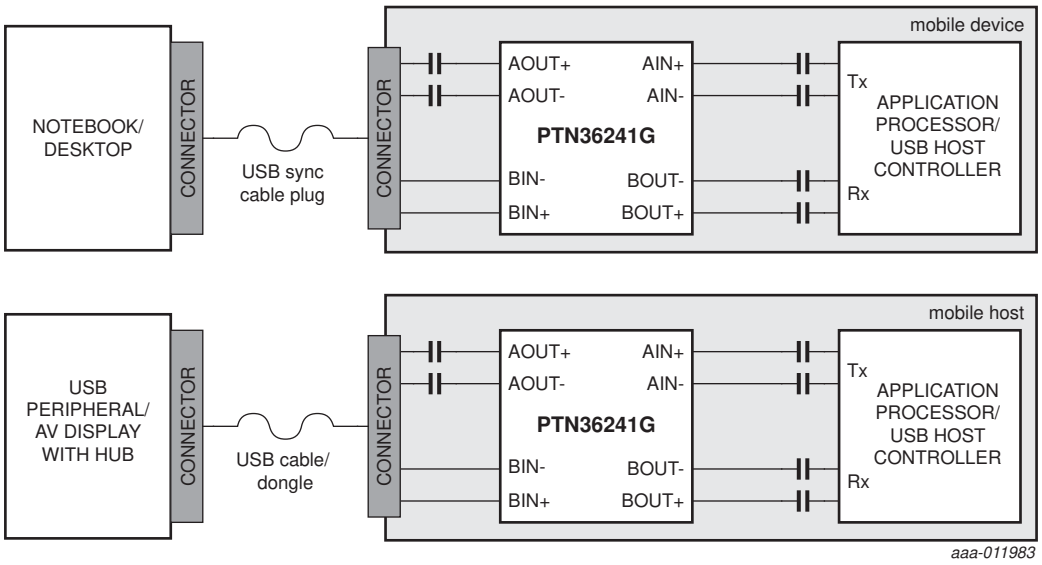


Fig 1. PTN36241G context diagrams

5. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PTN36241G	41G	X2QFN12	plastic, super thin quad flat package; no leads; 12 terminals; body 1.25 × 2.10 × 0.35 mm; 0.4 mm lead pitch	SOT1408-1

5.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN36241GHX	PTN36241GHXZ	X2QFN12	REEL 7" Q1/T1 *STANDARD MARK DP	6000	T_{amb} = −40 °C to +85 °C

6. Block diagram

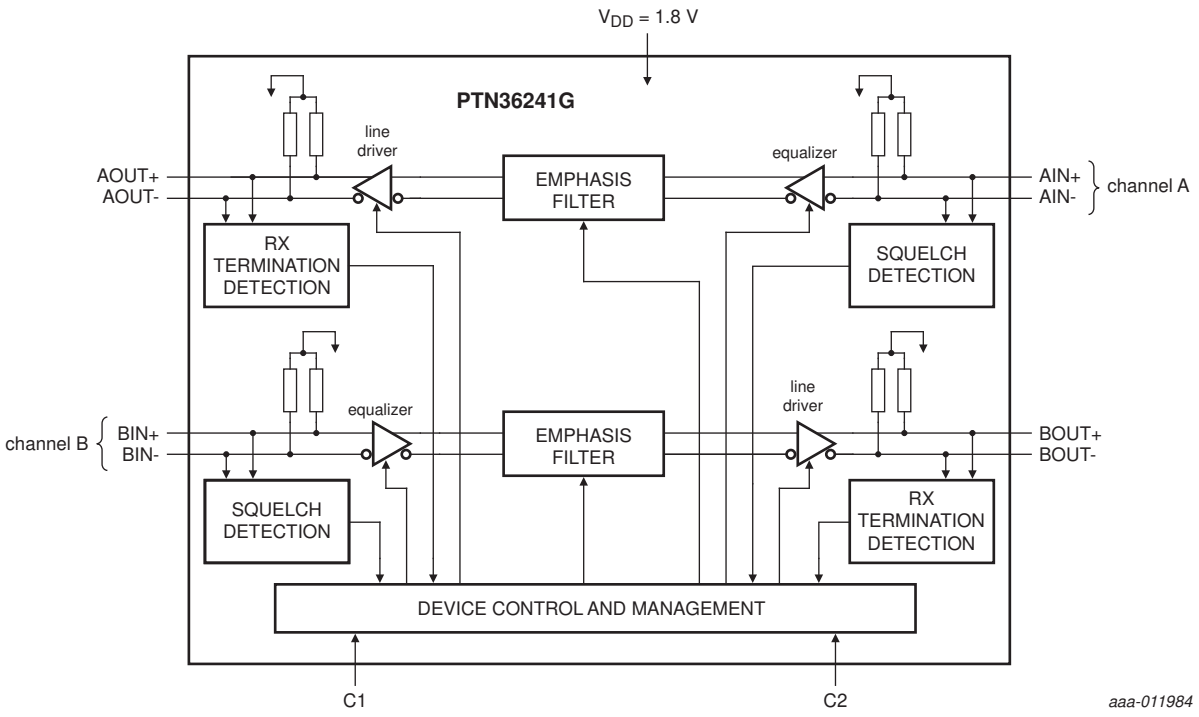


Fig 2. Block diagram of PTN36241G

7. Pinning information

7.1 Pinning

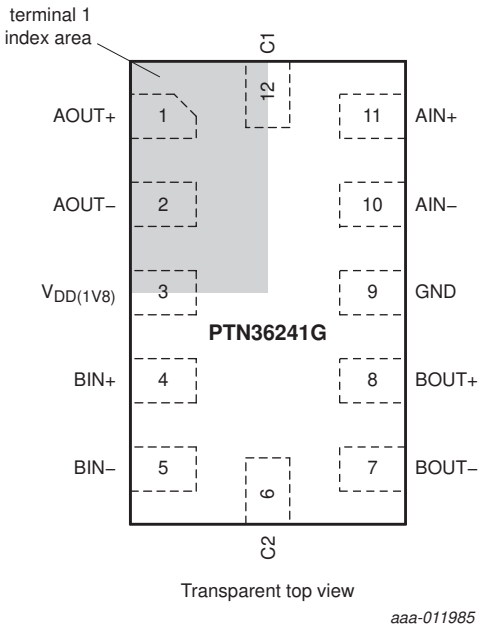


Fig 3. Pin configuration for X2QFN12

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
High-speed differential signals			
AIN+	11	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. AIN+ makes a differential pair with AIN–. The input to this pin must be AC-coupled externally.
AIN–	10	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. AIN– makes a differential pair with AIN+. The input to this pin must be AC-coupled externally.
BOUT+	8	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. BOUT+ makes a differential pair with BOUT–. The output of this pin must be AC-coupled externally.
BOUT–	7	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. BOUT– makes a differential pair with BOUT+. The output of this pin must be AC-coupled externally.
AOUT+	1	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. AOUT+ makes a differential pair with AOUT–. The output of this pin must be AC-coupled externally.
AOUT–	2	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. AOUT– makes a differential pair with AOUT+. The output of this pin must be AC-coupled externally.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
BIN+	4	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. BIN+ makes a differential pair with BIN–. The input to this pin must be AC-coupled externally.
BIN–	5	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. BIN– makes a differential pair with BIN+. The input to this pin must be AC-coupled externally.
Configuration and control signals			
C1	12	Ternary input	C1 controls traces on the left side (as shown in Figure 2) of the redriver — AOUT–/AOUT+ and BIN–/BIN+. C1 controls setting of AOUT+/AOUT– output swing and de-emphasis and BIN–/BIN+ equalization.
C2	6	Ternary input	C2 controls traces on the right side (as shown in Figure 2) of the redriver — BOUT–/BOUT+ and AIN–/AIN+. C2 controls setting of BOUT+/BOUT– output swing and de-emphasis and AIN–/AIN+ equalization.
Power supply			
$V_{DD(1V8)}$	3	power	1.8 V supply. A 0201 or 0402 size 0.1 μF de-coupling capacitor is highly recommended to be placed as close as possible on this pin to GND.
Ground connection			
GND	9	power	Ground.

8. Functional description

Refer to Figure 2 “Block diagram of PTN36241G”.

PTN36241G is a SuperSpeed USB 3.0 redriver meant to be used for signal integrity enhancement on mobile platforms – smart phone, tablet, notebook, hub, A/V display and peripheral devices, for example. With its high fidelity differential signal conditioning capability and wide configurability, this chip is flexible and versatile enough for use under a variety of system environments. PTN36241G implements ternary control IO logic on C1 and C2 control pins to detect HIGH (connected to VDD), LOW (connected to GND) or left unconnected condition (OPEN).

The following sections describe the individual block functions and capabilities of the device in more detail.

8.1 C1 control pin

C1 controls signal traces on the left side (as shown in Figure 2) of the redriver. It controls the transmit de-emphasis and output swing of AOUT–/AOUT+ channel. It also controls the receive equalization of BIN–/BIN+ channel.

When C1 = HIGH, the left side of the redriver is optimized to drive long trace length of the left Link.

When C1 = OPEN, the left side of the redriver is optimized to drive medium trace length of the left Link.

When C1 = LOW, the left side of the redriver is optimized to drive short trace length of the left Link.

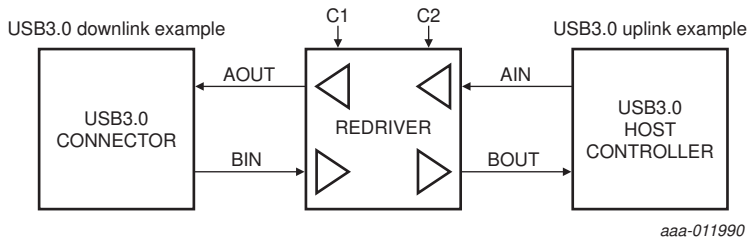


Fig 4. C1 controls traces on left side of the redriver

Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[1]	DE[2]	OS[3]
HIGH	Long	HIGH	9 dB	–5.3 dB	1.1 V
OPEN	Medium	OPEN	6 dB	–3.1 dB	1.0 V
LOW	Short	LOW	3 dB	0 dB	0.9 V

[1] EQ is the internal input receiver equalization gain at 2.5 GHz.

[2] DE is the internal output signal de-emphasis gain.

[3] OS is the internal transmit output differential voltage swing.

8.2 C2 control pin

C2 controls signal traces on the right side with functionality similar to C1.

Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[2]	OS[3]
HIGH	Long	HIGH	9 dB	–5.3 dB	1.1 V
OPEN	Medium	OPEN	6 dB	–3.1 dB	1.0 V
LOW	Short	LOW	3 dB	0 dB	0.9 V

[1] EQ is the internal input receiver equalization gain at 2.5 GHz.

[2] DE is the internal output signal de-emphasis gain.

[3] OS is the internal transmit output differential voltage swing.

8.3 Deep power-saving mode entry and exit using C1 and C2 pins

C1 and C2 pins can be controlled by GPIOs from the on-board processor. When C1 and C2 pins are both pulled LOW, it will take up to 115 ms (t_{sHL})for internal logic to sample C1 and C2 pin states, and place the PTN36241G in Deep Power-saving mode. To exit from Deep Power-saving mode, the processor GPIOs should pull up C1 and/or C2 pins to HIGH, and PTN36241G will return back to normal active mode in 1 µs. In order for C1/C2 settings to take effect 6 ms (t_{sLH}) after PTN36241G returns back to Active mode, C1/C2 settings should be applied within the first 4 ms window. If settings are applied outside this 4 ms window, new C1 and C2 values will be latched and take effect every 115 ms (t_{rcfg}). Refer to Figure 5 for Deep Power-saving entry and exit control timing.

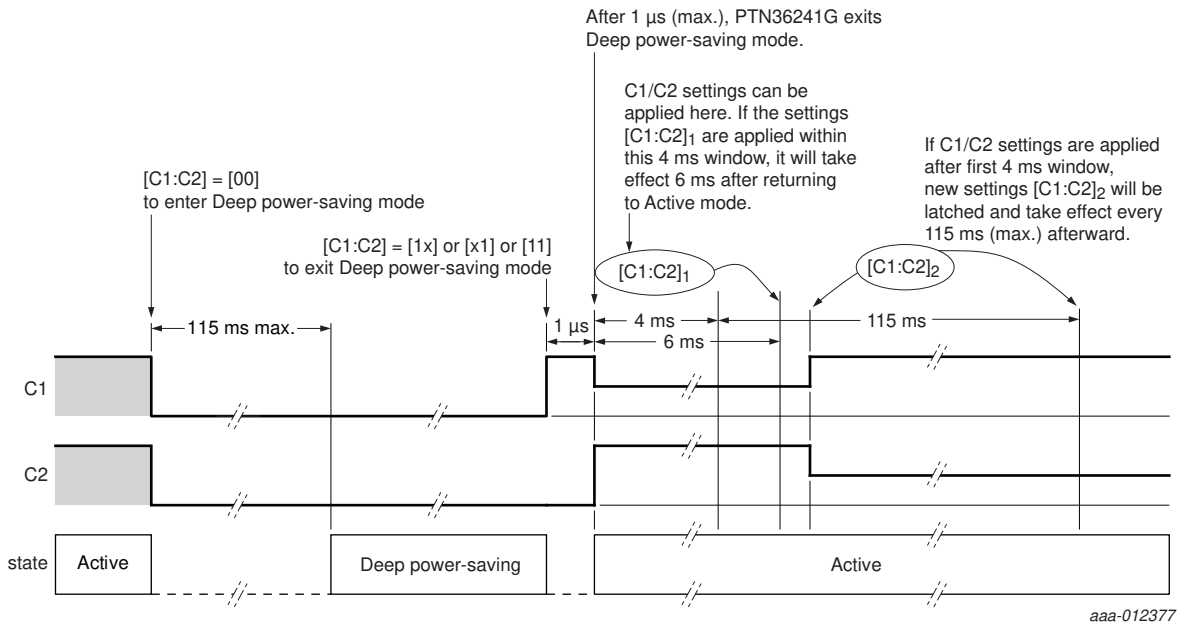


Fig 5. Deep power-saving entry and exit control timing

8.4 C1 and C2 overall control table

Table 6. C1 and C2 control table

C1	C2	EQ		DE		OS		CE[1]
		Channel A	Channel B	Channel A	Channel B	Channel A	Channel B	
HIGH	HIGH	9 dB	9 dB	–5.3 dB	–5.3 dB	1.1 V	1.1 V	1
HIGH	OPEN	6 dB	9 dB	–5.3 dB	–3.1 dB	1.1 V	1.0 V	1
HIGH	LOW	3 dB	9 dB	–5.3 dB	0 dB	1.1 V	0.9 V	1
OPEN	HIGH	9 dB	6 dB	–3.1 dB	–5.3 dB	1.0 V	1.1 V	1
OPEN	OPEN	6 dB	6 dB	–3.1 dB	–3.1 dB	1.0 V	1.0 V	1
OPEN	LOW	3 dB	6 dB	–3.1 dB	0 dB	1.0 V	0.9 V	1
LOW	HIGH	9 dB	3 dB	0 dB	–5.3 dB	0.9 V	1.1 V	1
LOW	OPEN	6 dB	3 dB	0 dB	–3.1 dB	0.9 V	1.0 V	1
LOW	LOW	Deep power-saving mode						0

[1] CE is the internal chip enable signal.

8.5 Transmit de-emphasis

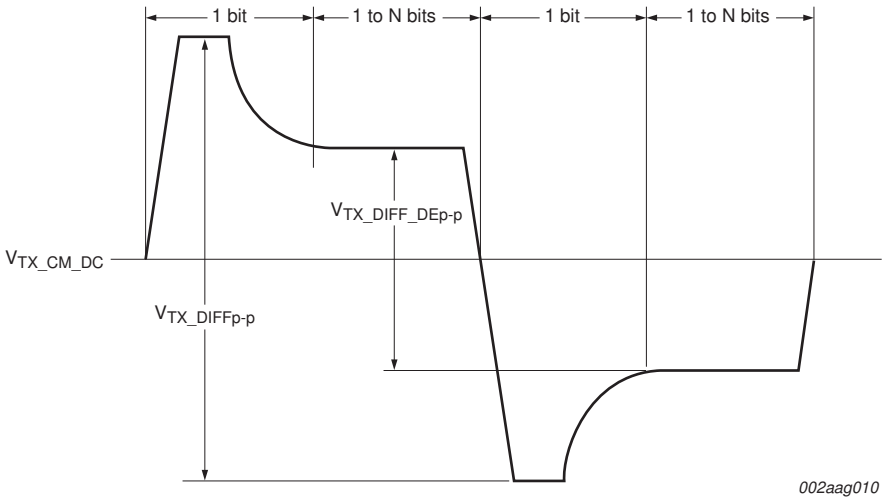


Fig 6. Output with –6 dB de-emphasis

8.6 Device states and power management

PTN36241G has implemented an advanced power management scheme that operates in tune with USB 3.0 bus electrical condition. Although the device does not decode USB power management commands (related to USB 3.0 U1/U2/U3 transitions) exchanged between USB 3.0 host and peripheral/device, it relies on bus electrical conditions and control pins/register settings to decide to be in one of the following states:

- **Active state** wherein device is fully operational, USB data is transported on channels A and B. In this state, USB connection exists and the Receive Termination indication remains active. But there is no need for Receive Termination detection.
- **Power-saving state** wherein the channels A and B are kept enabled. In this state, squelching, detection and/or Receive termination detection circuitry are active. Based on USB connection, there are two possibilities:
  - No USB connection.
  - When USB connection exists and when the link is in USB 3.0 U2/U3 mode.
- **Deep power-saving state** wherein both channels' TX and RX terminations are placed in OPEN condition, and the device achieves the most power saving. To enter deep power saving mode, an external GPIO controller can pull down C1 and C2 pins to ground at any time. Please refer to Section 8.3 for Deep power-saving entry and exit control timing information.

  As an example of utilizing deep power saving mode to achieve maximum power saving when USB3.0 interface is not active in a device such as a smart phone, the system can use the following scheme as a design guideline to implement the deep power saving mode.

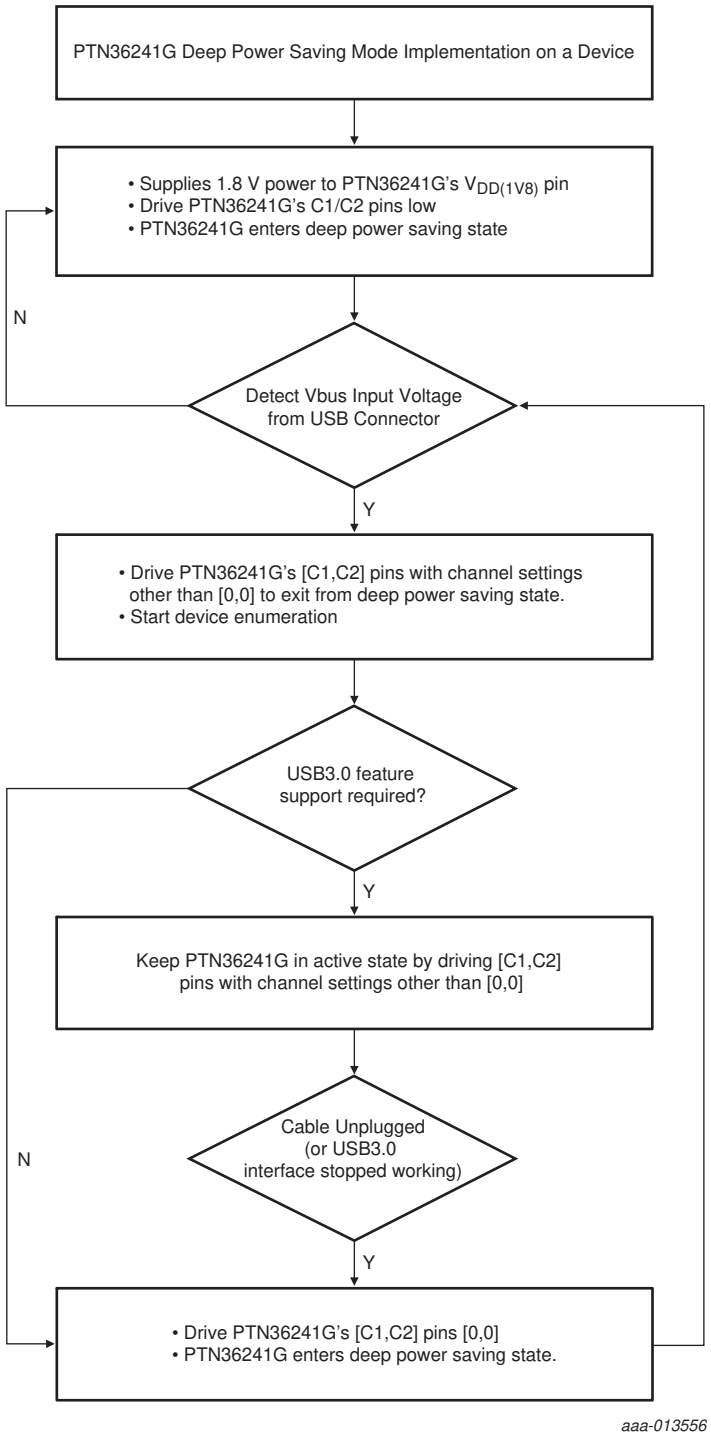


Fig 7. Flow chart

- **Off state**: When PTN36241G is not being powered (i.e., V_{DD1V8} = 0 V), special steps should be done to prevent back-current issues on C1/C2 pins when these pins' states are not low. C1/C2 pins can be controlled through two different ways.
  a. pull-up/pull-down resistors - make sure these pull-up resistors' V_{DD} is the same power source as to power PTN36241G. When power to PTN36241G is off, power to these pull-up resistors will be off as well.
  b. external processor's GPIO - if PTN36241G is turned off when the external processor's power stays on, processor should configure these GPIOs connected to C1/C2 pins as output low (< 0.4 V) or tri-state mode (configure GPIOs as input mode). This will make sure no current will be flowing into PTN36241G through C1/C2 pins.

The Receive termination detection circuitry is implemented as part of a transmitter and detects whether a load device with equivalent DC impedance Z_{RX_DC} is present.

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)	[1]	−0.3	+2.5	V
V_I	input voltage	[1]	−0.3	$V_{DD(1V8)}$ + 0.5	V
T_{stg}	storage temperature		−65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM [2]	-	7000	V
		CDM [3]	-	1000	V

[1] All voltage values (except differential voltages) are with respect to network ground terminal.

[2] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[3] Charged Device Model; JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

10. Recommended operating conditions

Table 8. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)	1.8 V supply option	1.7	1.8	1.9	V
V_I	input voltage	control and configuration pins (C1, C2)	−0.3	$V_{DD(1V8)}$	$V_{DD(1V8)}$ + 0.3	V
T_{amb}	ambient temperature	operating in free air	−40	-	+85	°C

11. Characteristics

11.1 Device characteristics

Table 9. Device characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	between supply voltage within operating range (90 % of V_{DD}) until automatic receiver termination detection	-	-	6	ms
$t_{s(LH)}$	LOW to HIGH settling time	disable to enable; enable time from 'Deep power-saving mode' (C1 = C2 = LOW) to active modes change; device is supplied with valid supply voltage	-	-	6	ms
$t_{s(HL)}$	HIGH to LOW settling time	enable to disable; disable time from active modes to 'Deep power-saving mode' (C1 = C2 = LOW) change until Deep power-saving mode; device is supplied with valid supply voltage	-	-	115	ms
t_{rcfg}	reconfiguration time	any configuration pin change (from one setting to another setting) to specified operating characteristics; device is supplied with valid supply voltage	-	-	115	ms
$t_{PD(dif)}$	differential propagation delay	between 50 % level at input and output; see Figure 8	-	-	0.5	ns
t_{idle}	idle time	default wait time to wait before getting into Power-saving state	-	300	400	ms
$t_{d(pwrsave-act)}$	delay time from power-save to active	time for exiting from Power-saving state and get into Active state; see Figure 10	-	-	115	µs
$t_{d(act-idle)}$	delay time from active to idle	reaction time for squelch detection circuit; see Figure 9	-	9	14	ns
$t_{d(idle-act)}$	delay time from idle to active	reaction time for squelch detection circuit; see Figure 9	-	5	11	ns
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC still air test environment; value is based on simulation under JEDEC still air test environment with 2S2P(4L) JEDEC PCB	-	92	-	°C/W
Ψ_{jt}	junction to top of case thermal characterization parameter	to case top; at ambient temperature of 85 °C; value is based on simulation under JEDEC still air test environment with 2S2P(4L) JEDEC PCB	-	0.5	-	°C/W
I_{DD}	supply current	Active state; C1 = C2 = OPEN; Rx equalization gain = 6 dB; Tx output signal swing = 1000 mV (differential peak-to-peak value); Tx de-emphasis = −3.1 dB	-	105	-	mA
		U2/U3 Power-saving state	-	1	-	mA
		no USB connection state	-	0.5	-	mA
		Deep power-saving state; C1 = C2 = LOW	-	2	-	µA

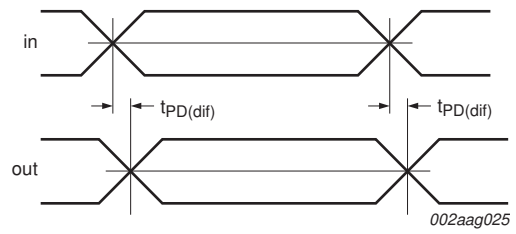


Fig 8. Propagation delay

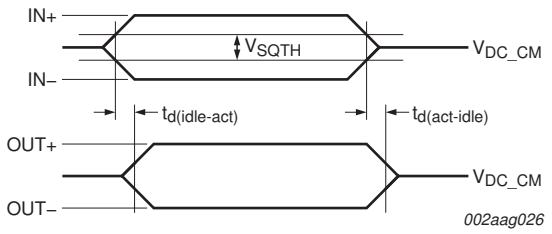


Fig 9. LFPS electrical idle transitions in U0/U1 modes

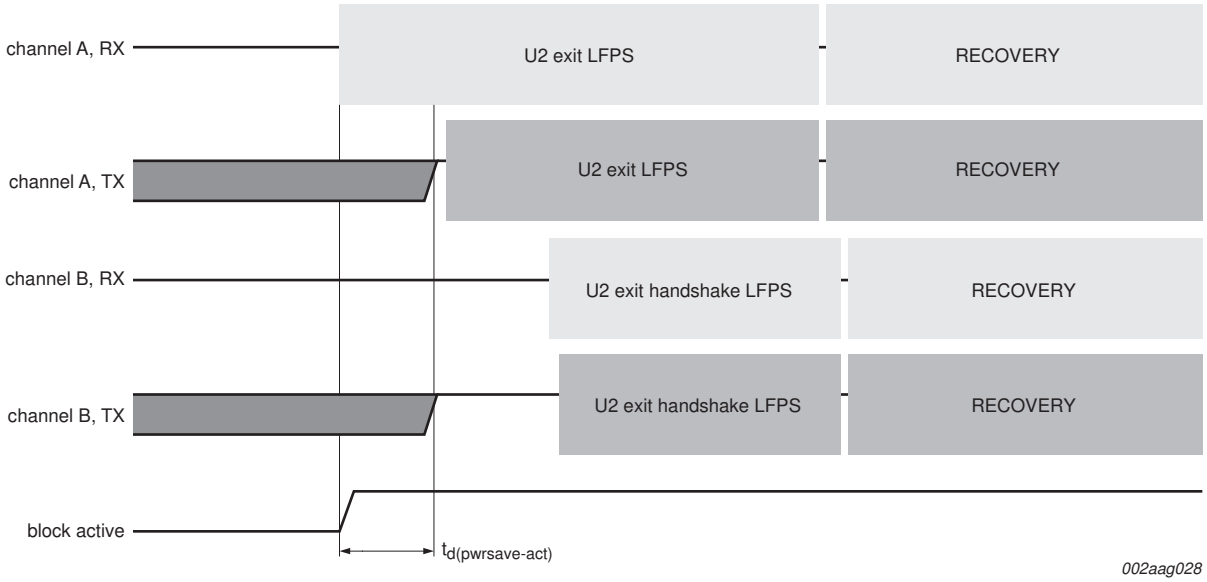


Fig 10. U2/U3 exit behavior

11.2 Receiver AC/DC characteristics

Table 10. Receiver AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{RX_DC}	receiver DC common-mode impedance		18	-	30	Ω
$Z_{RX\_DIFF\_DC}$	DC differential impedance	RX pair	72	-	120	Ω
$Z_{RX\_HIGH\_IMP}$	common-mode input impedance	DC common-mode input impedance when output of redriver is not terminated	25	-	-	kΩ
$V_{RX(diff)(p-p)}$	peak-to-peak differential receiver voltage		100	-	1200	mV
$V_{RX\_DC\_CM}$	RX DC common mode voltage		-	1.8	-	V
$V_{RX\_CM\_AC\_P}$	RX AC common-mode voltage	peak	-	-	150	mV
$V_{th(i)}$	input threshold voltage	differential peak-to-peak value	75	-	150	mV
$RL_{DD11,RX}$	RX differential mode return loss	10 MHz to 1250 MHz	12	14	-	dB
		1250 MHz to 2500 MHz	7	8.5	-	dB
		2500 MHz to 3000 MHz	6	7.5	-	dB
$RL_{CC11,RX}$	RX common mode return loss	10 MHz to 1250 MHz	12	15	-	dB
		1250 MHz to 2500 MHz	8	10	-	dB
		2500 MHz to 3000 MHz	7	9	-	dB

11.3 Transmitter AC/DC characteristics

Table 11. Transmitter AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{TX_DC}	transmitter DC common-mode impedance		18	-	30	Ω
$Z_{TX\_DIFF\_DC}$	DC differential impedance		72	-	120	Ω
$V_{TX\_DIFFp-p}$	differential peak-to-peak output voltage	R_L = 100 Ω				
		OS = short channel	800	900	1000	mV
		OS = medium channel	900	1000	1100	mV
		OS = long channel	1000	1100	1200	mV
$V_{TX\_DC\_CM}$	transmitter DC common-mode voltage		-	1.3	$V_{DD(1V8)}$	V
$V_{TX\_CM\_ACpp\_ACTIV}$	TX AC common-mode peak-to-peak output voltage (active state)	device input fed with differential signal	-	-	100	mV
$V_{TX\_IDL\_DIFF\_ACpp}$	electrical idle differential peak-to-peak output voltage	when link is in electrical idle	-	-	10	mV
$t_{W(deemp)TX}$	transmitter de-emphasis pulse width		160	175	200	ps
$V_{TX\_RCV\_DETECT}$	voltage change allowed during receiver detection	positive voltage swing to sense the receiver termination detection	-	-	600	mV
$R_{TX\_RCV\_DETECT}$	TX receiver termination detect charging resistance	output resistor of the transmitter when it does RX detection	-	3.1	-	kΩ
$t_{r(tx)}$	transmit rise time	measured using 20 % and 80 % levels; see Figure 11	40	55	75	ps
$t_{f(tx)}$	transmit fall time	measured using 80 % and 20 % levels; see Figure 11	40	55	75	ps
$t_{(r-f)tx}$	difference between transmit rise and fall time	measured using 20 % and 80 % levels	-	-	20	ps
$RL_{DD11,TX}$	TX differential mode return loss	10 MHz to 1250 MHz	12	13.5	-	dB
		1250 MHz to 2500 MHz	6.5	8	-	dB
		2500 MHz to 3000 MHz	5	6.5	-	dB
$RL_{CC11,TX}$	TX common mode return loss	10 MHz to 1250 MHz	12	14	-	dB
		1250 MHz to 2500 MHz	8	10	-	dB
		2500 MHz to 3000 MHz	9	9	-	dB

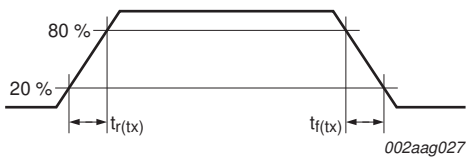


Fig 11. Output rise and fall times

11.4 Jitter performance

Table 12 provides jitter performance of PTN36241G under a specific set of conditions that is illustrated by Figure 8.

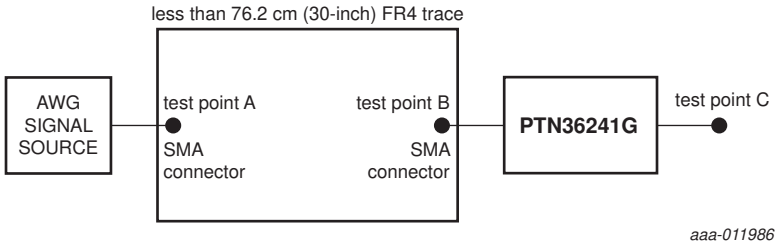
Table 12. Jitter performance characteristics

Unit Interval (UI) = 200 ps.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{jit(o)(p-p)}$	peak-to-peak output jitter time	total jitter at test point C [1]	-	0.19	-	UI
$t_{jit(dtrm)(p-p)}$	peak-to-peak deterministic jitter time	[1]	-	0.11	-	UI
$t_{jit(rndm)(p-p)}$	peak-to-peak random jitter time	[1][2]	-	0.08	-	UI

[1] Measured at test point C with K28.5 pattern, V_{ID} = 1000 mV (peak-to-peak), 5 Gbit/s; –3.1 dB de-emphasis from source.

[2] Random jitter calculated as 14.069 times the RMS random jitter for 10^{-12} bit error rate.



Source jitter measurements:

total jitter = 21 ps

deterministic jitter = 8 ps

random jitter (RMS value) = 0.95 ps

Fig 12. Jitter measurement setup

11.5 Ternary control inputs C1 and C2

Table 13. Ternary control inputs for C1 and C2 pins

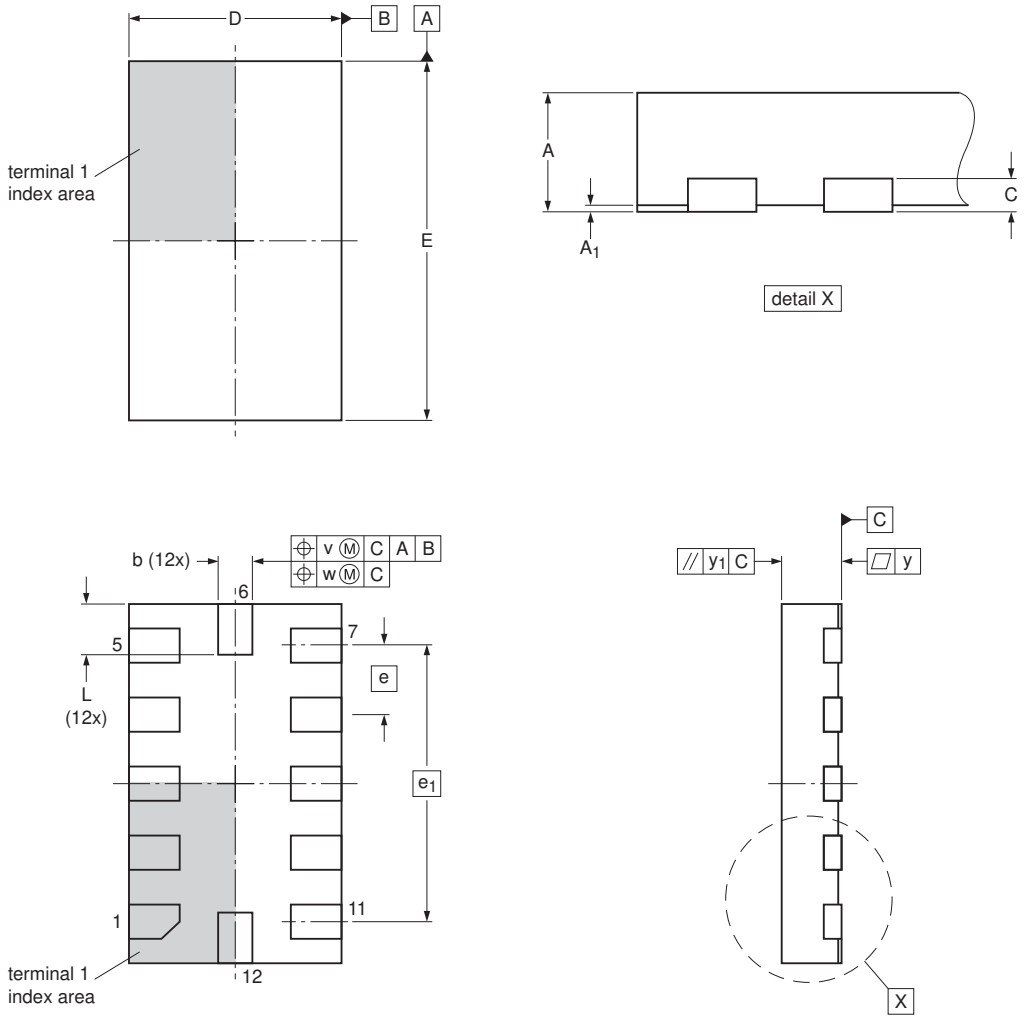
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	Trigger level of the Schmitt Trigger buffer when input is going from LOW to HIGH	0.70 × V_{DD}	V_{DD}	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage	Trigger level of the Schmitt Trigger buffer when input is going from HIGH to LOW	–0.3	0	0.30 × V_{DD}	V
$R_{pu(ext)}$	external pull-up resistor	connected between VDD1V8 and setting pin; for detection of HIGH condition	0	-	30	kΩ
$R_{pd(ext)}$	external pull-down resistor	connected between setting pin and GND; for detection of LOW condition	0	-	30	kΩ
$Z_{ext(OPEN)}$	external impedance	for detection of OPEN condition	250	-	-	kΩ
I_{IL}	LOW-level input current	setting pin is driven LOW by external GPIO	–45	-	-	μA

Table 13. Ternary control inputs for C1 and C2 pins *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	setting pin is driven HIGH (to 1.8 V) by external GPIO	-	-	+45	μA
$I_{Lext(OPEN)}$	external leakage current	of external GPIO; for reliable detection of OPEN condition	−6	-	+6	μA
$C_{L(ext)}$	external load capacitance	on setting pin; for reliable detection of OPEN condition	-	-	150	pF
$R_{pu(int)}$	internal pull-up resistance	for detection of Ternary setting	-	50	-	kΩ
$R_{pd(int)}$	internal pull-down resistance	for detection of Ternary setting	-	50	-	kΩ

12. Package outline

X2QFN12: plastic, super thin quad flat package; no leads; 12 terminals; body 2.10 x 1.25 x 0.35 mm **SOT1408-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	C	D	E	e	e_1	L	v	w	y	y_1
mm	max	0.40	0.05	0.25		1.30	2.15			0.35				
	nom	0.35	0.02	0.20	0.10	1.25	2.10	0.4	1.6	0.30	0.07	0.05	0.08	0.1
	min	0.30	0.00	0.15		1.20	2.05			0.25				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1408-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1408-1		MO-255				~~15-01-15~~ 15-01-19

Fig 13. Package outline SOT1408-1 (X2QFN12)

13. Packing information

13.1 SOT1408-1 (X2QFN12); Reel dry pack, SMD, 7"; Q1/T1 standard product orientation; Orderable part number ending ,515 or Z; Ordering code (12NC) ending 515

13.1.1 Packing method

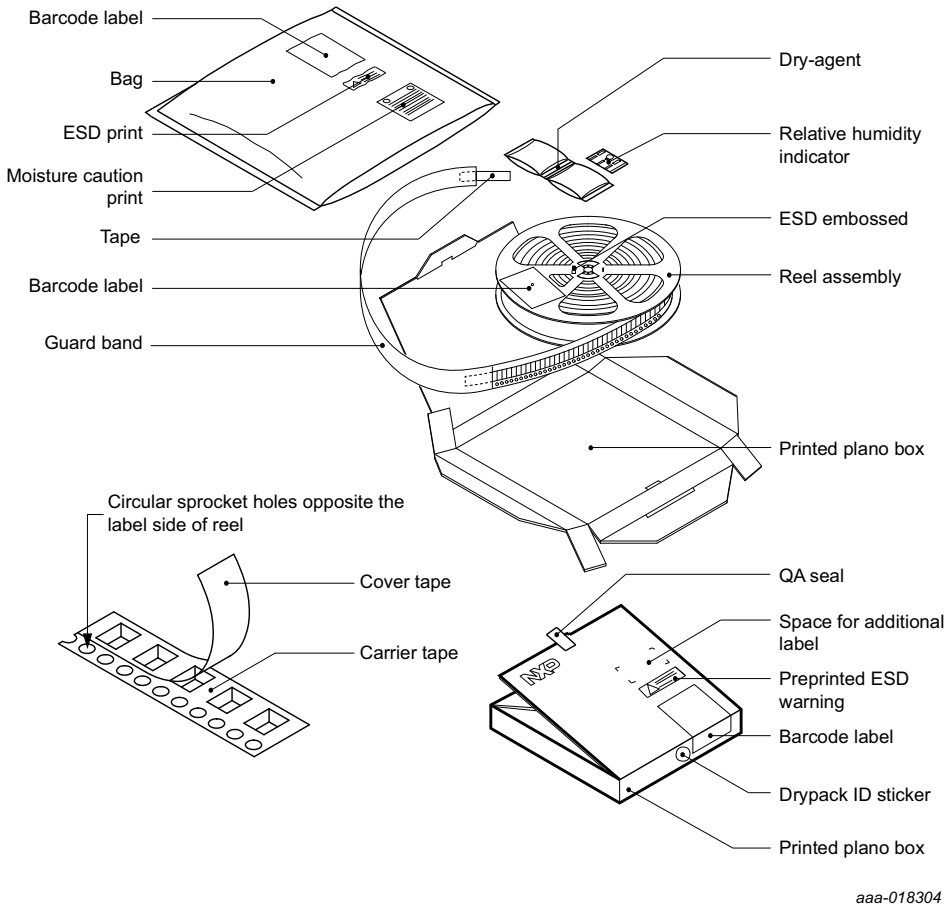


Fig 14. Reel dry pack for SMD

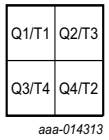
Table 14. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
180 × 8	6000	1	209 × 206 × 34

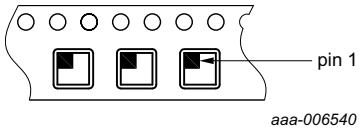
[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.
View ordering and availability details at NXP order portal, or contact your local NXP representative.

13.1.2 Product orientation



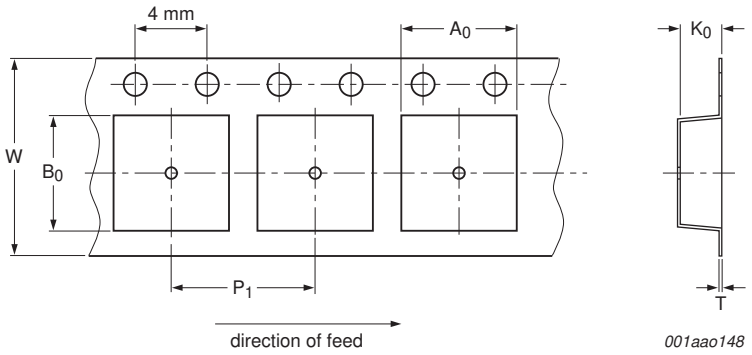
Tape pocket quadrants



Pin 1 is in quadrant Q1/T1

Fig 15. Product orientation in carrier tape

13.1.3 Carrier tape dimensions



Not drawn to scale.

Fig 16. Carrier tape dimensions

Table 15. Carrier tape dimensions
In accordance with IEC 60286-3.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
1.55 ± 0.1	2.40 ± 0.1	0.5 ± 0.05	0.25 ± 0.05	4.0 ± 0.1	8.0 ± 0.3

13.1.4 Reel dimensions

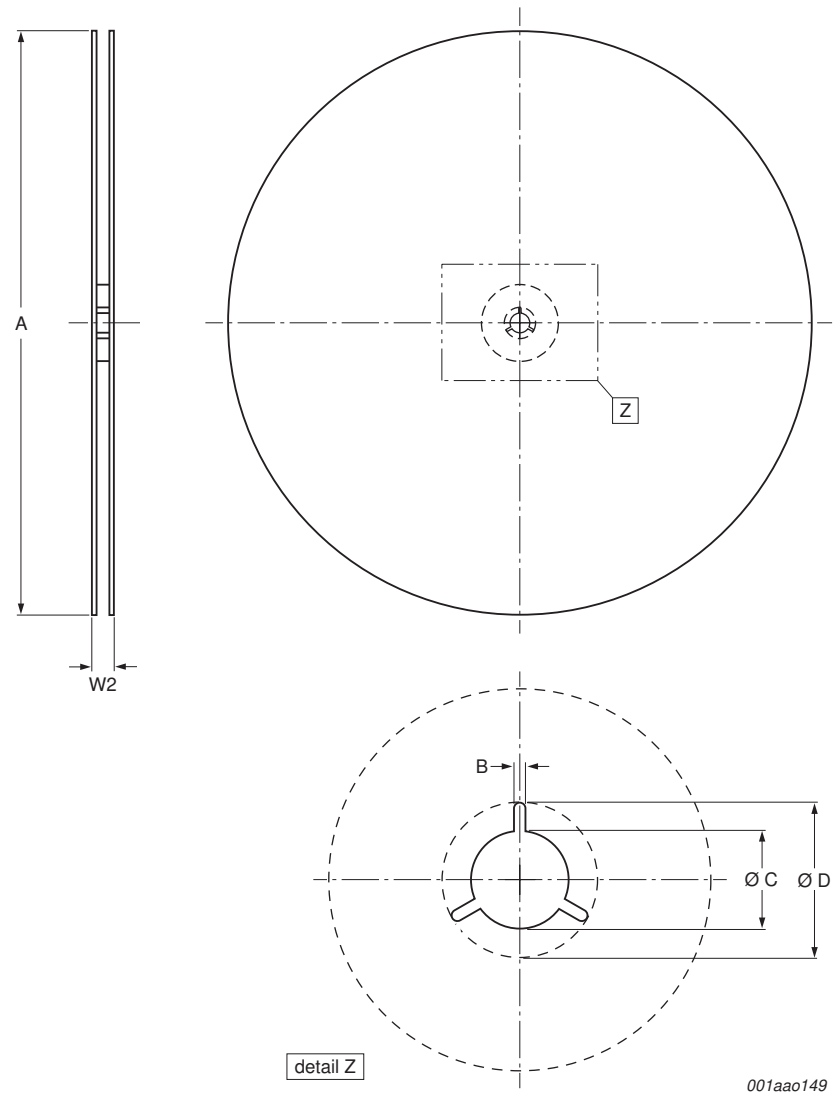


Fig 17. Schematic view of reel

Table 16. Reel dimensions

In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
180	14.4	1.5	12.8	20.2

13.1.5 Barcode label

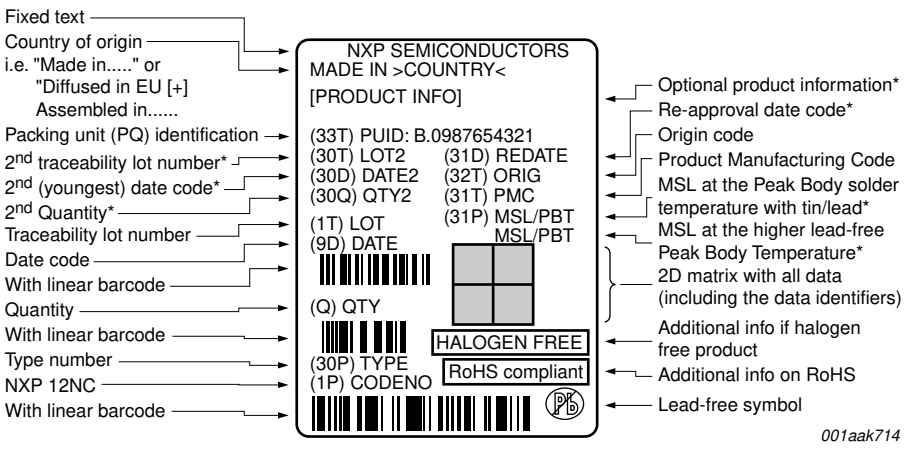


Fig 18. Example of typical box and reel information barcode label

Table 17. Barcode label dimensions

Box barcode label l × w (mm)	Reel barcode label l × w (mm)
100 × 75	100 × 75

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities