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PTN3700

1.8 V simple mobile interface link bridge IC

Rev. 3 — 12 October 2011 Product data sheet

1. General description

The PTN3700 is a 1.8 V simple mobile interface link bridge IC which can function both as a transmitter-serializer or a receiver-deserializer for RGB888 video data. When configured as transmitter (using input pin TX/$\overline{RX}$), the PTN3700 serializes parallel CMOS video input data into 1, 2 or 3 subLVDS-based high-speed serial data channels. When configured as receiver, the PTN3700 deserializes up to 3 high-speed serial data channels into parallel CMOS video data signals.

The parallel interface of the PTN3700 is based on the conventional and widely used 24-bit wide data bus for RGB video data, plus active LOW $\overline{HS}$ (Horizontal Synchronization) and $\overline{VS}$ (Vertical Synchronization) signals, and an active HIGH DE (Data Enable) signal. An additional two auxiliary bits A[1:0] are provided to permit signaling of miscellaneous status or mode information across the link to the display. The serial interface link of the PTN3700 is based on the open Simple Mobile Interface Link (SMILi) definition. In order to keep power low while accommodating various display sizes (e.g., up to 24-bit, 60 frames per second XVGA), the number of high-speed serial channels ('lanes') is configurable from 1 to 3 depending on the bandwidth needed. The data link speed is determined by the PCLK (Pixel Clock) rate and the number of serial channels selected.

In order to maintain a low power profile, the PTN3700 has three power modes, determined by detection of an active input clock and by shutdown pin $\overline{XSD}$. In Shutdown mode ($\overline{XSD}$ = LOW), the PTN3700 is completely inactive and consumes a minimum of current. In Standby mode ($\overline{XSD}$ = HIGH), the device is ready to switch to Active mode as soon as an active input clock signal is detected, and assume normal link operation.

In Transmitter mode, the PTN3700 performs parity calculation on the input data (R[7:0], G[7:0], B[7:0] plus $\overline{HS}$, $\overline{VS}$ and DE data bits) and adds an odd parity bit CP to the serial transmitted data stream. The PTN3700 in Receiver mode also integrates a parity checking function, which checks for odd parity across the decoded input word (R[7:0], G[7:0], B[7:0] plus $\overline{HS}$, $\overline{VS}$ and DE data bits), and indicates whether a parity error has occurred on its CPO out pin (active HIGH). When a parity error occurs, the most recent error-free pixel data will be output instead of the received invalid pixel data.

PTN3700 in Receiver mode offers an optional advanced frame mixing feature, which allows 18-bit displays to effectively display 24-bit color resolution by applying a patent-pending pixel data processing algorithm to the 24-bit video input data.

One of two serial transmission methods is selectable: pseudo source synchronous transmission based on the pixel clock, or true source synchronous transmission based on the bit clock. The latter uses a patent-pending methodology characterized by zero overhead and operation guaranteed free from false pixel synchronization.

The PTN3700 automatically rotates the order of the essential signals (parallel CMOS and high-speed serial data and clock) depending on whether it is operating as transmitter or as receiver (using pin TX/$\overline{RX}$). In addition, two Pinning Select bits (inputs PSEL[1:0]) allow for four additional signal order configurations. This allows for various topologies of printed circuit board or flex foil layout without crossing of traces, and enables the easy introduction of PTN3700 into an existing 'parallel' design avoiding board re-layout.

The PTN3700 is available in a 56-ball VFBGA package and operates across a temperature range of −40 °C to +85 °C.

2. Features and benefits

- Configurable as either Transmitter or Receiver
- One of two serial transmission methods selectable (pixel clock referenced pseudo source synchronous or bit clock referenced true source synchronous)
- 3 differential subLVDS high-speed serial lanes
- One differential pixel clock
- Configurable aggregate data bandwidth allowing up to 24-bit color, 60 fps XGA:
  - 1 lane at 30× serialization rate up to 650 Mbit/s
  - 2 lanes at 15× serialization rate up to 1300 Mbit/s
  - 3 lanes at 10× serialization rate up to 1.95 Gbit/s
- Parity encoding (transmitter) and detection (receiver) with last valid pixel repetition
- Advanced Frame Mixing function (in Receiver mode) for 24-bit color depth using conventional 18-bit displays or specially adapted '18-bit plus' displays
- Parallel CMOS I/O based on interface definition of RGB888 plus $\overline{HS}$, $\overline{VS}$, DE
- Very low power profile:
  - Shutdown mode for minimum idle power (< 3 μA typical)
  - Low-power Standby mode with input clock frequency auto-detect (< 3 μA typical)
  - Low active transmitter power: 18 mW (typ.) for QVGA[1] and 40 mW (typ.) for WVGA[2]
  - Low active receiver power: 15 mW (typ.) for QVGA and 36 mW (typ.) for WVGA
- Slew rate control on receiver parallel CMOS outputs
- Operates from a single 1.8 V ± 150 mV power supply
- Configurable mirroring pinout (dependent on Tx or Rx mode and PSEL[1:0] inputs) for optimum single layer flex-foil flow-through in various application scenarios
- Available in 56-ball VFBGA package

3. Applications

- High-resolution mobile phones
- Portable applications with video display capability

1. QVGA: 240 × 320 pixels at 60 Hz frame rate; 20 % non-active display data overhead; PCLK at 5.5 MHz; one-lane operation at 166 Mbit/s; 24-bit color data.
2. WVGA: 854 × 480 pixels at 60 Hz frame rate; 20 % non-active display data overhead; PCLK at 29.5 MHz; two-lane operation at 885.4 Mbit/s; 24-bit color data.

4. Ordering information

Table 1. Ordering information

Type number	Solder process	Package		
		Name	Description	Version
PTN3700EV/G	Pb-free (SnAgCu solder ball compound)	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4 × 4.5 × 0.65 mm[1]	SOT991-1

[1] 0.5 mm ball pitch; 1.0 mm maximum package height.

4.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
PTN3700EV/G	3700	−40 °C to +85 °C

5. Functional diagram

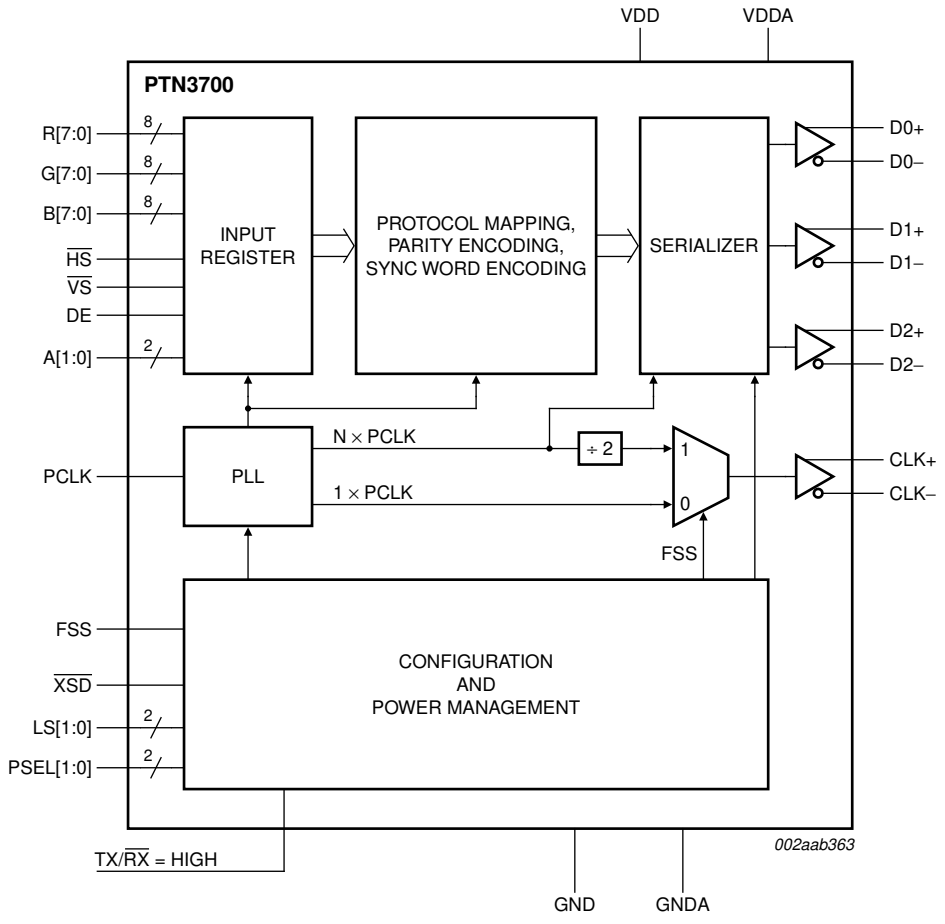


Fig 1. Functional diagram of PTN3700 in Transmitter mode

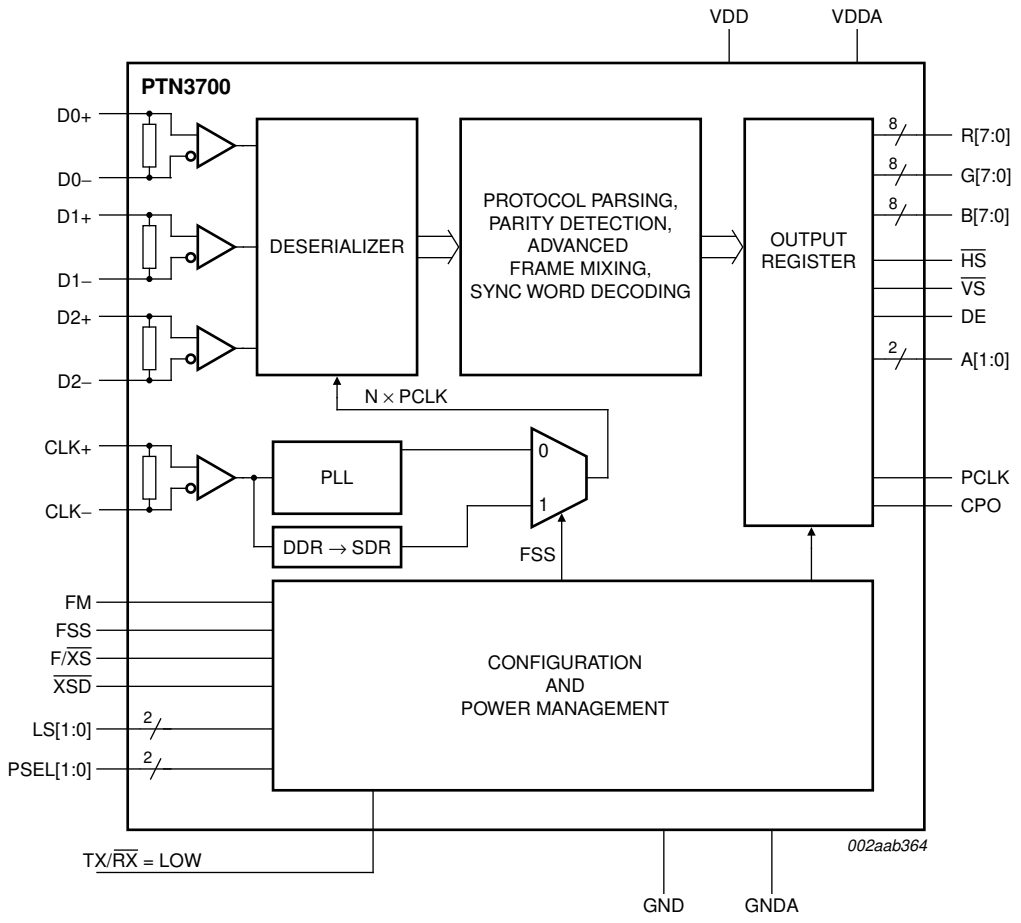
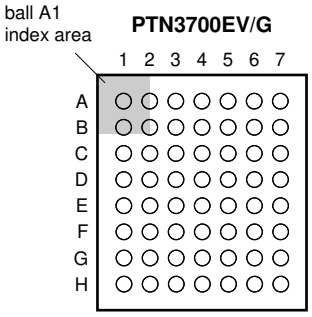


Fig 2. Functional diagram of PTN3700 in Receiver mode

6. Pinning information

6.1 Pinning



Transparent top view

Fig 3. Ball configuration for VFBGA56

	1	2	3	4	5	6	7
A	D2+	VDDA	DE	$\overline{HS}$	B0	B2	B4
B	D2−	GNDA	$\overline{VS}$	PCLK	B1	B3	B5
C	D1+	TX/$\overline{RX}$	A1	GND	VDD	B6	B7
D	D1−	VDD	PSEL0	LS0	FM	G0	G1
E	CLK+	GND	PSEL1	LS1	FSS	G2	G3
F	CLK−	F/$\overline{XS}$	A0	GND	VDD	G4	G5
G	D0+	$\overline{XSD}$	R6	R4	R2	R0	G6
H	D0−	CPO	R7	R5	R3	R1	G7

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56-ball, 7 × 8 grid; transparent top view

Fig 4. VFBGA56 ball mapping - Transmitter mode (TX/RX = HIGH); PSEL[1:0] = 00b

	1	2	3	4	5	6	7
A	D2+	VDDA	DE	$\overline{HS}$	R7	R5	R3
B	D2−	GNDA	$\overline{VS}$	PCLK	R6	R4	R2
C	D1+	TX/$\overline{RX}$	A1	GND	VDD	R1	R0
D	D1−	VDD	PSEL0	LS0	FM	G7	G6
E	CLK+	GND	PSEL1	LS1	FSS	G5	G4
F	CLK−	F/$\overline{XS}$	A0	GND	VDD	G3	G2
G	D0+	$\overline{XSD}$	B1	B3	B5	B7	G1
H	D0−	CPO	B0	B2	B4	B6	G0

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56-ball, 7 × 8 grid; transparent top view

Fig 5. VFBGA56 ball mapping - Transmitter mode (TX/RX = HIGH); PSEL[1:0] = 01b

	1	2	3	4	5	6	7
A	D0−	VDDA	DE	$\overline{HS}$	B0	B2	B4
B	D0+	GNDA	$\overline{VS}$	PCLK	B1	B3	B5
C	CLK−	TX/$\overline{RX}$	A1	GND	VDD	B6	B7
D	CLK+	VDD	PSEL0	LS0	FM	G0	G1
E	D1−	GND	PSEL1	LS1	FSS	G2	G3
F	D1+	F/$\overline{XS}$	A0	GND	VDD	G4	G5
G	D2−	$\overline{XSD}$	R6	R4	R2	R0	G6
H	D2+	CPO	R7	R5	R3	R1	G7

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56-ball, 7 × 8 grid; transparent top view

Fig 6. VFBGA56 ball mapping - Transmitter mode (TX/RX = HIGH); PSEL[1:0] = 10b

	1	2	3	4	5	6	7
A	D0−	VDDA	DE	$\overline{HS}$	R7	R5	R3
B	D0+	GNDA	$\overline{VS}$	PCLK	R6	R4	R2
C	CLK−	TX/$\overline{RX}$	A1	GND	VDD	R1	R0
D	CLK+	VDD	PSEL0	LS0	FM	G7	G6
E	D1−	GND	PSEL1	LS1	FSS	G5	G4
F	D1+	F/$\overline{XS}$	A0	GND	VDD	G3	G2
G	D2−	$\overline{XSD}$	B1	B3	B5	B7	G1
H	D2+	CPO	B0	B2	B4	B6	G0

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56-ball, 7 × 8 grid; transparent top view

Fig 7. VFBGA56 ball mapping - Transmitter mode (TX/RX = HIGH); PSEL[1:0] = 11b

	1	2	3	4	5	6	7
A	D2+	VDDA	R7	R5	R3	R1	G7
B	D2−	GNDA	R6	R4	R2	R0	G6
C	D1+	TX/$\overline{RX}$	A1	GND	VDD	G5	G4
D	D1−	VDD	PSEL0	LS0	FM	G3	G2
E	CLK+	GND	PSEL1	LS1	FSS	G1	G0
F	CLK−	F/$\overline{XS}$	A0	GND	VDD	B7	B6
G	D0+	$\overline{XSD}$	$\overline{VS}$	PCLK	B1	B3	B5
H	D0−	CPO	DE	$\overline{HS}$	B0	B2	B4

002aac382

56-ball, 7 × 8 grid; transparent top view

Fig 8. VFBGA56 ball mapping - Receiver mode (TX/$\overline{RX}$ = LOW); PSEL[1:0] = 00b

	1	2	3	4	5	6	7
A	D2+	VDDA	B0	B2	B4	B6	G0
B	D2−	GNDA	B1	B3	B5	B7	G1
C	D1+	TX/$\overline{RX}$	A1	GND	VDD	G2	G3
D	D1−	VDD	PSEL0	LS0	FM	G4	G5
E	CLK+	GND	PSEL1	LS1	FSS	G6	G7
F	CLK−	F/$\overline{XS}$	A0	GND	VDD	R0	R1
G	D0+	$\overline{XSD}$	$\overline{VS}$	PCLK	R6	R4	R2
H	D0−	CPO	DE	$\overline{HS}$	R7	R5	R3

002aac383

56-ball, 7 × 8 grid; transparent top view

Fig 9. VFBGA56 ball mapping - Receiver mode (TX/$\overline{RX}$ = LOW); PSEL[1:0] = 01b

	1	2	3	4	5	6	7
A	D0−	VDDA	R7	R5	R3	R1	G7
B	D0+	GNDA	R6	R4	R2	R0	G6
C	CLK−	TX/$\overline{RX}$	A1	GND	VDD	G5	G4
D	CLK+	VDD	PSEL0	LS0	FM	G3	G2
E	D1−	GND	PSEL1	LS1	FSS	G1	G0
F	D1+	F/$\overline{XS}$	A0	GND	VDD	B7	B6
G	D2−	$\overline{XSD}$	$\overline{VS}$	PCLK	B1	B3	B5
H	D2+	CPO	DE	$\overline{HS}$	B0	B2	B4

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56-ball, 7 × 8 grid; transparent top view

Fig 10. VFBGA56 ball mapping - Receiver mode (TX/$\overline{RX}$ = LOW); PSEL[1:0] = 10b

	1	2	3	4	5	6	7
A	D0−	VDDA	B0	B2	B4	B6	G0
B	D0+	GNDA	B1	B3	B5	B7	G1
C	CLK−	TX/$\overline{RX}$	A1	GND	VDD	G2	G3
D	CLK+	VDD	PSEL0	LS0	FM	G4	G5
E	D1−	GND	PSEL1	LS1	FSS	G6	G7
F	D1+	F/$\overline{XS}$	A0	GND	VDD	R0	R1
G	D2−	$\overline{XSD}$	$\overline{VS}$	PCLK	R6	R4	R2
H	D2+	CPO	DE	$\overline{HS}$	R7	R5	R3

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56-ball, 7 × 8 grid; transparent top view

Fig 11. VFBGA56 ball mapping - Receiver mode (TX/$\overline{RX}$ = LOW); PSEL[1:0] = 11b

6.2 Pin description

Table 3. Pin description - Transmitter mode

Symbol	Pin[1]	Type	Description
Parallel data inputs			
R[7:0], G[7:0], B[7:0]		CMOS	8-bit wide R, G, B pixel data inputs
$\overline{HS}$		CMOS	Horizontal synchronization data input, active LOW
$\overline{VS}$		CMOS	Vertical synchronization data input, active LOW
DE		CMOS	Data Enable input, active HIGH
A0, A1		CMOS	Auxiliary input bits
High-speed serial outputs			
D0+, D0−, D1+, D1−, D2+, D2−		SubLVDS driver	Serialized high-speed differential subLVDS data outputs
CLK+, CLK−		SubLVDS driver	Serialized high-speed differential subLVDS clock outputs
Clock inputs			
PCLK		CMOS	Pixel clock reference input
Configuration inputs			
TX/$\overline{RX}$		CMOS	Transmitter/Receiver configuration input pin. When HIGH, PTN3700 is configured as transmitter.
LS0, LS1		CMOS	Serialization mode program pins. Select between 1, 2 or 3 lanes. See Table 5.
PSEL0, PSEL1		CMOS	Pin mirroring select pins. See Table 6 and Table 7
$\overline{XSD}$		CMOS	Shutdown mode input pin, active LOW, puts PTN3700 in lowest-power mode by deactivating all circuitry. When HIGH, PTN3700 is either in Active mode or awaiting clock input (Standby mode)
FSS		CMOS	Fully Source Synchronous select pin. When LOW, PTN3700 uses pseudo source synchronous serial transmission mode with the pixel clock as both the reference frequency and the frame boundary delineation. When HIGH, PTN3700 uses true source synchronous transmission with a serial Double Data Rate (DDR) bit clock for the serial data. Embedded synchronization words are encoded for pixel synchronization. On both Receiver and Transmitter, the settings of the FSS pin should match. Otherwise the link will not function.
Power supply			
VDD		power	power supply voltage
VDDA		power	analog (PLL) power supply voltage
GNDA		ground	analog (PLL) ground
GND		ground	ground
Miscellaneous			
CPO, FM, F/$\overline{XS}$		CMOS	Signals are inactive in Transmitter mode and should be tied down to GND.

[1] Depends on configuration.

Table 4. Pin description - Receiver mode

Symbol	Pin[1]	Type	Description
Parallel data outputs			
R[7:0], G[7:0], B[7:0]		CMOS	8-bit wide R, G, B pixel data outputs
$\overline{HS}$		CMOS	Horizontal synchronization data output, active LOW
$\overline{VS}$		CMOS	Vertical synchronization data output, active LOW
DE		CMOS	Data Enable output, active HIGH
A0, A1		CMOS	Auxiliary output bits
High-speed serial inputs			
D0+, D0−, D1+, D1−, D2+, D2−		SubLVDS receiver	Serialized high-speed differential subLVDS data inputs
CLK+, CLK−		SubLVDS receiver	Serialized high-speed differential subLVDS clock inputs
Clock outputs			
PCLK		CMOS	Pixel clock output
Configuration inputs			
TX/$\overline{RX}$		CMOS	Transmitter/Receiver configuration input pin. When LOW, PTN3700 is configured as receiver.
LS0, LS1		CMOS	Serialization mode program pins. Select between 1, 2 or 3 lanes. See Table 5.
PSEL0, PSEL1		CMOS	Pin mirroring select pins. See Table 6 and Table 7.
$\overline{XSD}$		CMOS	Shutdown mode input pin, active LOW, puts PTN3700 in lowest-power mode by deactivating all circuitry. When HIGH, PTN3700 is either in Active mode or awaiting clock input (Standby mode).
F/$\overline{XS}$		CMOS	Program pin for fast (F/$\overline{XS}$ = HIGH) or slow (F/$\overline{XS}$ = LOW) parallel output and PCLK slew rate
FM		CMOS	Frame Mixing select pin. When LOW, Frame Mixing is disabled and PTN3700 passes 24-bit video data transparently. When HIGH, Frame Mixing is enabled and PTN3700 applies processing to the 24-bit video data resulting in 18-bit output data words encoded with 24-bit color depth. Frame Mixing is only available in Receiver mode.
FSS		CMOS	Fully Source Synchronous select pin. When LOW, PTN3700 uses pseudo source synchronous serial reception mode with the pixel clock as both the reference frequency and the frame boundary delineation. When HIGH, PTN3700 uses true source synchronous reception with embedded synchronization word decoding, with the bit clock as reference frequency. On both Receiver and Transmitter, the settings of the FSS pin should match. Otherwise the link will not function.
Parity output			
CPO		CMOS	Parity error output, active HIGH. A HIGH level indicates a parity error was detected in the current pixel data
Power supply			
VDD			power supply voltage
VDDA			analog (PLL) power supply voltage
GNDA			analog (PLL) ground
GND			ground

[1] Depends on configuration.

7. Functional description

7.1 General

A complete simple mobile interface link consists of one PTN3700 configured as transmitter (see Figure 1); two, three or four differential-pair high-speed signaling channels; and one PTN3700 configured as receiver (see Figure 2). Link power and ground are supplied to pins VDD and GND respectively (power and ground should be routed and decoupled to analog supply pin VDDA and ground pin GNDA separately for lowest jitter operation). Configuration of either transmitter or receiver mode is achieved by strapping the CMOS input pin TX/$\overline{\text{RX}}$ HIGH or LOW, respectively.

Configured as transmitter, PTN3700 accepts parallel CMOS input data including color pixel data (R[7:0], G[7:0], B[7:0]), three control bits $\overline{\text{HS}}$ (horizontal synchronization), $\overline{\text{VS}}$ (vertical synchronization), DE (data enable), auxiliary bits A[1:0] and pixel clock PCLK. The PTN3700 calculates a parity bit (excluding the auxiliary bits, see Section 7.6) and serializes the data and outputs as a high-speed serial data stream on up to three subLVDS differential outputs (D0+, D0−, D1+, D1−, D2+, D2−) depending on the serialization mode selected by pins LS[1:0] (see Section 7.2). An integrated low-jitter PLL generates internally the bit clock used for serialization of video input data, parity bit and control bits, and outputs along with the serial output data a differential pixel clock on differential subLVDS output pair CLK+ and CLK−.

Configured as receiver, PTN3700 accepts serial differential data inputs D0+, D0−, D1+, D1−, D2+, D2− and differential input clock CLK+ and CLK− from the signaling channel and deserializes the received data into parallel output data on pins R[7:0], G[7:0], B[7:0], $\overline{\text{HS}}$, $\overline{\text{VS}}$, DE and A[1:0] along with the PLL-regenerated pixel clock PCLK. Also, a parity checking function is performed on the incoming R[7:0], G[7:0], B[7:0], $\overline{\text{HS}}$, $\overline{\text{VS}}$, DE bits and an error flagged by signaling a HIGH state on CMOS output pin CPO (see Section 7.6). Serialization mode pins LS[1:0] need to be selected according to the expected serialization mode (see Section 7.2) to correctly receive and decode the up to three subLVDS differential serial inputs. To minimize EMI, the parallel outputs can be configured by tying pin F/$\overline{\text{XS}}$ either HIGH or LOW to output fast or slow output slew rates respectively.

The PTN3700 is capable of operating in either of two distinct transmission modes: Pseudo Source Synchronous mode (PSS), and Full (or ‘true’) Source Synchronous mode (FSS), selected by CMOS input pin FSS. In PSS mode, the pixel clock PCLK is used both as the transmission frequency reference and its rising edge as the delineation of the start of a pixel. This transmission mode relies on the Receiver PLL to reconstruct the bit clock at the receiving end. In FSS mode, the bit clock is transmitted (in DDR mode) instead of the pixel clock. Rather than achieve frame boundary detection using the pixel clock edge as in PSS mode, in FSS mode the Transmitter encodes ‘synchronization words’ over the link which are detected and used for data to pixel alignment by the Receiver. This methodology guarantees false-synchronization-free transmission with zero protocol overhead.

The PTN3700 can be put into very low ‘Shutdown’ power state by tying CMOS input pin $\overline{\text{XSD}}$ LOW. Additionally, the PTN3700 will automatically enter a low-power ‘Standby’ mode when no active input clock is detected on its inputs (see Section 7.5).

7.2 Link programmability

The number of high-speed serial channels used is programmed by CMOS input pins LS[1:0]. For a given link consisting of a transmitter and receiver pair of PTN3700's, the number of channels used must be programmed identically or the link will malfunction. The PTN3700, once programmed, will assume the corresponding serialization ratio as shown in Table 5. When pins LS[1:0] are both HIGH, the PTN3700 is put in a test mode which is used for production testing purposes only and should not be used in application.

The 1-lane mode is typically meant for smaller video display formats (e.g., QVGA to HVGA), while the 2-lane mode is typically used for display formats like HVGA and VGA. The 3-lane mode supports larger display formats such as VGA or XGA. Please see Section 12.1 for more information.

Table 5. Link programmability

LS1	LS0	Mode	Number of high-speed serial channels	Supported PCLK frequency range (MHz)	Guaranteed data bandwidth per channel (Mbit/s)	Guaranteed aggregate link bandwidth (Mbit/s)
L	L	00	1	4.0 to 21.6	120 to 650	650
L	H	01	2	8.0 to 43.3	120 to 650	1300
H	L	10	3	20.0 to 65.0	200 to 650	1950
H	H	11	reserved[1]	reserved	reserved	reserved

[1] Mode 11 is used for test purposes only.

7.3 Versatile signal mirroring programmability

In order to provide flexibility for different signal order and flow requirements in different applications, the PTN3700 can be programmed to mirror its signal order for the parallel and serial I/Os independently using the PSEL[1:0] inputs. The signal order also changes as a function of the TX/$\overline{RX}$ input by mirroring signals in such a way that the Transmitter and Receiver in a given link can be connected without signal crossings by simply opposing the two instances of PTN3700 and rotating one of them by 180 degrees. The truth table for the versatile signal mirroring scheme is shown in Table 6 and Table 7. The individual ball mappings are given in Figure 4 through Figure 11.

Table 6. Versatile signal mirroring programmability - Parallel I/O

Ball location[1]	TX/$\overline{RX}$			
	L		H	
	PSEL0			
	L	H	L	H
	(Receive mode)		(Transmit mode)	
H3	DE	DE	R7	B0
G3	$\overline{VS}$	$\overline{VS}$	R6	B1
H4	$\overline{HS}$	$\overline{HS}$	R5	B2
G4	PCLK	PCLK	R4	B3
H5	B0	R7	R3	B4
G5	B1	R6	R2	B5
H6	B2	R5	R1	B6
G6	B3	R4	R0	B7
H7	B4	R3	G7	G0
G7	B5	R2	G6	G1
F7	B6	R1	G5	G2
F6	B7	R0	G4	G3
E7	G0	G7	G3	G4
E6	G1	G6	G2	G5
D7	G2	G5	G1	G6
D6	G3	G4	G0	G7
C7	G4	G3	B7	R0
C6	G5	G2	B6	R1
B7	G6	G1	B5	R2
A7	G7	G0	B4	R3
B6	R0	B7	B3	R4
A6	R1	B6	B2	R5
B5	R2	B5	B1	R6
A5	R3	B4	B0	R7
B4	R4	B3	PCLK	PCLK
A4	R5	B2	$\overline{HS}$	$\overline{HS}$
B3	R6	B1	$\overline{VS}$	$\overline{VS}$
A3	R7	B0	DE	DE

[1] For PTN3700EV/G VFBGA56 package option. See also Figure 4 through Figure 11.

Table 7. Versatile signal mirroring programmability - Serial I/O

Ball location[1]	PSEL1	
	L	H
A1	D2+	D0−
B1	D2−	D0+
C1	D1+	CLK-
D1	D1−	CLK+
E1	CLK+	D1−
F1	CLK−	D1+
G1	D0+	D2−
H1	D0−	D2+

[1] For PTN3700EV/G VFBGA56 package option. See also Figure 4 through Figure 11.

7.4 High-speed data channel protocol options

The PTN3700 maps the transmission protocol in accordance with the serialization mode selected by pins LS[1:0]. In Mode 00 (1-channel), all RGB, parity and synchronization bits are serialized onto a single 30-bit sequence. In Mode 01 (2-channel), these bits are mapped onto two simultaneous 15-bit sequences divided across two lanes. In Mode 10 (3-channel), the 30 bits are serialized onto three simultaneous 10-bit sequences.

The serial bit mapping is different between pseudo-source-synchronous mode (FSS = LOW) and fully source-synchronous mode (FSS = HIGH). The mapping of the data bits in pseudo-source synchronous mode is shown in Figure 12, Figure 13 and Figure 14. (Note that the CLK in Mode 01 has an asymmetrical duty cycle of 8/15). The serial bit mapping in fully source-synchronous mode is shown in Figure 15, Figure 16 and Figure 17. Note that the fully source synchronous transmission mode is not dependent on the phase of PCLK for receiver synchronization.

7.4.1 Serial protocol bit mapping - pseudo source synchronous mode (FSS = LOW)

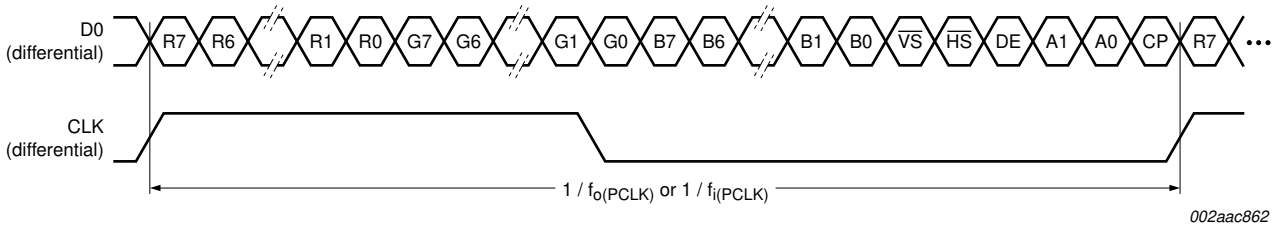


Fig 12. Mode 00 - single serial data channel mode (FSS = LOW)

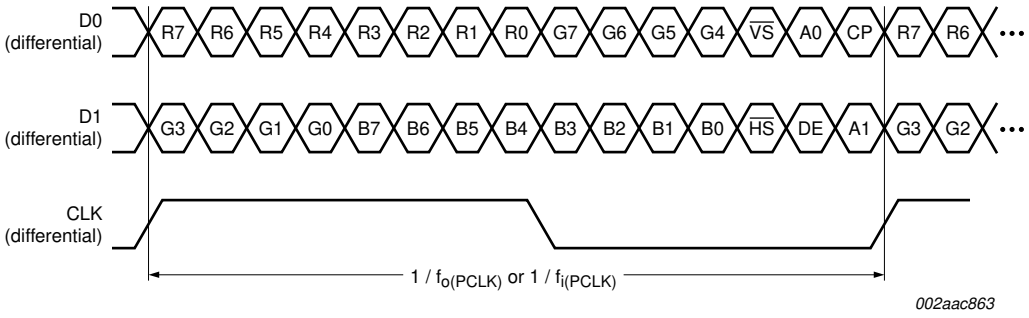


Fig 13. Mode 01 - dual serial data channel mode (FSS = LOW)

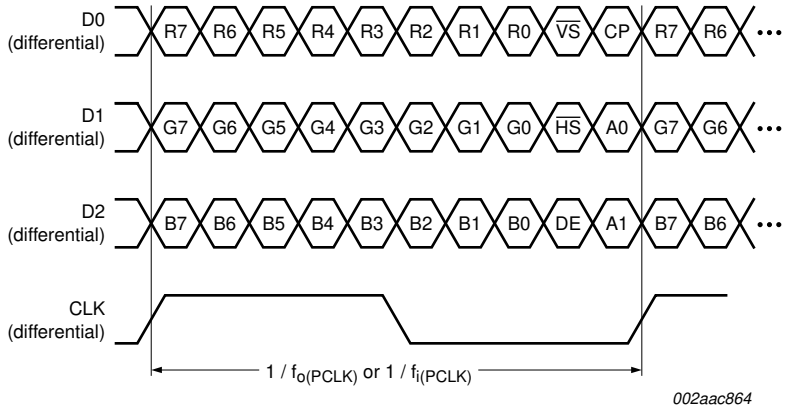


Fig 14. Mode 10 - triple serial data channel mode (FSS = LOW)

7.4.2 Serial protocol bit mapping - fully source synchronous mode (FSS = HIGH)

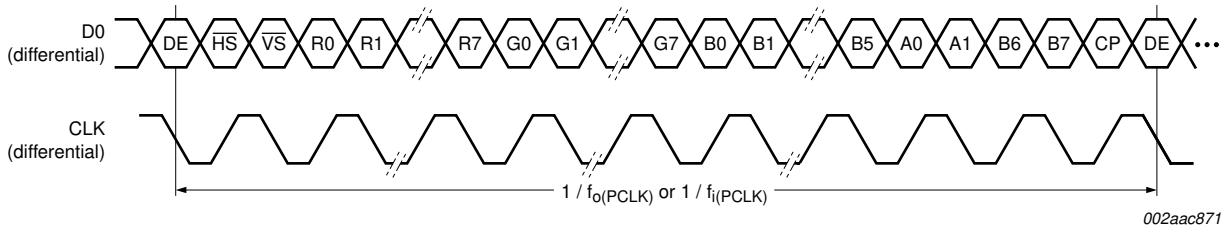


Fig 15. Mode 00 - single serial data channel mode (FSS = HIGH)

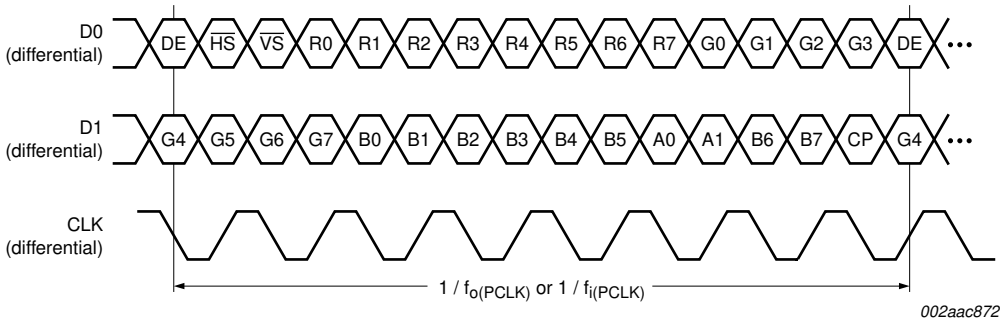


Fig 16. Mode 01 - dual serial data channel mode (FSS = HIGH)

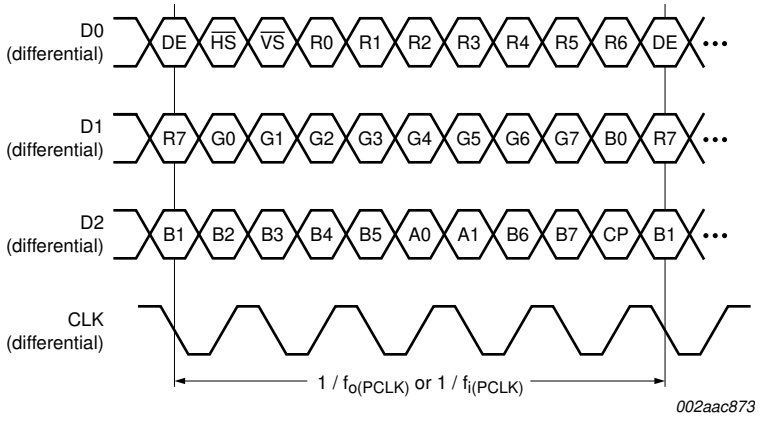


Fig 17. Mode 10 - triple serial data channel mode (FSS = HIGH)

7.4.3 PLL, PCLK, CLK and pixel synchronization

7.4.3.1 Pixel synchronization

PSS mode: The serial clock CLK provides the word boundaries explicitly for frame synchronization. At the receiver side, a PLL is needed to re-generate the bit clock, translating to a higher receiver power dissipation.

FSS mode: The serial clock CLK is truly synchronous with the serial data. Embedded synchronization words are transmitted in the non-active display area for pixel synchronization. The receiver PLL is powered down during this mode, hence the lower power consumption when compared with PSS mode. The special embedded synchronization words are guaranteed by design to never trigger false synchronization.

7.4.3.2 PLL

The PLL locks onto the PCLK input during transmit mode or the CLK input during receiver mode. It generates an internal high-speed clock, which is phase-aligned to the input clock. The PLL logic uses the lane select and transmit/receive status to determine the necessary PLL bandwidth settings and PLL divider values automatically. The PLL is able to track spread spectrum clocking to reduce EMI. The spread spectrum clock modulation frequency can be from 30 kHz to 33 kHz.

Transmitter: The internally generated clock is always aligned to the input clock PCLK.

- PSS mode: Refer to Section 7.4.1.
- FSS mode: The output clock CLK is Double Data Rate (DDR) and both clock edges are aligned to the data output.

Receiver:

- PSS mode: The PLL generates an internal clock at serial bit frequency and locks to the input clock CLK.
- FSS mode: The receiver uses Double Data Rate (DDR) input clock CLK, which is aligned to the data already.

7.4.4 $\overline{HS}$, $\overline{VS}$ and DE signal usage in various PTN3700 modes

When frame mixing is not used in PSS mode, $\overline{VS}$, $\overline{HS}$, DE, R[7:0], G[7:0], B[7:0] are treated as arbitrary user data. In this mode, PTN3700 functions as a pure serializer and deserializer, and is unaware of the meaning or polarity of $\overline{VS}$, $\overline{HS}$, DE, R[7:0], G[7:0], B[7:0]. In FSS mode, PTN3700 makes use of $\overline{VS}$, $\overline{HS}$ and DE to implement pixel synchronization with embedded sync words in the non-active display area.

When frame mixing is used, $\overline{VS}$, $\overline{HS}$, DE and R[7:0], G[7:0], B[7:0] are used to implement NXP-patented frame mixing algorithm.

Table 8 summarizes the requirements of $\overline{VS}$, $\overline{HS}$, DE and RGB in various modes.

Table 8. $\overline{VS}$, $\overline{HS}$, DE, and RGB requirements[1][2]

FSS	Mode	FM	$\overline{VS}$, $\overline{HS}$	DE	R, G, B	A[1:0]
LOW	PSS	HIGH	active LOW	active HIGH	R, G, B	X
		LOW	X	X	X	X
HIGH	FSS	HIGH	active LOW	active HIGH	R, G, B	X
		LOW	active LOW	active HIGH	X	X

[1] 'X' signifies that PTN3700 handles this signal transparently, i.e., data is transmitted and received as-is.

[2] 'R, G, B' signifies that R, G, B video data have to be input according to the exact chosen pin configuration of PTN3700, specifically:

a) Bit order reversal is not allowed, even if both the transmit data and receive data are reversed in bit order. For example, the MSB of 'R' color from video source must be input as 'R7'.

b) 'R' must be used for red color, 'G' for green color, and 'B' for blue color.

7.4.4.1 PSS mode

$\overline{HS}$, $\overline{VS}$ and DE are treated by PTN3700 in the same way as RGB signals in PSS mode; that is, $\overline{HS}$, $\overline{VS}$, and DE are serialized and transmitted transparently by the PTN3700 transmitter, and transparently received and deserialized by PTN3700 receiver. Data Enable (DE) signal is typically used to signify the active display area from the non-active display area.

In the case that advanced frame mixing is not used:

- DE signal can be tied HIGH or LOW, for displays not using DE signal.
- $\overline{HS}$ and $\overline{VS}$ can be active HIGH or active LOW.

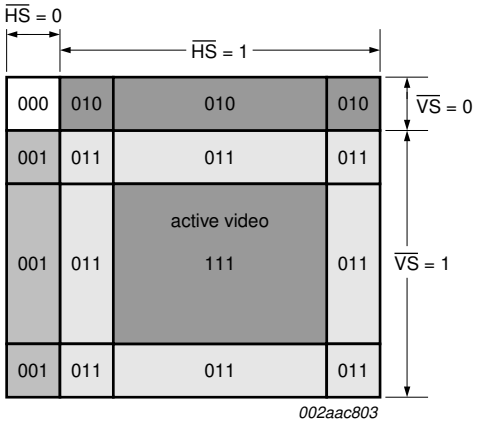
7.4.4.2 FSS mode

In FSS mode, PTN3700 uses true source synchronous transmission with a serial Double Data Rate (DDR) bit clock for the serial data.

FSS mode requires the following operating conditions:

- Active LOW $\overline{HS}$
- Active LOW $\overline{VS}$
- Active HIGH DE

In FSS mode, DE = 1 means active video, and PTN3700 generates embedded sync words when DE = 0. DE, $\overline{VS}$ and $\overline{HS}$ must be actively driven according to the typical video screen figure shown in Figure 18.



3 numbers correspond to [DE, HS, VS]

Fig 18. Typical video screen

7.5 Power modes

The PTN3700 has three different power modes to minimize power consumption of the link as a function of link activity: Shutdown mode, Standby mode, and Active mode. The truth table for the three power modes is shown in Table 9 and Table 10.

- **Shutdown mode:** By driving input pin $\overline{XSD}$ LOW, the PTN3700 assumes lowest power mode. All internal logic circuits are reset during this mode, and the link is completely inactive. The transmitter high-speed serial output channels are put in high-impedance state, and the receiver high-speed serial input channels are pulled LOW. The receiver CMOS parallel outputs will all be set HIGH with the exception of DE and PCLK which are reset LOW. However, the input buffers for the transmitter remain active, so it is recommended to stop PCLK and RGB data to achieve the lowest Shutdown mode power.
- **Standby mode:** When pin $\overline{XSD}$ is set HIGH but no input clock is active, the PTN3700 detects inactivity of the clock[3] and remains in a low-power Standby mode until an active input clock is detected. The transmitter serial outputs, receiver serial inputs and receiver parallel outputs all behave identically to their respective states in Shutdown mode.
- **Active mode:** When pin $\overline{XSD}$ is set HIGH and an active input clock is detected, PTN3700 will assume normal link operation. Current consumption depends on the PCLK frequency, number of lanes, FSS/PSS mode, data pattern, etc.

Table 9. Power modes - Transmitter mode

Inputs		Power mode	Outputs	
$\overline{XSD}$	PCLK		D0+, D0−, D1+, D1−, D2+, D2−	CLK+, CLK−
L	X	Shutdown	high-Z	high-Z
H	stopped	Standby	high-Z	high-Z
H	running	Active	active serial data	active

3. The PTN3700 clock detection circuit identifies the clock as inactive when the PCLK input signal frequency is less than 500 kHz.

Table 10. Power modes - Receiver mode

Inputs		State of serial data inputs D0+, D0−, D1+, D1−, D2+, D2−	Power mode	Data Outputs	
$\overline{XSD}$	CLK+, CLK−			R[7:0], G[7:0], B[7:0], HS, VS	DE, PCLK
L	X or floating	resistively pulled H or L	Shutdown	H	L
H	stopped	resistively pulled H or L	Standby	H	L
H	running	normal receiver state	Active	active data	active

7.6 Link error detection and correction

In Transmitter mode, PTN3700 calculates an odd parity bit and merges this into the serialized output data stream to allow the receiver to detect whether parity has been violated for its received input data. The parity bit CP is calculated across the 27-bit input data word (R[7:0], G[7:0], B[7:0], $\overline{HS}$, $\overline{VS}$ and DE) for every pixel transmitted, as shown in Table 11. Note that the auxiliary bits A[1:0] are excluded from the parity calculation.

Table 11. Parity encoding function table - Transmitter mode

Inputs			Encoded parity bit
$\overline{XSD}$	PCLK	$\sum$ of inputs = H (R[7:0], G[7:0], B[7:0], $\overline{HS}$, $\overline{VS}$, DE)	CP
H	running	odd	L
H	running	even	H
H	stopped	X or floating	undefined
L	X or floating	X or floating	undefined

In Receiver mode, the received encoded parity bit CP is compared against the received 27-bit input data word (R[7:0], G[7:0], B[7:0], $\overline{HS}$, $\overline{VS}$ and DE) for every pixel, and an error is flagged by setting parity error output CPO HIGH for the duration of the pixel clock period in which the error was detected. Note that the auxiliary output bits A[1:0] are excluded from the parity detection.

In addition, during the pixel clock period in which the error occurs, the last valid pixel word is output to R[7:0], G[7:0], B[7:0], $\overline{HS}$, $\overline{VS}$ and DE instead of the current erroneous pixel data. The last valid pixel word is defined as the data prior to the first parity error detected in any concatenation of parity errors.

If a parity error is detected but no valid previous pixel information is available, the receiver will output values R[7:0] = G[7:0] = B[7:0] = $\overline{HS}$ = $\overline{VS}$ = HIGH, and DE = LOW. The truth table for receiver parity function is shown in Table 12. Note that the auxiliary bits A[1:0] are not affected by the last valid pixel repetition.

Table 12. Parity decoding function table - Receiver mode

Inputs			Received parity bit	Parity output	Data outputs
$\overline{XSD}$	Clock	∑ of bits received in frame = H (R[7:0], G[7:0], B[7:0], HS, VS, DE)	CP	CPO	R[7:0], G[7:0], B[7:0], HS, VS, DE[1][2]
H	running	odd	L	L	RGB_n, $\overline{HS}_n$, $\overline{VS}_n$, DE_n
H	running	even	L	H	RGB_0, $\overline{HS}_0$, $\overline{VS}_0$, DE_0
H	running	odd	H	H	RGB_0, $\overline{HS}_0$, $\overline{VS}_0$, DE_0
H	running	even	H	L	RGB_n, $\overline{HS}_n$, $\overline{VS}_n$, DE_n
H	stopped	X or floating	X	L	undefined
L	X or floating	X or floating	X	L	undefined

[1] YYY_n = current valid pixel data is output to the parallel interface.

[2] YYY_0 = most recent valid pixel data is output to the parallel interface.

7.7 Frame Mixing and Advanced Frame Mixing

When PTN3700 is configured as Receiver (TX/$\overline{RX}$ = LOW), the CMOS input FM selects whether the Frame Mixing function is turned on (FM = HIGH) or off (FM = LOW). (When PTN3700 is configured as Transmitter (TX/$\overline{RX}$ = HIGH), the Frame Mixing function is not available, and the FM input should not be used.)

Advanced Frame Mixing is a proprietary pixel mapping algorithm that features the ability to render full 24-bit color resolution (provided 24-bit source data is input) using an 18-bit or an 18-bit plus display.

When Frame Mixing is off, the full 24-bit data path is maintained unaltered for the link (transparent).

When Frame Mixing is enabled, the algorithm maps the incoming 24-bit data to the 18-bit output data, aligned to the MSB. This is illustrated in Table 13. The new 18-bit data fields ($R[7:2]_{FM}$, $G[7:2]_{FM}$ and $B[7:2]_{FM}$) contain the altered information as calculated by the Frame Mixing algorithm from the original data. One additional 'Advanced Frame Mixing' bit is encoded into the next lower significant bit ($R1_{AFM}$, $G1_{AFM}$ and $B1_{AFM}$) of the output data.

Table 13. Advanced Frame Mixing bit mapping (FM = HIGH)

Bit	7	6	5	4	3	2	1	0
Input data	R7	R6	R5	R4	R3	R2	R1	R0
	G7	G6	G5	G4	G3	G2	G1	G0
	B7	B6	B5	B4	B3	B2	B1	B0
Output data	$R7_{FM}$	$R6_{FM}$	$R5_{FM}$	$R4_{FM}$	$R3_{FM}$	$R2_{FM}$	$R1_{AFM}$	HIGH
	$G7_{FM}$	$G6_{FM}$	$G5_{FM}$	$G4_{FM}$	$G3_{FM}$	$G2_{FM}$	$G1_{AFM}$	HIGH
	$B7_{FM}$	$B6_{FM}$	$B5_{FM}$	$B4_{FM}$	$B3_{FM}$	$B3_{FM}$	$B1_{AFM}$	HIGH

When using Frame Mixing with normal 18-bit displays, the 6 MSBs of the parallel video data outputs (R[7:2], G[7:2] and B[7:2]) should be connected to the display driver inputs. When using special '18-bit plus' display drivers (Advanced Frame Mixing capable), additionally the next lower significant bit (R1, G1 and B1) should be connected to the corresponding display driver input.

7.8 Auxiliary signals

The two auxiliary bits A[1:0] are user-supplied bits that can be additionally serialized and deserialized by the PTN3700 in transmitter and receiver modes, respectively. These auxiliary bits are transparent to the PTN3700 and can be used to transmit and receive miscellaneous status or mode information across the link to the display. Note that the auxiliary bits A[1:0] are excluded from the parity calculation and detection in the transmitter and receiver modes respectively. Even in the event of parity error being detected in the receiver mode, A[1:0] will still be deserialized as they are detected by the receiver.

8. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.3	+3.0	V
V_I	input voltage	receiver		−0.3	V_{DD} + 0.5	V
V_O	output voltage	driver		−0.3	V_{DD} + 0.5	V
T_{stg}	storage temperature			−65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	1500	V
		MM	[2]	-	200	V
		CDM	[3]	-	1000	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Machine Model: ANSI/EOS/ESD-S5.2.1-1999, standard for ESD sensitivity testing, Machine Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model: ANSI/EOS/ESD-S5.3.1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 15. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		1.65	1.8	1.95	V
V_I	input voltage		0	-	V_{DD}	V
I_{OH}	HIGH-level output current	0.8 × V_{DD}	-	-	−1	mA
I_{OL}	LOW-level output current	0.2 × V_{DD}	-	-	1	mA
T_{amb}	ambient temperature	operating in free air	−40	-	+85	°C

10. Static characteristics

Table 16. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		1.65	1.8	1.95	V
V_{IH}	HIGH-level input voltage	I_I = −10 μA	$0.7V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage	I_I = 10 μA	0	-	$0.3V_{DD}$	V
V_{OH}	HIGH-level output voltage	I_O = −1 mA	$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	I_O = 1 mA	0	-	$0.2V_{DD}$	V
C_i	input capacitance	TX mode	-	2	4	pF
Transmitter mode, PSS mode ($\overline{TX}$/RX = HIGH; FSS = LOW)						
I_{DD}	supply current	Shutdown mode; T_{amb} = −40 °C to +60 °C	-	4	10	μA
		Standby mode; T_{amb} = −40 °C to +60 °C	-	4	10	μA
		Active mode	[1]			
		PCLK = 6 MHz; Mode 00	-	11	12.6	mA
		PCLK = 12 MHz; Mode 00	-	15	17.3	mA
		PCLK = 20 MHz; Mode 00	-	21	23.5	mA
		PCLK = 8 MHz; Mode 01	-	13	14.8	mA
		PCLK = 22 MHz; Mode 01	-	19	21.2	mA
		PCLK = 40 MHz; Mode 01	-	26	29.3	mA
		PCLK = 20 MHz; Mode 10	-	19	21.1	mA
		PCLK = 40 MHz; Mode 10	-	26	28.8	mA
		PCLK = 65 MHz; Mode 10	-	35	36.8	mA
Transmitter mode, FSS mode ($\overline{TX}$/RX = HIGH; FSS = HIGH)						
I_{DD}	supply current	Shutdown mode; T_{amb} = −40 °C to +60 °C	-	4	10	μA
		Standby mode; T_{amb} = −40 °C to +60 °C	-	4	10	μA
		Active mode	[1]			
		PCLK = 6 MHz; Mode 00	-	12	13.7	mA
		PCLK = 12 MHz; Mode 00	-	17	19.2	mA
		PCLK = 20 MHz; Mode 00	-	24	26.6	mA
		PCLK = 8 MHz; Mode 01	-	13	14.9	mA
		PCLK = 22 MHz; Mode 01	-	20	22.3	mA
		PCLK = 40 MHz; Mode 01	-	28	31.9	mA
		PCLK = 20 MHz; Mode 10	-	19	21.2	mA
		PCLK = 40 MHz; Mode 10	-	26	29.1	mA
		PCLK = 65 MHz; Mode 10	-	35	38.9	mA

Table 16. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver mode, PSS mode (TX/$\overline{RX}$ = LOW; FSS = LOW)[2]						
I_{DD}	supply current	Shutdown mode; T_{amb} = −40 °C to +60 °C	-	4	10	μA
		Standby mode; T_{amb} = −40 °C to +60 °C	-	4	10	μA
		Active mode [1]				
		PCLK = 6 MHz; Mode 00	-	8	10.7	mA
		PCLK = 12 MHz; Mode 00	-	14	16.5	mA
		PCLK = 20 MHz; Mode 00	-	22	25	mA
		PCLK = 8 MHz; Mode 01	-	8.5	11	mA
		PCLK = 22 MHz; Mode 01	-	16	19.5	mA
		PCLK = 40 MHz; Mode 01	-	25	31	mA
		PCLK = 20 MHz; Mode 10	-	14	17.8	mA
		PCLK = 40 MHz; Mode 10	-	22.5	28	mA
		PCLK = 65 MHz; Mode 10	-	34	40	mA
Receiver mode, FSS mode (TX/$\overline{RX}$ = LOW; FSS = HIGH)[2]						
I_{DD}	supply current	Shutdown mode; T_{amb} = −40 °C to +60 °C	-	4	10	μA
		Standby mode; T_{amb} = −40 °C to +60 °C	-	4	10	μA
		Active mode [1]				
		PCLK = 6 MHz; Mode 00	-	7.5	10.2	mA
		PCLK = 12 MHz; Mode 00	-	13	15.5	mA
		PCLK = 20 MHz; Mode 00	-	20.6	23.6	mA
		PCLK = 8 MHz; Mode 01	-	8.1	10.6	mA
		PCLK = 22 MHz; Mode 01	-	15.4	18.6	mA
		PCLK = 40 MHz; Mode 01	-	23.4	29.3	mA
		PCLK = 20 MHz; Mode 10	-	13.5	17.3	mA
		PCLK = 40 MHz; Mode 10	-	21.8	26.9	mA
		PCLK = 65 MHz; Mode 10	-	33	38	mA

[1] Worst-case data pattern for power dissipation is used: alternating vertical stripes. The colors of the stripes correspond to the data pattern: RGB[23:0] = 0xAA AAAA (odd stripes) / RGB[23:0] = 0x55 5555 (even stripes).

[2] Based on receiver output load (per output) of 16 pF. The loaded outputs are: PCLK, R[7:0], G[7:0], B[7:0], $\overline{HS}$, $\overline{VS}$ and DE.

11. Dynamic characteristics

11.1 Transmitter mode

Table 17. Dynamic characteristics for Transmitter mode

V_{DD} = 1.65 V to 1.95 V, T_{amb} = −40 °C to +85 °C, unless otherwise specified.
All CMOS input signals' rise time and fall time to Transmitter are stipulated to be from 1 ns to 15 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{i(PCLK)}$	input frequency on pin PCLK	Mode 00; see Table 5	4.0	-	21.6	MHz
		Mode 01; see Table 5	8.0	-	43.3	MHz
		Mode 10; see Table 5	20.0	-	65.0	MHz
$\delta_{i(PCLK)}$	input duty cycle on pin PCLK		33	-	67	% T_{PCLK}
$t_{su(D-PCLK)}$	set-up time from data input to PCLK		2.0	-	-	ns
$t_{h(D-PCLK)}$	hold time from data input to PCLK		2.0	-	-	ns
$t_{jit(cc)}$	cycle-to-cycle jitter time	PCLK	−300	-	+300	ps
$B_{PLL(loop)}$	PLL loop bandwidth	−3 dB corner frequency of PLL loop filter response	0.02 × $f_{i(PCLK)}$	0.03 × $f_{i(PCLK)}$	0.05 × $f_{i(PCLK)}$	MHz

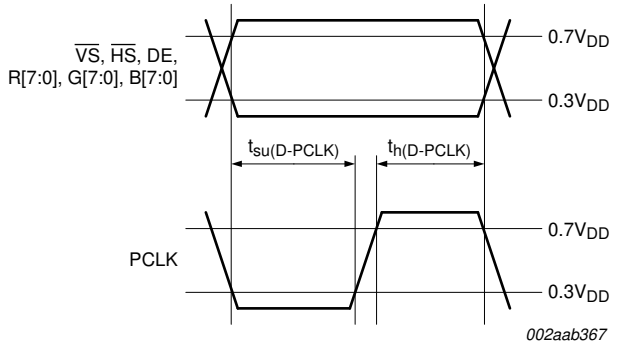


Fig 19. AC timing diagram - Transmitter mode

11.2 Receiver mode

Table 18. Dynamic characteristics for Receiver mode

V_{DD} = 1.65 V to 1.95 V, T_{amb} = −40 °C to +85 °C, unless otherwise specified.
CMOS output load C_L = 16 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(PCLK)}$	output frequency on pin PCLK	Mode 00; see Table 5	4.0	-	21.6	MHz
		Mode 01; see Table 5	8.0	-	43.3	MHz
		Mode 10; see Table 5	20.0	-	65.0	MHz
$\delta_{o(PCLK)}$	output duty cycle on pin PCLK	Mode 00 or Mode 10; F/$\overline{XS}$ = 1	45	50	55	% T_{PCLK}
		Mode 01; F/$\overline{XS}$ = 1	48	53	59	% T_{PCLK}
$t_{sk(Q)}$	data output skew time	Mode 00; F/$\overline{XS}$ = 1	−0.5	0	1.5	ns
		Mode 01; F/$\overline{XS}$ = 1	−0.5	0	0.8	ns
		Mode 10; F/$\overline{XS}$ = 1	−0.5	0	0.8	ns
		Mode 00; F/$\overline{XS}$ = 0	−3.0	0	2.0	ns
		Mode 01; F/$\overline{XS}$ = 0	−0.5	0	2.5	ns
		Mode 10; F/$\overline{XS}$ = 0	−1.4	0	3.0	ns
$t_{jit(r)PCLK}$	PCLK rise jitter time		−0.6	0	0.6	ns
t_r	rise time	CMOS signals				
		Mode 00; F/$\overline{XS}$ = 0	8	-	18	ns
		Mode 00; F/$\overline{XS}$ = 1	4	-	10	ns
		Mode 01; F/$\overline{XS}$ = 0	4	-	10	ns
		Mode 01; F/$\overline{XS}$ = 1	1	-	3	ns
		Mode 10; F/$\overline{XS}$ = 0	4	-	10	ns
		Mode 10; F/$\overline{XS}$ = 1	1	-	3	ns
t_f	fall time	CMOS signals				
		Mode 00; F/$\overline{XS}$ = 0	8	-	18	ns
		Mode 00; F/$\overline{XS}$ = 1	4	-	10	ns
		Mode 01; F/$\overline{XS}$ = 0	4	-	10	ns
		Mode 01; F/$\overline{XS}$ = 1	1	-	3	ns
		Mode 10; F/$\overline{XS}$ = 0	4	-	10	ns
		Mode 10; F/$\overline{XS}$ = 1	1	-	3	ns
$B_{PLL(loop)}$	PLL loop bandwidth	−3 dB corner frequency of PLL loop filter response	0.09 × $f_{o(PCLK)}$	0.11 × $f_{o(PCLK)}$	0.14 × $f_{o(PCLK)}$	MHz

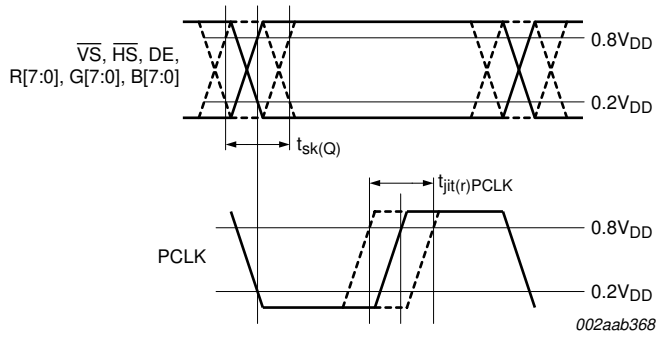


Fig 20. AC timing diagram - Receiver mode