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# PTN5100D

## USB Type-C power delivery PHY and protocol IC

Rev. 1 — 2 August 2016

Product data sheet

## 1. General description

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PTN5100D is a single port USB Type-C Power Delivery (PD) PHY and Protocol IC that provides Type-C Configuration channel interface and USB PD Physical and Protocol layer functions to a System PD Port Policy Controller (Policy Engine and Device Policy Manager, Alternate mode controller). It complies with USB PD[1] and Type-C[2] specifications. PTN5100D is architected to deliver robust performance, compliant behavior, configurability and system implementation flexibility that are essential to tide over interoperability and compliance hurdles in the platform applications.

PTN5100D can support system realization of the following PD roles: (i) Consumer only (ii) Consumer/Provider. Further, it is register programmed to operate in Type-C specific Upstream Facing Port (UFP). It can work along with the PD policy controller to operate in other modes (DFP, DRP).

PTN5100D operates from platform power supply VDD, or it can also be powered from USB power VBUS directly. The host interface operates on VIO supply to facilitate interfacing to systems that use IO supply rail different from VDD supply rail.

It provides SPI/I2C interface for system host control/status update. The interface choice is pre-configured in NXP factory.

PTN5100D is available in a small footprint package option: HVQFN20 4 mm x 4 mm, 0.5 mm pitch.

## 2. Features and benefits

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### 2.1 USB PD and Type-C Features

Complies with USB PD[1] and USB Type-C[2] specifications.

- Supports implementation of various system PD roles: Consumer, Consumer/Provider
- Supports Type-C role configurability
  - ◆ Type-C role (UFP, DFP)
  - ◆ Implements UFP role pull down behavior to handle dead battery condition on battery powered platforms
  - ◆ Implements 'Rd' indication on CC pin
- Cooperatively works under the control of Policy controller MCU for power delivery negotiation and contract(s), Alternate mode and VDM exchanges
  - ◆ Implements BMC (de)coding, 4B5B symbol (de)coding, CRC generation/checking, PD packet assembling/disassembling including Preamble, SOP, EOP, Good CRC response, Retries, Hard and Cable resets
  - ◆ PD PHY and Protocol layer interface control and status update handled via SPI/I2C interface



- DRP and DFP roles can be supported

## 2.2 System protection features

- Back current protection on all pins when PTN5100D is unpowered
- CC1 and CC2 pins are 5.5 V tolerant
- VBUS pin and VBUS power path MOSFET enable pins are 28 V tolerant

## 2.3 General

- Delivers (active LOW enable) gate control signals for PMOS Power MOSFETs on VBUS source and sink power paths
- Provides dedicated IO pin (CC\_ORIENT) for indicating Cable/plug orientation
- Delivers up to 30 mA (max) for powering Policy controller MCU
- Supports SPI slave interface (SPI modes 1 and 2 supported) up to 30 MHz
- Supports I2C slave interface standard mode (100 kHz), Fast mode (400 kHz) and Fast mode plus (1 MHz)
- I2C Device slave address programmable up to 3 values
- Supports 3.3 V or 1.8 V capable I<sup>2</sup>C-bus or SPI interface
  - ◆ Supports register access - device configuration, control and status/interrupt interfacing through Slave I<sup>2</sup>C-bus interface
- Power supplies - VDD (3.3 V ±10 %) or VBUS
  - ◆ Tolerant up to 28 V on VBUS and operational up to maximum of 25 V on VBUS
- Operating temperature –20 °C to 85 °C
- ESD 8 kV HBM, 1 kV CDM
- Package: HVQFN20 4 mm × 4 mm, 0.5 mm pitch.

## 3. Applications

- PC accessories/peripherals: Docking, Mobile Monitors, Multi-Function Monitors, Portable/External hard drives, Dongles and accessories, etc.

## 4. Ordering information

Table 1. Ordering information

| Type number | Topside marking | Package |   |          |
|-------------|-----------------|---------|---|----------|
|             |                 | Name    | Description   | Version  |
| PTN5100DBS  | 51D0            | HVQFN20 | plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 4 × 4 × 0.85 mm <sup>[2]</sup> | SOT917-4 |
| PTN5100DABS | 51DA            | HVQFN20 | plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 4 × 4 × 0.85 mm <sup>[3]</sup> | SOT917-4 |

[1] Total height after printed-circuit board mounting ≤1 mm (maximum)

[2] Supported system interface - SPI

[3] Supported system interface - I<sup>2</sup>C

4.1 Ordering options

Table 2. Ordering options

| Type number | Orderable part number | Package | Packing method                                   | Minimum order quantity | Temperature                         |
|-------------|-----------------------|---------|--|------------------------|-------------------------------------|
| PTN5100DBS  | PTN5100DBSMP          | HVQFN20 | Reel 13" Q2/T3<br>*standard mark SMD<br>dry pack | 6000                   | T <sub>amb</sub> = -20 °C to +85 °C |
| PTN5100DABS | PTN5100DABSMP         | HVQFN20 | Reel 13" Q2/T3<br>*standard mark SMD<br>dry pack | 6000                   | T <sub>amb</sub> = -20 °C to +85 °C |

5. Block diagram

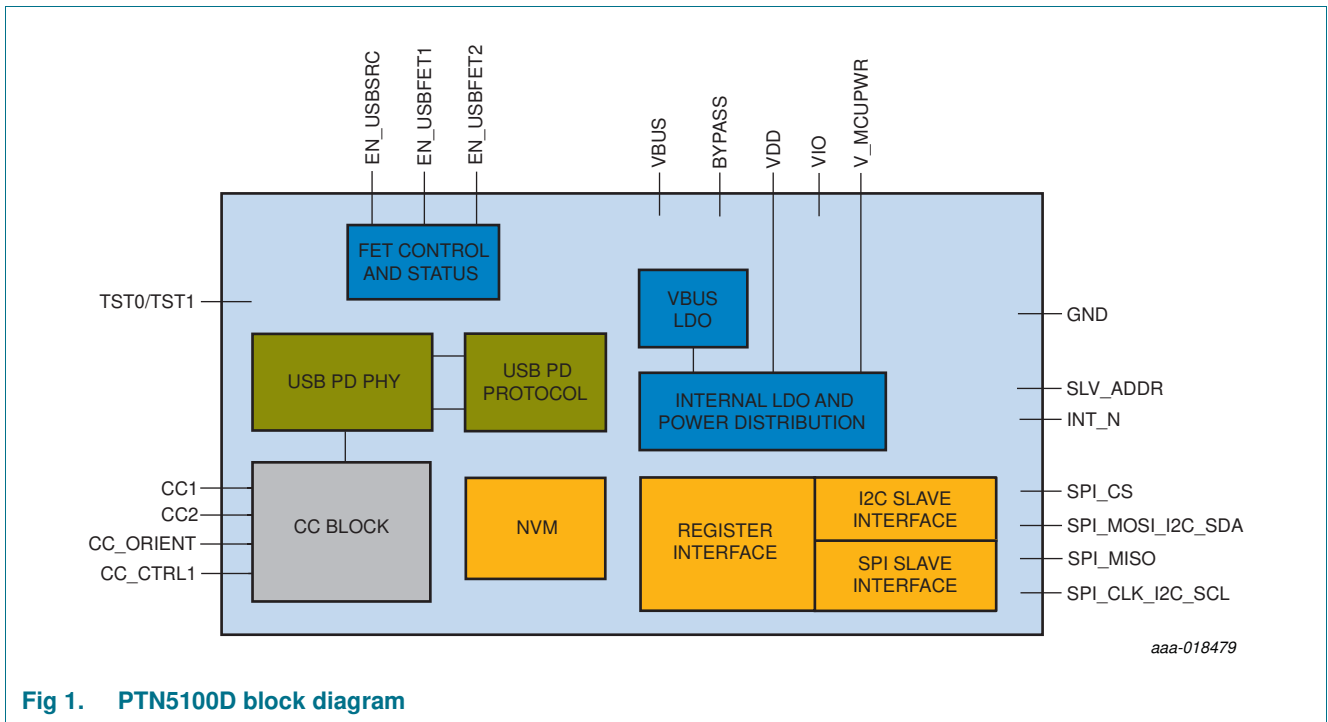


Fig 1. PTN5100D block diagram

## 6. Pinning information

### 6.1 Pinning

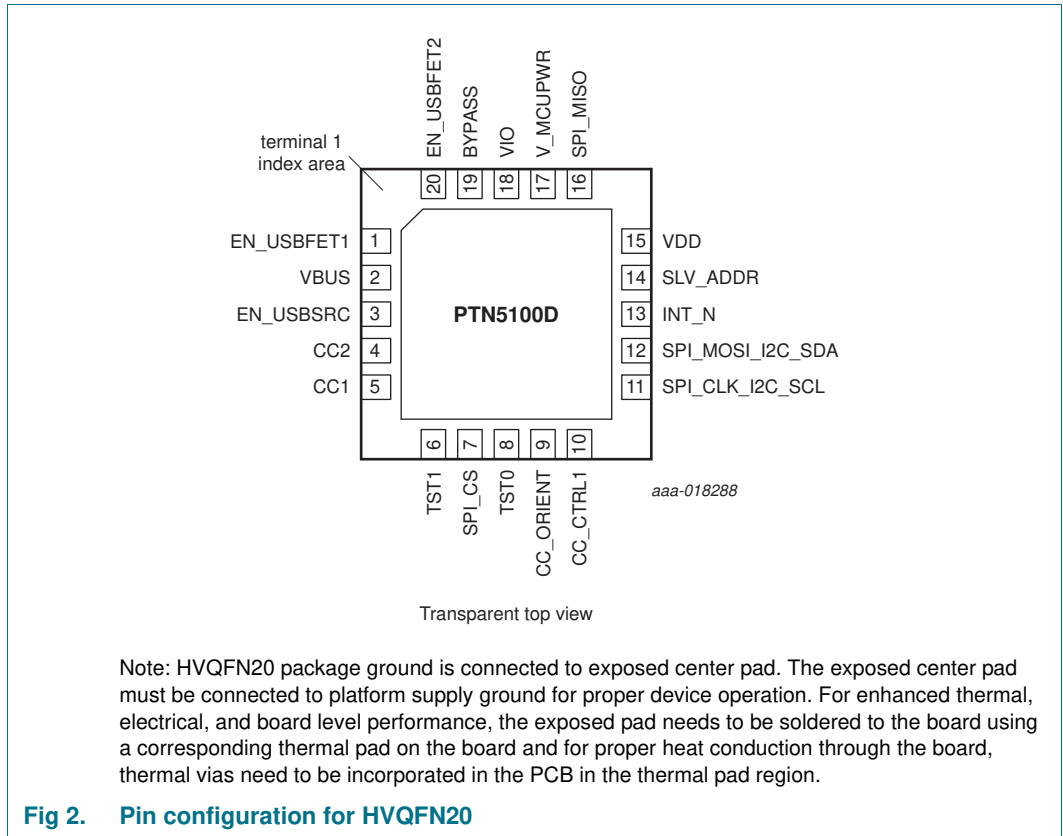


Fig 2. Pin configuration for HVQFN20

## 6.2 Pin description

Table 3. Pin description

| Symbol     | Pin | Pin direction | Pin Type                  | Description  |
|------------|-----|---------------|---------------------------|--|
| EN_USBSRC  | 3   | Output        | Open drain                | <p>USB PD VBUS Source Power path PMOS FET gate Active Low enable.</p> <p>At default/POR, this pin is Hi-Z; PTN5100D drives this pin LOW based on Type-C connection state and/or policy controller MCU command.</p> <p>The pin status can be read in the internal register(s).</p>  |
| EN_USBFET1 | 1   | Output        | Open drain                | <p>USB PD VBUS Source or Sink Power path PMOS FET gate Active Low enable.</p> <p>At default/POR, this pin is Hi-Z; PTN5100D drives this pin LOW based on Type-C connection state and/or policy controller MCU command.</p> <p>The pin status can be read in the internal register(s).</p>  |
| EN_USBFET2 | 20  | Output        | Open drain                | <p>USB PD VBUS Source or Sink Power path PMOS FET gate Active Low enable.</p> <p>At default/POR, this pin is Hi-Z; PTN5100D drives this pin LOW based on policy controller MCU command.</p> <p>The pin status can be read in the internal register(s).</p>   |
| CC1        | 5   | IO            | Custom IO                 | <p>Type-C Configuration channel #1</p> <p>TVS or similar protection diode (e.g. PESD5V0S1USF, PESD5V0S1UL, etc.) shall be used to protect the CC1/2 pins from overshoot/undershoot during cable plug/unplug and cable discharge events.</p>  |
| CC2        | 4   | IO            | Custom IO                 | <p>Type-C Configuration channel #2</p> <p>TVS or similar protection diode (e.g. PESD5V0S1USF, PESD5V0S1UL, etc.) shall be used to protect the CC1/2 pins from overshoot/undershoot during cable plug/unplug and cable discharge events.</p>  |
| CC_ORIENT  | 9   | Output        | CMOS IO on VIO power rail | <p>This pin indicates Type-C cable plug orientation.</p> <p>The pin's polarity is inverted at power-on reset and the PD policy controller MCU has to initialize PTN5100D before the pin level is valid. After the initialization, the pin indicates orientation as follows:</p> <p>LOW = Normal plug orientation (CC communication on CC1)</p> <p>HIGH = Reverse plug orientation (CC communication on CC2)</p> <p>Default pin value is LOW even if there is no connection or normal plug connection</p> |
| CC_CTRL1   | 10  | Input         | Analog Input              | <p>Input to indicate whether to present 'Rd' or Open on CC pin under Unpowered condition</p>   |
| TST1       | 6   | Output        | CMOS IO on VIO power rail | <p>Meant for Test purpose only. Do not connect in the application</p>  |

Table 3. Pin description ...continued

| Symbol               | Pin        | Pin direction | Pin Type   | Description   |
|----------------------|------------|---------------|--|---|
| TST0                 | 8          | Input         | Power  | Pin for Test purpose. This pin shall be connected to GND in customer applications.  |
| SPI_MOSI_<br>I2C_SDA | 12         | IO            | Open drain IO (I2C mode) referenced to VIO voltage<br>V_MCUPWR power rail (SPI mode) | Dual purpose pin. In I2C slave mode, this serves as I2C data input/output (open drain)<br>In SPI slave mode, this pin serves Master Output Slave Input function (push pull CMOS IO) |
| SPI_MISO             | 16         | Output        | V_MCUPWR rail  | This serves Master Input Slave Output function of SPI interface   |
| SPI_CLK_I2C_SCL      | 11         | Input         | Open drain IO (I2C mode) referenced to VIO voltage<br>V_MCUPWR power rail (SPI mode) | Dual purpose pin. In I2C slave mode, this serves as I2C clock input (open drain).<br>In SPI slave mode, it serves as SPI clock input pin  |
| SPI_CS               | 7          | Input         | V_MCUPWR rail  | This pin provides SPI chip select Input   |
| INT_N                | 13         | Output        | Open drain   | Level triggered interrupt. Open drain output; This pin needs to be externally pulled up VIO.<br>This pin is usable only when VDD is valid   |
| SLV_ADDR             | 14         | Ternary input | V_MCUPWR rail  | Ternary slave address (I2C) pin   |
| V_MCUPWR             | 17         | Output        | Power  | This pin delivers current up to 30 mA (max) to policy controller MCU. External supply de-coupling capacitor(s) (2.2 $\mu$ F $\pm$ 10 % ceramic capacitor) are required              |
| VIO                  | 18         | Input         | Power  | IO domain power supply. External supply de-coupling capacitor(s) are required   |
| VBUS                 | 2          | Input         | Power  | VBUS power supply. External supply de-coupling capacitor(s) are required  |
| VDD                  | 15         | Input         | Power  | Core domain power supply. External supply de-coupling capacitor(s) are required   |
| BYPASS               | 19         | Internal      | Internal power rail  | Internal power rail. A ceramic capacitor (2.2 $\mu$ F $\pm$ 10 %) is to be connected to this pin  |
| GND                  | Center pad |               | GND  | Ground Center pad   |

## 7. Functional description

PTN5100D is a 1-port USB Type-C PD Physical and Protocol Layer IC that can be used to realize single or multi-port USB Type-C PD and/or Alternate mode implementations. It complies with USB PD [1] and Type-C specifications [2]. PTN5100D is required to be initialized after power-on by the PD policy controller MCU before the dedicated pin CC\_ORIENT behaves as specified in this data sheet specification.

PTN5100D can be partitioned into the following major functional blocks along with their respective interfaces:

- Type-C Configuration Channel functional block
- USB Power Delivery function
- Power FET Enable Control
- MCU interface and Control

The following subsections describe the PTN5100D with its major functional blocks.

### 7.1 Type-C Configuration Channel functional block

Type-C Configuration Channel (CC) function operates as a front end to cable/plug interface. This block implements Orientation detection, Cable/Plug insertion and removal detection as per [2].

PTN5100D can operate under MCU control. To support use cases, PTN5100D implements HW circuitry to perform the following operations:

- Applying 'Rp' or 'Rd' depending on the (NVM) configured role
- Detecting cable/plug connect and disconnect events
- Indicating Type-C current limit level in a system under DFP role
- Detecting the current level supported by remote end under UFP role
- Identifying plug orientation and indicating through CC\_ORIENT<sup>1</sup> pin
- Updating event, interrupt and status registers and raising interrupt signal using INT\_N pin

In order to provide reliable connect/disconnect event triggers, debouncing is also implemented as per [2].

PTN5100D allows for register programmability to enable usage under different platform configurations.

### 7.2 USB Power Delivery Function

In general, the Embedded Controller (EC) or System Management Controller (SMC) handles the overall Application/Platform power management given the system states, battery status, etc. It reviews capabilities and status of various power providers (USB PD,

1. The CC\_ORIENT pin's polarity is inverted at power-on and the PD policy controller MCU has to initialize PTN5100D before the pin level is valid



AC-DC adapter, battery, docking, etc.) dynamically and determines a specific source for powering/charging the platform - the power source selection is an important and platform dependent aspect of Application power delivery scheme.

- For example, in some applications, platform host processor plays a central role in controlling the various power sources including USB PD. To support this, PTN5100D and Policy controller MCU can be configured to negotiate and agree on power contract based on command/response exchanges with host processor
- In several applications, host processor may not even exist or it wants to play a hands-off role. To support these applications, PTN5100D and Policy controller MCU can be configured to operate autonomously

In a Type-C PD implementation, the system partitioning involves the following parts:

- Port PHY and Protocol layer functions → PTN5100D
- Port policy engine and device policy management, Alternate mode support → Discrete policy controller MCU
- System management → host processor

PTN5100D implements USB PD PHY layer and HW intensive Protocol functions and it works along with a discrete MCU to implement Full PD functionality. The combined 2-chip system solution (PTN5100D and MCU) can be configured to support one or more of the following PD roles:

1. PD Consumer
2. PD Consumer/Provider

The interface between PTN5100D and Policy controller MCU can be either SPI or I2C. PTN5100D provides a transparent set of commands and register interface for the MCU to control the operation and ensure safe/suitable system behavior/response. PTN5100D Application Programming guide [3] describes the register set supported for the PD control, status updates and operational control/sequences.

The policy controller MCU implements PD port policy layer as per [1]. The default PD power profiles are configured in the MCU and the host processor could request for specific profile and PD contract based on platform application. The 2-chip solution can operate autonomously or under host processor control.

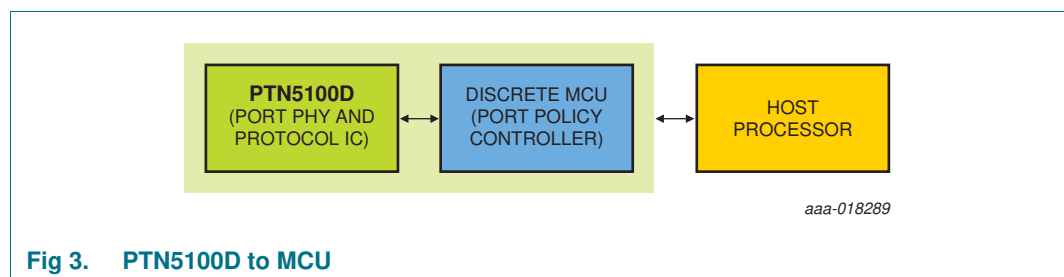
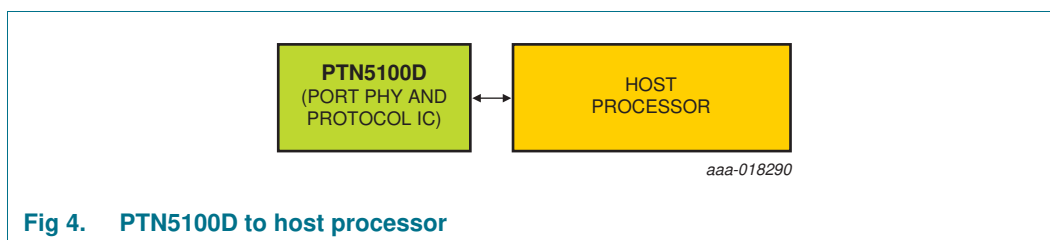


Fig 3. PTN5100D to MCU



PTN5100D implements USB PD PHY layer function as follows:

- Slew rate controlled IO
- Bit transmission and data recovery
- Bi-phase Mark Coding
- 4B5B Line coding
- CRC computation and checking

It handles the following Protocol layer functions:

- Data Packetization and Extraction
- Good CRC Response
- Automated Retries
- Hard reset, Cable reset
- Tx and Rx buffer management

It handles both Transmit and Receive operation and it maintains dedicated TX and RX data buffers. To minimize chances of collision, PTN5100D checks the CC line before start of transmission. Once the data is transmitted or received, the I2C interface status is updated and MCU is interrupted.

BIST mode (Tx, Rx) is also supported.

Note: NXP is open to engage on Firmware licensing to give a head start to customers on USB PD Policy and Alternate mode Firmware front. Please contact NXP for further details.

### 7.3 Power FET control

PTN5100D implements three dedicated open drain IOs that can be used to control the external power MOSFETs and enable/ disable VBUS source and sink power paths of the system. These are enabled or disabled based on PD power role (provider or consumer) of the Type-C interface. Based on PD negotiation and contract, the policy controller MCU enables/disables the specific power path (source FET or sink FETs).

- EN\_USBSRC: This pin is used to enable/disable the power MOSFETs that corresponds to VBUS source (e.g. 5V regulated output). The FET enable can be configured and controlled through the register interface by the MCU. The pin status is monitored and updated in a status register.
- EN\_USBFET1: This pin is used to enable/disable the power MOSFETs that corresponds to USB PD power from external power sources or delivering VBUS power to external peripherals. Its specific use as a VBUS source or sink path control

is programmable. The FET enable can be configured and controlled through the register interface by the MCU. The pin status is monitored and updated in a status register.

- EN\_USBFET2: This pin is used to enable/disable the power MOSFETs that corresponds to USB PD power from external power sources or delivering VBUS power to external peripherals. Its specific use as a VBUS source or sink path control is programmable. The FET enable can be configured and controlled through the register interface by the MCU. The pin status is monitored and updated in a status register.

### 7.4 MCU interface and control

PTN5100D works along with policy controller MCU to realize USB PD functionality and/or Alternate mode support. The MCU can control and interface with PTN5100D through a dedicated I2C/SPI interface. In a given system implementation, only one of the two interfaces (I2C, SPI) can be used.

PTN5100D provides up to three I2C slave address combinations based on ternary pin (SLV\_ADDR) setting as per the table below.

**Table 4. I2C slave address combinations**

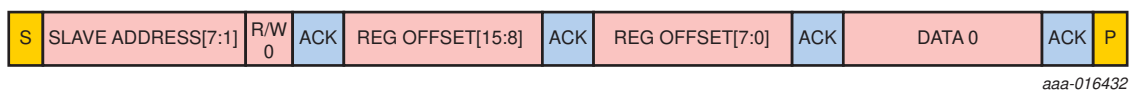
| SLV_ADDR pin | Device address (Write/read) |
|--------------|-----------------------------|
| GND          | 0xE0/0xE1                   |
| VDDIO        | 0xE4/0xE5                   |
| Unconnected  | 0xE8/0xE9                   |

#### 7.4.1 I<sup>2</sup>C-bus interface

PTN5100D has a slave I2C interface through which it provides a mechanism for control and status interaction/communication with the MCU. It supports Standard mode, Fast mode and Fast mode plus.

##### 7.4.1.1 I2C writes

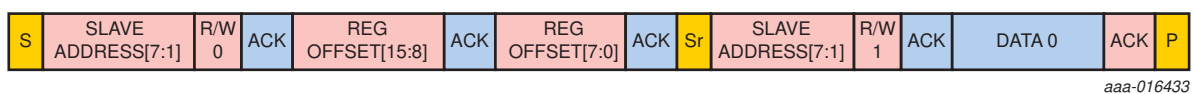
The following figure shows the basic protocol for I2C writes. A 16-bit offset is used to address each register.



**Fig 5. I2C writes**

##### 7.4.1.2 I2C reads

The following figure shows the basic protocol for I2C reads. They start off like I2C writes by specifying a 16-bit register offset. This is followed by a repeat start condition, the Slave Address (Read), and the read data.



**Fig 6. I2C reads**

### 7.4.1.3 I2C address auto-incrementing

Bursts are allowed during writes and reads. Bit 15 of the register offset is the auto-increment indication. If '0' then the internally generated MMIO address will not increment with each data byte. If '1', then the address will increment with each data byte.

A detailed description of the I<sup>2</sup>C-bus specification, with applications, is given in user manual UM10204, "I<sup>2</sup>C-bus specification and user manual" [4]. Referring to I2C protocol, PTN5100D positively acknowledges all 256 register offset addresses, though there are certain undefined address offsets.

### 7.4.2 SPI interface

PTN5100D provides an SPI slave interface as well. It supports SPI modes 1 and 2. This interface exposes same register interface as that of I2C. Its main advantage is faster command and data transport and relaxes MCU response time/latency requirements.

### 7.4.3 Register interface

PTN5100D Application programming guide [3] describes the various registers with their bit definitions, POR values and the various functions. Also, sample 'C' programs corresponding to various functions and operations are given. This guide can be used by the platform system architects to implement the EC firmware to control the operations with PTN5100D. Refer to programming guide for more information. The register definitions are also described in the guide.

### 7.4.4 Relevant Interface pins - SLV\_ADDR, SPI\_CLK\_I2C\_SCL, SPI\_MOSI\_I2C\_SDA, SPI\_CS, SPI\_MISO, INT\_N

- SLV\_ADDR is a ternary input pin that is used to support up to 3 slave PTN5100D devices on a given platform. This pin can be pulled to V\_MCUPWR rail, left open or pulled to GND.
- While in SPI mode, SPI\_CLK\_I2C\_SCL, SPI\_MISO, SPI\_MOSI\_I2C\_SDA and SPI\_CS provide the necessary interface for connecting to SPI master controller on the MCU.
- While in I2C mode, SPI\_CLK\_I2C\_SCL and SPI\_MOSI\_I2C\_SDA are used for I2C clock and data interfacing to MCU
- INT\_N pin is used to raise Active LOW level triggered interrupt signal to EC. PTN5100D processes various events and raises interrupt that require SMC intervention. Once all relevant events are processed by the MCU, the INT\_N pin goes HIGH. At POR, this pin remains HIGH (when VIO is valid). The specific events that can generate the interrupt can be selected.

## 7.5 Power supplies

PTN5100D is designed to operate under various power supplies. It can operate under both normal battery and dead battery environments (while drawing power from VBUS). PTN5100D handles power supply transitions (VBUS, VDD) transparently and there is no specific power supply ramp requirement imposed on the system (between VDD and VIO rails) also.

The following table highlights the power supplies and operating conditions for PTN5100D.

Table 5. Power supplies vs. operating conditions

| Valid power supply input combination | Operational condition   | Remarks   |
|--------------------------------------|---|---|
| VDD, VIO                             | Normal powered condition (both battery based or non-battery based platforms)  | All interfaces operational                                |
| VDD, VIO, VBUS                       | Normal powered condition; Host Platform may be powered/charged through VBUS simultaneously  | All interfaces operational                                |
| VBUS, VIO(=V_MCUPWR)                 | Dead battery in battery based platforms or Normal powered condition under other platforms; Host Platform powered/charged through USB PD | All interfaces operational                                |
| VBUS                                 | Dead battery operation; PTN5100D draws power from VBUS for its operation; Host Platform may be powered/charged through USB PD later     | PTN5100D pins (dependent on VIO rail) are not operational |

**Remark:** The Policy controller MCU is powered by PTN5100D.

The relevant pins associated with this functional block are:

- VDD
- VIO
- VBUS
- V\_MCUPWR
- BYPASS

## 8. PTN5100D - Use case view

Given that USB Power Delivery could address the requirements of a wide set of markets and product segments, PTN5100D is designed to work over a range of product categories, platform applications, use cases and usage roles. With its configurability, it can serve the needs of both general and custom applications. Not limited to these but the following subsection illustrates a use case for PTN5100D.

8.1 System use case illustration

8.1.1 Type-C cable adapter with PTN5100D

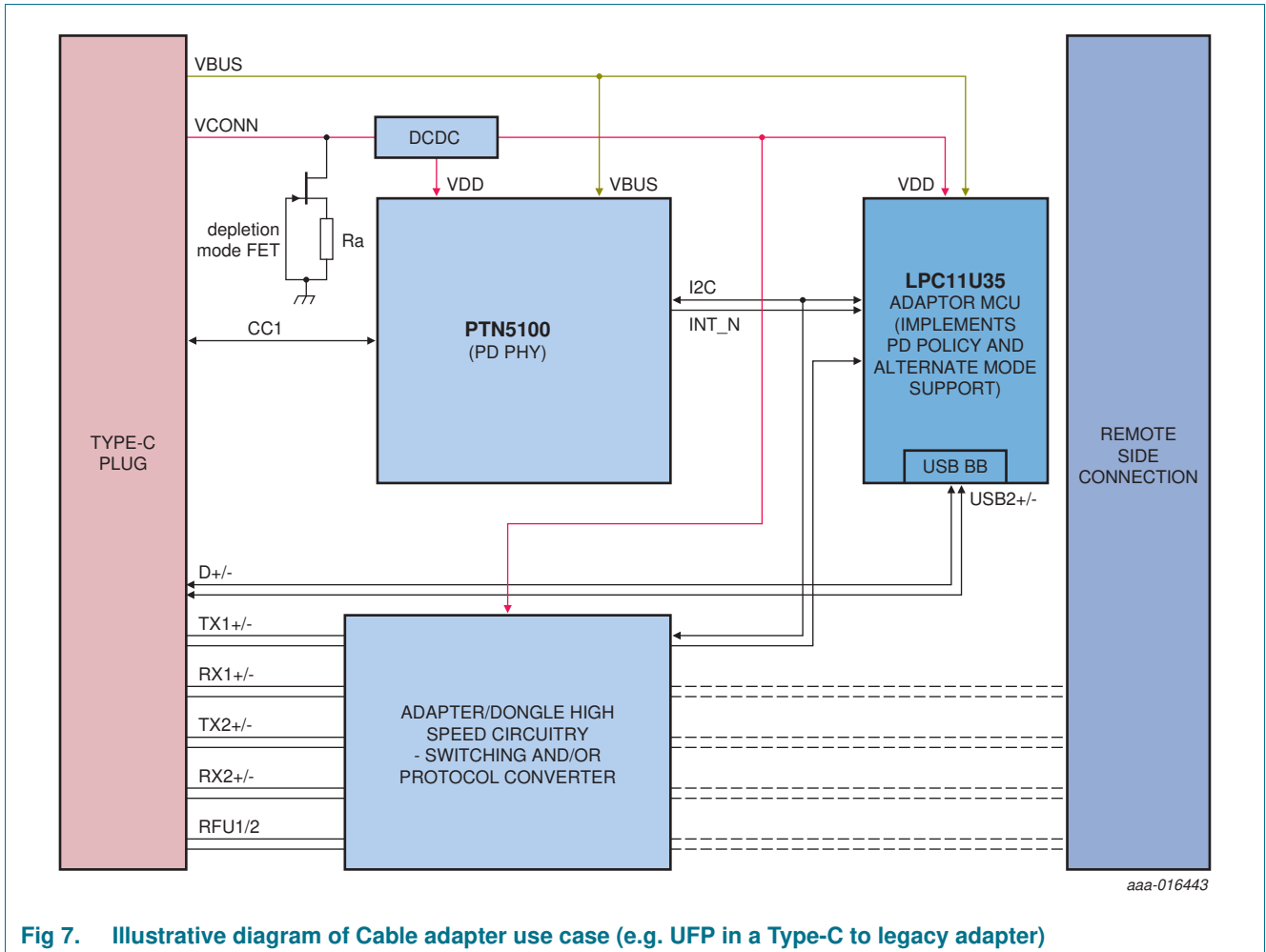


Fig 7. Illustrative diagram of Cable adapter use case (e.g. UFP in a Type-C to legacy adapter)

8.1.1.1 Application description

In this illustration, PTN5100D is inside Type-C cable adapter operating in UFP role. Some example use cases are Type-C to DP adapter, Type-C to VGA adapter, Type-C to Thunderbolt adapter etc. PTN5100D serves as PD PHY layer device for a Cable adapter management MCU or dedicated PD MCU wherein PD policy management, Alternate mode and VDM support are handled. The USB Billboard device is implemented as part of adapter management MCU.

The cable adapter implementation operates on VCONN and/or VBUS supply. Discrete depletion mode FET has to be used in the application for 'Ra' indication.

TVS protection diode (e.g. PESD5V0S1USF, PESD5V0S1UL, etc.) shall be used to protect the CC1/2 pins from overshoot/undershoot during cable plug/unplug and cable discharge events.

## 9. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol           | Parameter                       | Conditions  | Min  | Max  | Unit |
|------------------|---------------------------------|---|------|------|------|
| V <sub>DD</sub>  | supply voltage                  |   | -0.5 | +4.6 | V    |
| V <sub>IO</sub>  | IO voltage                      |   | -0.5 | +4.6 | V    |
| V <sub>BUS</sub> | USB VBUS voltage                |   | -0.5 | +28  | V    |
| V <sub>I</sub>   | Input voltage                   | voltage at the pin  |      |      |      |
|                  |                                 | CC_CTRL1, CC_ORIENT   | -0.5 | +4.6 | V    |
|                  |                                 | CC1, CC2  | -0.5 | +6.0 | V    |
|                  |                                 | EN_USBSRC, EN_USBFET1, EN_USBFET2   | -0.5 | +28  | V    |
|                  |                                 | BYPASS  | -0.5 | +2.5 | V    |
|                  |                                 | INT_N   | -0.5 | +4.6 | V    |
|                  |                                 | SLV_ADDR  | -0.5 | +4.6 | V    |
|                  |                                 | SPI_CLK_I2C_SCL, SPI_MOSI_SDA, SPI_MISO, SPI_CS   | -0.5 | +4.6 | V    |
| T <sub>stg</sub> | Storage temperature             |   | -65  | +150 | °C   |
| V <sub>ESD</sub> | electrostatic discharge voltage | HBM: VBUS, CC1, CC2 <a href="#">[1][2]</a>  | 8000 | -    | V    |
|                  |                                 | HBM for internal pins: <a href="#">[2]</a><br>CC_CTRL1, CC_ORIENT, BYPASS, VDD, VIO, INT_N, SLV_ADDR, SPI, EN_USBFET1, EN_USBFET2 and EN_USBSRC signals | 1500 | -    | V    |
|                  |                                 | CDM <a href="#">[3]</a>   | 1000 | -    | V    |

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[3] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

## 10. Recommended operating conditions

Table 7. Operating conditions

| Symbol           | Parameter                     | Conditions                              | Min  | Typ | Max | Unit |
|------------------|-------------------------------|---|------|-----|-----|------|
| VDD              | System supply voltage         |   | 3.0  | -   | 3.6 | V    |
| VIO              | System IO supply voltage      | when 3.3 V supply is used               | 3.0  | -   | 3.6 | V    |
|                  |                               | when 1.8 V supply is used               | 1.7  | -   | 1.9 | V    |
| VBUS             | USB VBUS voltage              |   | 3.7  | -   | 25  | V    |
| V <sub>I</sub>   | input voltage on the pin      |   |      | -   |     |      |
|                  |                               | CC_CTRL1, CC_ORIENT                     | -0.3 | -   | 3.6 | V    |
|                  |                               | CC1, CC2                                | -0.3 | -   | 5.5 | V    |
|                  |                               | EN_USBSRC,<br>EN_USBFET1,<br>EN_USBFET2 | -0.3 | -   | 25  | V    |
|                  |                               | INT_N                                   | -0.3 | -   | 3.6 | V    |
|                  |                               | SLV_ADDR                                | -0.3 | -   | 3.6 | V    |
| T <sub>amb</sub> | Ambient Operating temperature |   | -20  | -   | +85 | °C   |



## 11. Characteristics

### 11.1 Device characteristics

**Table 8. Device characteristics**

Applicable across operating temperature and power supply ranges as per [Section 10](#) (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

| Symbol          | Parameter  | Conditions  | Min | Typ | Max | Unit    |
|-----------------|--|---|-----|-----|-----|---------|
| $T_{FET\_EN}$   | Time duration between I2C write/ACK and FET enable asserted    | Applicable to all FET enable pins   | -   | -   | 10  | $\mu$ s |
| $T_{FET\_DIS}$  | Time duration between I2C write/ACK and FET enable de-asserted | Applicable to all FET enable pins   | -   | -   | 10  | $\mu$ s |
| $I_{DD,Active}$ | Active mode operating current                                  | UFP role; attached condition; $V_{DD} = 3.3$ V  | -   | 200 | -   | $\mu$ A |
|                 |  | SPI interface is active   | -   | 3   | -   | mA      |
|                 |  | PD mode is functional; does not include power delivered on V_MCUPWR pin; $V_{DD} = 3.3$ V | -   | 3   | -   | mA      |
| $I_{DD(idle)}$  | Idle mode current on VDD                                       | UFP role; Unattached condition  | -   | 50  | -   | $\mu$ A |
| $I_{VIO(idle)}$ | Idle mode supply current (VIO)                                 |   | -   | -   | 10  | $\mu$ A |
| $I_{bckdrv}$    | Backdrive current  | Backdrive current on VDD pin when that pin is at 0 V                                      |     |     |     |         |
|                 |  | CC1, CC2 = 5 V  | -10 | -   | 10  | $\mu$ A |

## 11.2 USB PD and Type-C characteristics

**Table 9. USB PD and Type-C AC/DC characteristics**

Applicable across operating temperature and power supply ranges as per [Section 10](#) (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

| Symbol  | Parameter  | Conditions  | Min  | Typ   | Max  | Unit |
|---|--|---|------|-------|------|------|
| <b>USB PD normative specification</b>             |  |   |      |       |      |      |
| f <sub>Bitrate</sub>                              | Bit rate   |   | 270  | 300   | 330  | Kbps |
| t <sub>UnitInterval</sub>                         | unit interval  |   | 3.03 | -     | 3.7  | μs   |
| p <sub>BitRate</sub>                              | Maximum difference between the bit-rate during the payload and the reference bit-rate (The reference bit rate is the average bit rate of the last 32 bits of the preamble) | At the transmitter  | -    | -     | 0.25 | %    |
| t <sub>InterFrameGap</sub>                        | Time from the end of last bit of a Frame until the start of the first bit of the next Preamble.  |   | 25   | -     | -    | μs   |
| t <sub>StartDrive</sub>                           | Time before the start of the first bit of the Preamble when the transmitter shall start driving the line.  |   | -1   | -     | -    | μs   |
| <b>USB PD transmitter normative specification</b> |  |   |      |       |      |      |
| t <sub>EndDriveBMC</sub>                          | Time to cease driving the line after the end of the last bit of the Frame.   | Min value is limited by t <sub>HoldLowBMC</sub>   | -    | -     | 23   | μs   |
| t <sub>Fall</sub>                                 | Fall time  | 10 % and 90 % amplitude points, minimum is under unloaded condition   | 300  | -     | -    | ns   |
| t <sub>HoldLowBMC</sub>                           | Time to cease driving the line after the final high-to-low transition  | Max value is limited by t <sub>EndDriveBMC</sub>  | 1    | -     | -    | us   |
| t <sub>Rise</sub>                                 | Rise time  | 10 % and 90 % amplitude points, minimum is under unloaded condition   | 300  | -     | -    | ns   |
| V <sub>Swing</sub>                                | Voltage swing  |   | 1.05 | 1.125 | 1.2  | V    |
| Z <sub>Driver</sub>                               | Transmitter output impedance   | Source output impedance at the Nyquist frequency of [USB2.0] low speed (750 kHz) while the source is driving the CC line. | 33   | -     | 75   | Ω    |
| <b>USB PD receiver normative specification</b>    |  |   |      |       |      |      |
| C <sub>Receiver</sub>                             | CC Receiver capacitance  | The CC pin (DFP or UFP) capacitance when not transmitting on the line   | 200  | -     | 600  | pF   |
| n <sub>TransitionCount</sub>                      | Transitions for signal detect  |   | 3    | -     | -    |      |
| t <sub>RxFilter</sub>                             | Time constant of Rx bandwidth limiting filter  |   | 100  | -     | -    | ns   |

**Table 9. USB PD and Type-C AC/DC characteristics ...continued**

Applicable across operating temperature and power supply ranges as per [Section 10](#) (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

| Symbol                        | Parameter                                       | Conditions  | Min  | Typ  | Max  | Unit             |
|-------------------------------|---|---|------|------|------|------------------|
| $t_{\text{TransitionWindow}}$ | Time window for detecting non-idle              |   | 12   | -    | 20   | $\mu\text{s}$    |
| $Z_{\text{BmcRx}}$            | Receiver Input Impedance                        |   | 1    | -    | -    | $\text{M}\Omega$ |
| <b>Type-C specification</b>   |   |   |      |      |      |                  |
| $I_{\text{pullup}}$           | Current source for DFP pullup indication        | Default current   | 76   | 80   | 84   | $\mu\text{A}$    |
|                               |   | 1.5 A   | 171  | 180  | 189  | $\mu\text{A}$    |
|                               |   | 3 A   | 314  | 330  | 346  | $\mu\text{A}$    |
| $R_{\text{pulldn}}$           | Pulldown termination on UFP                     | After on-board calibration is completed                   | 4.6  | 5.1  | 5.6  | $\text{k}\Omega$ |
| $Z_{\text{OPEN}}$             | UFP CC termination                              | Applies to self-powered UFP to remain undetectable by DFP | 126  | -    | -    | $\text{k}\Omega$ |
| $V_{\text{CLAMPH}}$           | High current mode clamp voltage                 | UFP mode; VDD = 0, VBUS = 0                               | 0.85 | -    | 2.18 | V                |
| $V_{\text{CLAMPM}}$           | Medium current mode clamp voltage               | UFP mode; VDD = 0, VBUS = 0                               | 0.45 | -    | 1.25 | V                |
| $V_{\text{CLAMPD}}$           | Default current mode clamp voltage              | UFP mode; VDD = 0, VBUS = 0                               | 0.25 | -    | 1.25 | V                |
| $V_{\text{TUM}}$              | Medium current mode detection threshold         | UFP mode  | 1.16 | 1.23 | 1.31 | V                |
| $V_{\text{TUS}}$              | Standard current mode detection threshold       | UFP mode  | 0.61 | 0.66 | 0.70 | V                |
| $V_{\text{TURa}}$             | Powered Accessory (Ra) mode detection threshold | UFP mode  | 0.15 | 0.2  | 0.25 | V                |
| $V_{\text{TDH,Ra}}$           | High current mode Ra detection threshold        | DFP mode  | 0.75 | 0.8  | 0.85 | V                |
| $V_{\text{TD,Rd}}$            | Rd detection threshold                          | DFP mode  | 2.45 | 2.6  | 2.75 | V                |
| $V_{\text{TDM,Ra}}$           | Medium current mode Ra detection threshold      | DFP mode  | 0.35 | 0.4  | 0.45 | V                |
| $V_{\text{TDS,Ra}}$           | Standard current mode Ra detection threshold    | DFP mode  | 0.15 | 0.2  | 0.25 | V                |

[1] At present, only a limited set is listed out here; future data sheet revision would include all mandatory Type-C specifications [2].

### 11.3 Power AC/DC characteristics

**Table 10. Power AC/DC characteristics**

Applicable across operating temperature and power supply ranges as per [Section 10](#) (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).<sup>[1]</sup>

| Symbol                 | Parameter                                | Conditions   | Min | Typ | Max | Unit |
|------------------------|--|--|-----|-----|-----|------|
| V <sub>MCUPWR</sub>    | DC Voltage on V_MCUPWR pin               | Applies to both VBUS and VDD   | 2.5 | -   | 3.6 | V    |
| I <sub>MCUPWR</sub>    | DC Current delivered out of V_MCUPWR pin | Applies to both VBUS and VDD;<br><br>2.2 μF ±10 %<br>De-coupling capacitor on V_MCUPWR pin | -   | -   | 30  | mA   |
| I <sub>inrush</sub>    | Inrush current                           | 2.2 μF capacitors on BYPASS and V_MCUPWR pins, these pins are at 0 V                       | -   | 150 | -   | mA   |
| V <sub>OUT_load</sub>  | V_MCUPWR voltage                         | VBUS @ 3.7 V, load current 30 mA   | 2.5 | -   | 3.6 | V    |
| V <sub>Line_reg</sub>  | Line voltage regulation                  | VBUS sweep 3.7 V to 25 V; load current 30 mA   | -   | -   | 200 | mV   |
| V <sub>Load_reg</sub>  | Load voltage regulation                  | VBUS @ 3.7 V; load current sweep 0 mA to 30 mA   | -   | -   | 50  | mV   |
| V <sub>Load_step</sub> | Load voltage variation under load step   | VBUS @ 3.7 V; load current step from 0 to 30 mA over 30 μS interval                        | -   | -   | 150 | mV   |
| PSRR                   | Power supply rejection ratio             | VBUS @ 3.7 V to 25 V   |     |     |     |      |
|                        |  | DC   | -   | 70  | -   | dB   |
|                        |  | F = 100 kHz  | -   | 50  | -   | dB   |
|                        |  | F = 1 MHz  | -   | 30  | -   | dB   |

[1] For all the specification measurements, supply decoupling capacitor 2.2 μA ±10 % is considered to be present on V\_MCUPWR pin. Also, the capacitor is charged up to V\_MCUPWR voltage unless otherwise specified.

### 11.4 I2C characteristics

**Table 11. I2C characteristics**

Applicable across operating temperature and power supply ranges as per [Section 10](#) (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).<sup>[1]</sup>

| Symbol           | Parameter                                    | Conditions  | Min         | Typ | Max         | Unit |
|------------------|--|-------------|-------------|-----|-------------|------|
| f <sub>I2C</sub> | I2C clock frequency                          |             | 0           | -   | 1000        | kHz  |
| V <sub>IH</sub>  | HIGH-level Input voltage                     |             | 0.7 × VDDIO | -   | -           | V    |
| V <sub>IL</sub>  | LOW-level Input voltage                      |             | -           | -   | 0.3 × VDDIO | V    |
| V <sub>hys</sub> | Hysteresis of Schmitt trigger inputs         | VDDIO > 2 V | 0.05× VDDIO | -   | -           | V    |
|                  |  | VDDIO < 2 V | 0.1×VDDIO   | -   | -           | V    |
| V <sub>OL</sub>  | LOW-level output voltage at 3mA sink current | VDDIO > 2 V | 0           | -   | 0.4         | V    |
|                  |  | VDDIO < 2 V | 0           | -   | 0.2× VDDIO  | V    |

**Table 11. I2C characteristics ...continued**

Applicable across operating temperature and power supply ranges as per [Section 10](#) (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).<sup>[1]</sup>

| Symbol              | Parameter   | Conditions  | Min  | Typ | Max | Unit |
|---------------------|---|---|------|-----|-----|------|
| I <sub>OL</sub>     | LOW-level output current                                      | V <sub>OL</sub> = 0.4 V;<br>Standard and Fast modes                   | 3    | -   | -   | mA   |
|                     |   | V <sub>OL</sub> = 0.4 V;<br>Fast mode plus                            | 20   | -   | -   | mA   |
|                     |   | V <sub>OL</sub> = 0.6 V;<br>Fast mode                                 | 6    | -   | -   | mA   |
| I <sub>IL</sub>     | LOW-level input current                                       | Pin voltage - 0.1×V <sub>DDIO</sub><br>to 0.9×V <sub>IO</sub> , max   | -10  | -   | 10  | μA   |
| C <sub>I</sub>      | Capacitance of IO pin   |   | -    | -   | 10  | pF   |
| t <sub>HD,STA</sub> | Hold time (repeated) START condition                          | Fast mode plus; After this period, the first clock pulse is generated | 0.26 | -   | -   | μs   |
| t <sub>LOW</sub>    | LOW period of I2C clock                                       | Fast mode plus  | 0.5  | -   | -   | μs   |
| t <sub>HIGH</sub>   | HIGH period of I2C clock                                      | Fast mode plus  | 0.26 | -   | -   | μs   |
| t <sub>SU,STA</sub> | Setup time (repeated) START condition                         | Fast mode plus  | 0.26 | -   | -   | μs   |
| t <sub>HD,DAT</sub> | Data Hold time  | Fast mode plus  | 0    | -   | -   | μs   |
| t <sub>SU,DAT</sub> | Data Setup time   | Fast mode plus  | 50   | -   | -   | ns   |
| t <sub>r</sub>      | Rise time of I2C_SCL and I2C_SDA signals                      | Fast mode plus  | -    | -   | 120 | ns   |
| t <sub>f</sub>      | Fall time of I2C_SCL and I2C_SDA signals                      | Fast mode plus  | -    | -   | 120 | ns   |
| t <sub>SU,STO</sub> | Setup time for STOP condition                                 | Fast mode plus  | 0.26 | -   | -   | μs   |
| t <sub>BUF</sub>    | Bus free time between STOP and START condition                | Fast mode plus  | 0.5  | -   | -   | μs   |
| t <sub>VD,DAT</sub> | Data valid time   | Fast mode plus  | 0.45 | -   | -   | μs   |
| t <sub>VD,ACK</sub> | Data valid acknowledge time                                   | Fast mode plus  | 0.45 | -   | -   | μs   |
| t <sub>SP</sub>     | Pulse width of spikes that must be suppressed by input filter |   | -    | -   | 50  | ns   |

[1] V<sub>DDIO</sub> is I2C-bus pull up voltage.

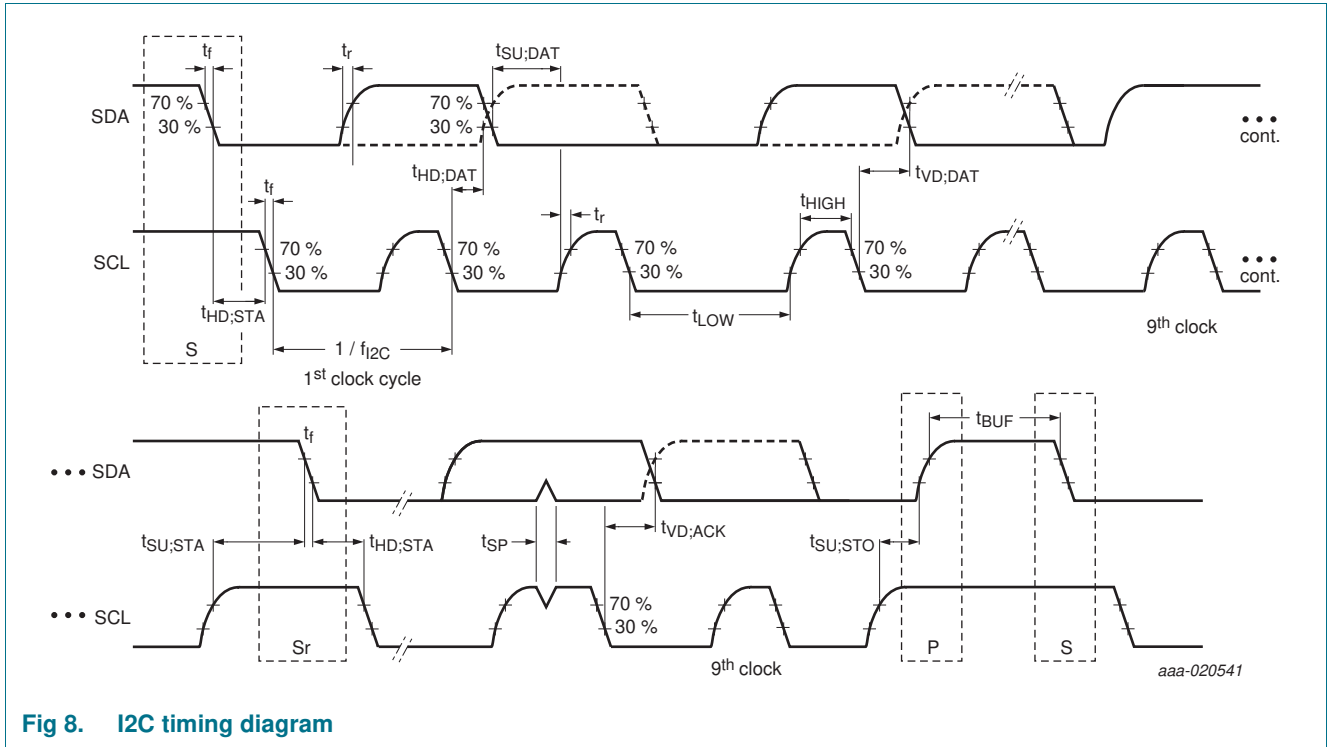


Fig 8. I2C timing diagram

## 11.5 SPI characteristics

**Table 12. SPI interface: AC/DC characteristics**

Applicable across operating temperature and power supply ranges as per [Section 10](#) (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

| Symbol                | Parameter                            | Conditions   | Min                             | Typ | Max                             | Unit |
|-----------------------|--------------------------------------|--|---------------------------------|-----|---------------------------------|------|
| f <sub>SPI</sub>      | SPI clock frequency (SPI_CLK)        | Applies to both TX and RX                                | -                               | -   | 20                              | MHz  |
| t <sub>SPI;HI</sub>   | SPI clock HIGH time                  |  | 20                              | -   | -                               | ns   |
| t <sub>SPI;LO</sub>   | SPI clock LOW time                   |  | 20                              | -   | -                               | ns   |
| t <sub>SPI;rise</sub> | SPI clock (LOW to HIGH) rise time    |  | 0.1                             | -   | -                               | V/ns |
| t <sub>SPI;fall</sub> | SPI clock (HIGH to LOW) fall time    |  | 0.1                             | -   | -                               | V/ns |
| t <sub>SPI;CSNS</sub> | SPI_CS Not Setup time                | Relative to SPI clock pin                                | 0                               | -   | -                               | ns   |
| t <sub>SPI;CSNH</sub> | SPI_CS Not Hold time                 | Relative to SPI clock pin                                | 0                               | -   | -                               | ns   |
| t <sub>SPI;DINS</sub> | Data In Setup time                   | Applies to SPI_MOSI_I2C_SDA; relative to SPI clock       | 5                               | -   | -                               | ns   |
| t <sub>SPI;DINH</sub> | Data In Hold time                    | Applies to SPI_MOSI_I2C_SDA; relative to SPI clock       | 5                               | -   | -                               | ns   |
| t <sub>SPI;DONS</sub> | SPI clock edge to Valid Data Out     | Applies to SPI_MISO                                      | -                               | -   | 7                               | ns   |
| t <sub>SPI;DONH</sub> | SPI clock edge to Data Out Hold time | Applies to SPI_MISO                                      | 0                               | -   | -                               | ns   |
| C <sub>L;SPI</sub>    | Maximum IO capacitance supported     | SPI_CLK_I2C_SCL, SPI_MOSI_I2C_SDA                        | -                               | -   | 10                              | pF   |
| C <sub>IN;SPI</sub>   | Maximum IO capacitance               | SPI_MISO, SPI_CS   | -                               | -   | 10                              | pF   |
| V <sub>IH;SPI</sub>   | HIGH-level input voltage             | SPI_MISO   | 0.7×<br>V <sub>MCUP</sub><br>WR | -   | -                               | V    |
| V <sub>IL;SPI</sub>   | LOW-level input voltage              | SPI_MISO   | -                               | -   | 0.3×<br>V <sub>MCU</sub><br>PWR | V    |
| V <sub>OL;SPI</sub>   | LOW-level output voltage             | SPI_CLK_I2C_SCL, SPI_CS, SPI_MOSI_I2C_SDA<br>IOL = 4 mA  | -                               | -   | 0.5                             | V    |
| V <sub>OH;SPI</sub>   | HIGH-level output voltage            | SPI_CLK_I2C_SCL, SPI_CS, SPI_MOSI_I2C_SDA<br>IOH = -4 mA | V <sub>MCUP</sub><br>WR - 0.5   | -   | -                               | V    |
| I <sub>LIH;EN</sub>   | HIGH-level input leakage current     | VI = 3.3 V   | -1                              | -   | 1                               | μA   |
| I <sub>LIL;EN</sub>   | LOW-level input leakage current      | VI = GND   | -1                              | -   | 1                               | μA   |

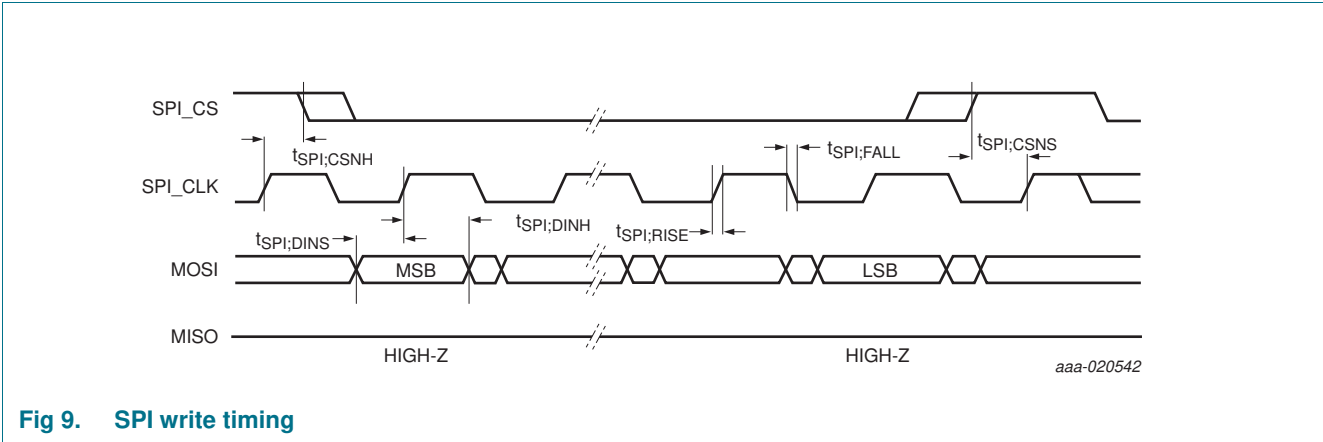


Fig 9. SPI write timing

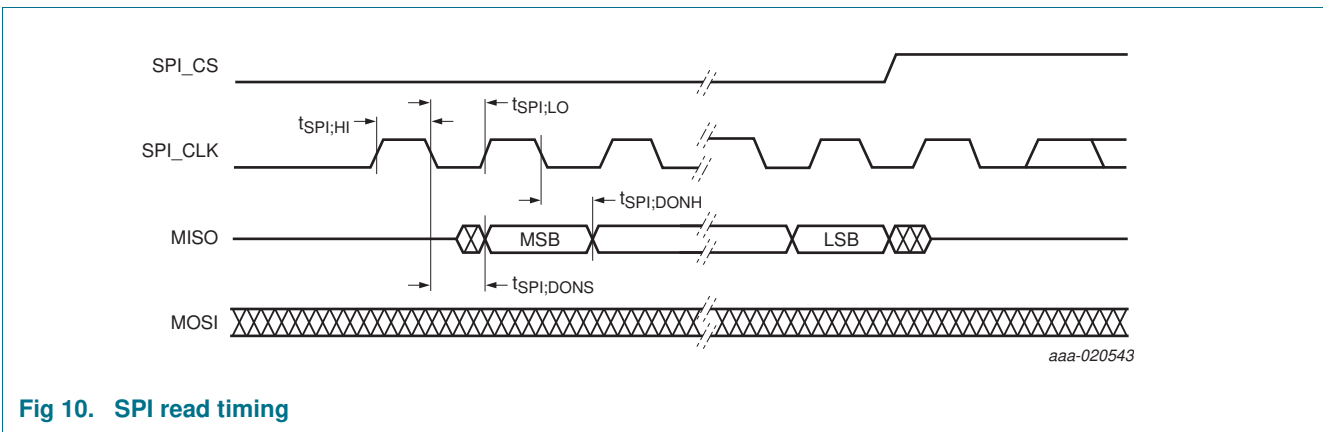


Fig 10. SPI read timing

### 11.6 CONTROL IO characteristics

Table 13. Control I/O characteristics

Applicable across operating temperature and power supply ranges as per Section 10 (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

| Symbol   | Parameter                        | Conditions                | Min            | Typ | Max                 | Unit          |
|--|----------------------------------|---------------------------|----------------|-----|---------------------|---------------|
| <b>System side CMOS output pins (CC_ORIENT)</b>          |                                  |                           |                |     |                     |               |
| $V_{OH}$   | HIGH-level Output voltage        | $I_{OH} = -2 \text{ mA}$  | $V_{IO} - 0.4$ | -   |                     | V             |
| $V_{OL}$   | LOW-level Output voltage         | $I_{OL} = 4 \text{ mA}$   | -              | -   | 0.5                 | V             |
| $C_I$  | Capacitance of IO pin            |                           | -              | -   | 20                  | pF            |
| $I_{LIH,EN}$   | HIGH-level input leakage current | $V_I = 3.3 \text{ V}$     | -1             | -   | 1                   | $\mu\text{A}$ |
| $I_{LIL,EN}$   | LOW-level input leakage current  | $V_I = \text{GND}$        | -1             | -   | 1                   | $\mu\text{A}$ |
| <b>System side input pins (CC_CTRL1, SLV_ADDR, TST0)</b> |                                  |                           |                |     |                     |               |
| $V_{IL}$   | LOW-level input voltage          | applies to CC_CTRL1, TST0 | -              | -   | 0.4                 | V             |
|  |                                  | applies to SLV_ADDR       | -              | -   | $0.3 \times V_{DD}$ | V             |



**Table 13. Control I/O characteristics**

Applicable across operating temperature and power supply ranges as per [Section 10](#) (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

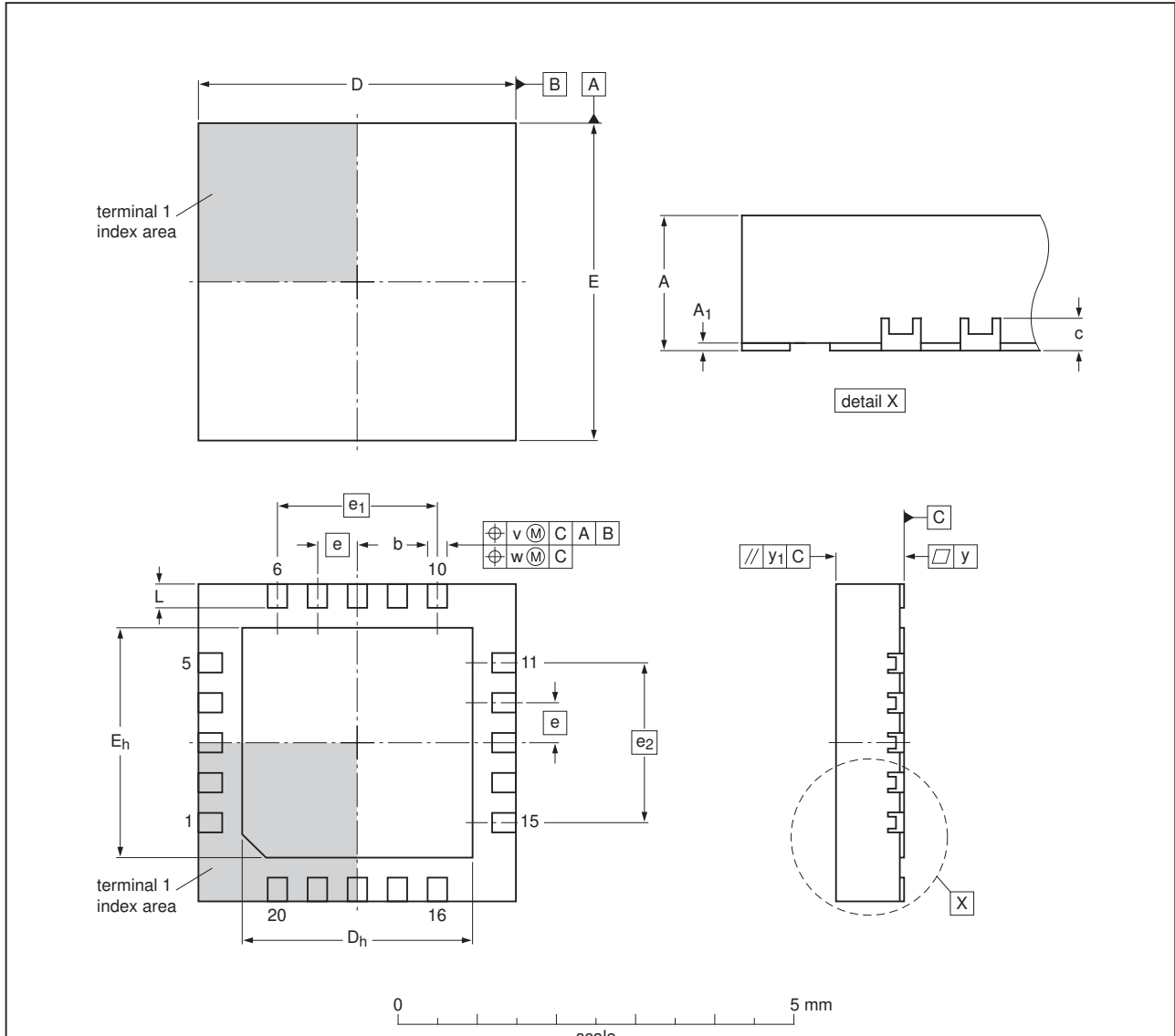
| Symbol   | Parameter                        | Conditions                  | Min                     | Typ | Max | Unit          |
|--|----------------------------------|-----------------------------|-------------------------|-----|-----|---------------|
| $V_{IH}$   | HIGH-level input voltage         | applies to SLV_ADDR         | $0.7 \times VDD$        | -   | -   | V             |
| $C_I$  | Capacitance of IO pin            | applies to CC_CTRL1 only    | -                       | -   | 20  | pF            |
|  |                                  | applies to SLV_ADDR         | -                       | -   | 20  | pF            |
| $I_{LIH,EN}$   | HIGH-level input leakage current | $V_I = 3.3\text{ V}$        | -1                      | -   | 1   | $\mu\text{A}$ |
| $I_{LIL,EN}$   | LOW-level input leakage current  | $V_I = \text{GND}$          | -1                      | -   | 1   | $\mu\text{A}$ |
| <b>System side open drain interface pins (INT_N); pulled up to VDDIO</b> |                                  |                             |                         |     |     |               |
| $V_{OL}$   | LOW-level Output voltage         | $I_{OL} = 4\text{ mA}$      | -                       | -   | 0.5 | V             |
| $C_I$  | Capacitance of IO pin            |                             | -                       | -   | 20  | pF            |
| <b>FET enable pins (EN_USBSRC, EN_USBFET1, EN_USBFET2)</b>               |                                  |                             |                         |     |     |               |
| $V_{OL,EN}$  | LOW-level output voltage         | $I_{OL} = 4\text{ mA};$     | -                       | -   | 0.5 | V             |
| $V_{IH,EN}$  | HIGH-level input voltage         | FET enable pins are in Hi-Z | $0.7 \times V_{MCUPWR}$ | -   | 25  | V             |
| $I_{LIH,EN}$   | HIGH-level input leakage current | $V_I = 25\text{ V}$         | -1                      | -   | 1   | $\mu\text{A}$ |
| $I_{LIL,EN}$   | LOW-level input leakage current  | $V_I = \text{GND}$          | -1                      | -   | 1   | $\mu\text{A}$ |

[1] VFET\_Bias is the bias voltage on the FET enable pins

12. Package outline

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads;  
20 terminals; body 4 x 4 x 0.85 mm

SOT917-4



Dimensions

| Unit | A    | A <sub>1</sub> | b    | c   | D <sup>(1)</sup> | D <sub>h</sub> | E <sup>(1)</sup> | E <sub>h</sub> | e   | e <sub>1</sub> | e <sub>2</sub> | L    | v   | w    | y    | y <sub>1</sub> |
|------|------|----------------|------|-----|------------------|----------------|------------------|----------------|-----|----------------|----------------|------|-----|------|------|----------------|
| max  | 1.00 | 0.05           | 0.30 |     | 4.1              | 3.0            | 4.1              | 3.0            |     |                |                | 0.35 |     |      |      |                |
| nom  | 0.85 |                | 0.25 | 0.2 | 4.0              | 2.9            | 4.0              | 2.9            | 0.5 | 2              | 2              | 0.30 | 0.1 | 0.05 | 0.08 | 0.1            |
| min  | 0.80 |                | 0.20 |     | 3.9              | 2.8            | 3.9              | 2.8            |     |                |                | 0.25 |     |      |      |                |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot917-4\_po

| Outline version | References |        |       | European projection | Issue date           |
|-----------------|------------|--------|-------|---------------------|----------------------|
|                 | IEC        | JEDEC  | JEITA |                     |                      |
| SOT917-4        |            | MO-220 | ---   |                     | 14-10-27<br>14-11-07 |

Fig 11. Package outline SOT917-4 (HVQFN20)