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PUSB3AB4

ESD protection for ultra high-speed interfaces

Rev. 2 — 4 May 2016

Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as SuperSpeed USB 3.1 at 10 Gbps, High-Definition Multimedia Interface (HDMI), DisplayPort, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes a high-level ESD protection diode structure protecting sensitive transmitters and receivers for ultra high-speed signal lines. The device is encapsulated in a leadless small DFN2510A-10 (SOT1176-1) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.2 pF maximum. These diodes utilize a snapback structure in order to provide protection to downstream components from ESD voltages up to ± 15 kV contact exceeding IEC 61000-4-2, level 4.

1.2 Features and benefits

- System-level ESD protection for USB 2.0 and SuperSpeed USB 3.1 up to 10 Gbps, HDMI, DisplayPort, eSATA and LVDS
- Line capacitance of only 0.2 pF maximum for each channel
- Outstanding system protection: extremely deep snapback combined with dynamic resistance of only 0.4 Ω .
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ± 15 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Design-friendly 'pass-through' signal routing

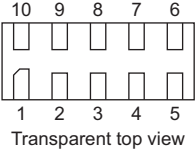
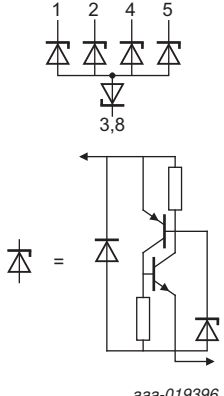
1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- Smartphones, tablet computers, Mobile Internet Devices (MID) and portable devices
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles

2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection		
2	CH2	channel 2 ESD protection		
3	GND	ground		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	n.c.	not connected		
7	n.c.	not connected		
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3AB4	DFN2510A-10	plastic extremely thin small outline package; no leads; 10 terminals; body 1 × 2.5 × 0.5 mm	SOT1176-1

4. Marking

Table 3. Marking codes

Type number	Marking code
PUSB3AB4	AB

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		−3.3	+3.3	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4 [1]			
		contact discharge	−15	+15	kV
		air discharge	−15	+15	kV
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	−7	7	A
T_{amb}	ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

[1] All pins to ground.

6. Characteristics

Table 5. Characteristics

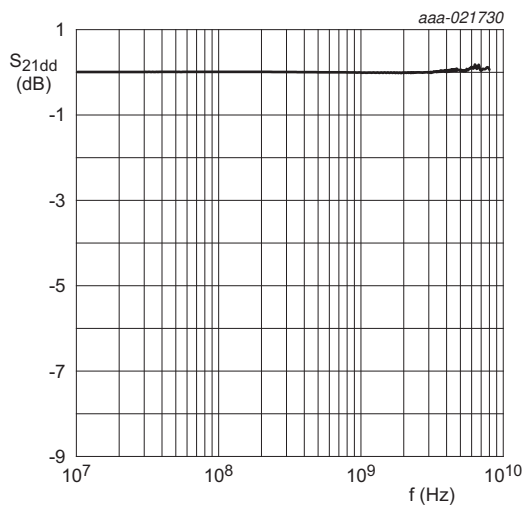
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BR}	breakdown voltage	$I_l = 1\text{ mA}$	5.5	9	-	V
I_{LR}	reverse leakage current	per channel; $V_l = 5\text{ V}$	-	<1	100	nA
C_{line}	line capacitance	$f = 1\text{ MHz}$; $V_l = 1.5\text{ V}$ [1]	-	0.17	0.2	pF
r_{dyn}	dynamic resistance	TLP [2]				
		positive transient	-	0.4	-	Ω
		negative transient	-	0.4	-	Ω
V_{sbck}	snapback voltage	$I_l = 1\text{ A}$; TLP 100/10 ns	-	3.3	-	V
V_{CL}	clamping voltage	$I_{PP} = 5\text{ A}$; positive transient [3]	-	5	-	V
		$I_{PP} = -5\text{ A}$; negative transient [3]	-	-5	-	V

[1] This parameter is guaranteed by design.

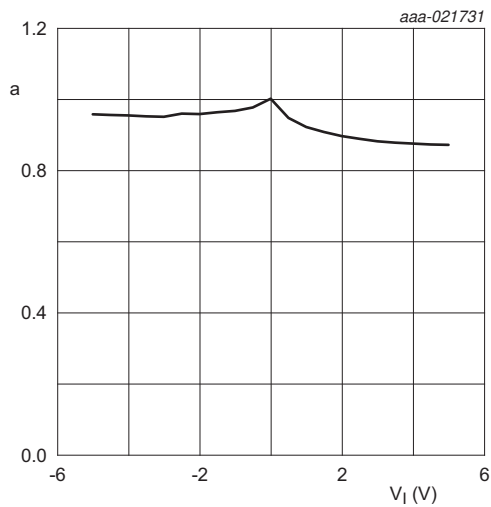
[2] 100 ns Transmission Line Pulse (TLP); 50 Ω ; pulser at 80 ns.

[3] According to IEC 61000-4-5 (8/20 μs current waveform).



differential mode

Fig 1. Insertion loss; typical values



$$a = \frac{C_{line}}{C_{line}(V_I = 0 \text{ V})}$$

Fig 2. Relative capacitance as a function of input voltage; typical values

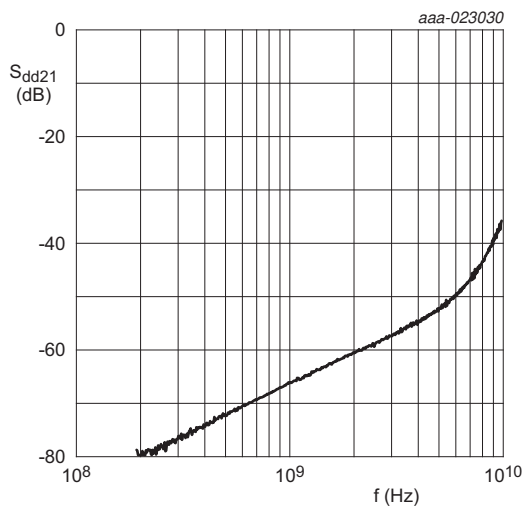
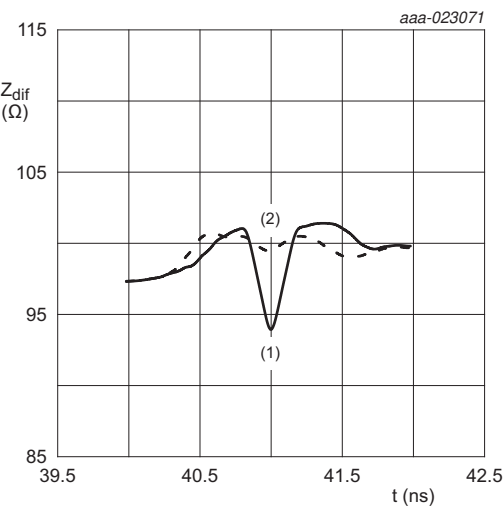


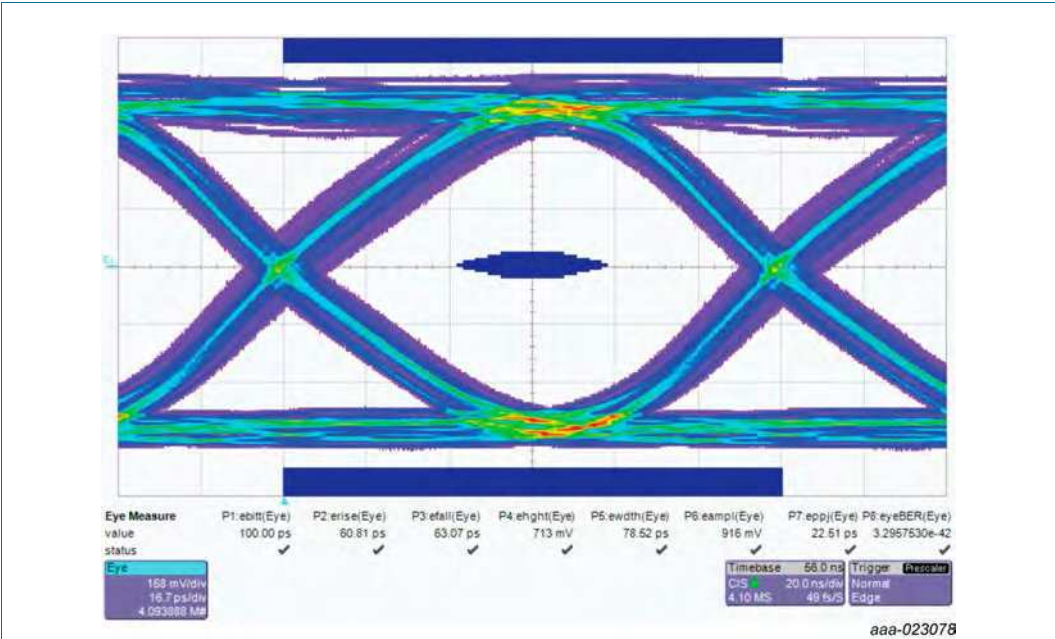
Fig 3. Differential crosstalk; typical values



$t_r = 200 \text{ ps}$

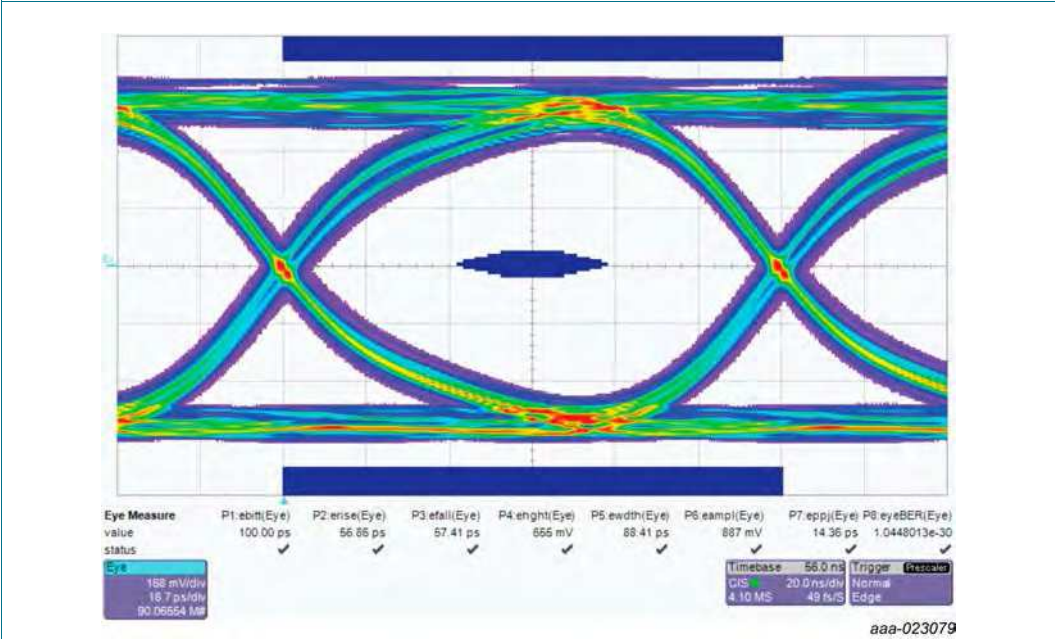
- (1) PUSB3AB4 on reference board
- (2) Reference board without Device Under Test (DUT)

Fig 4. Differential Time Domain Reflectometer (TDR) plot; typical values



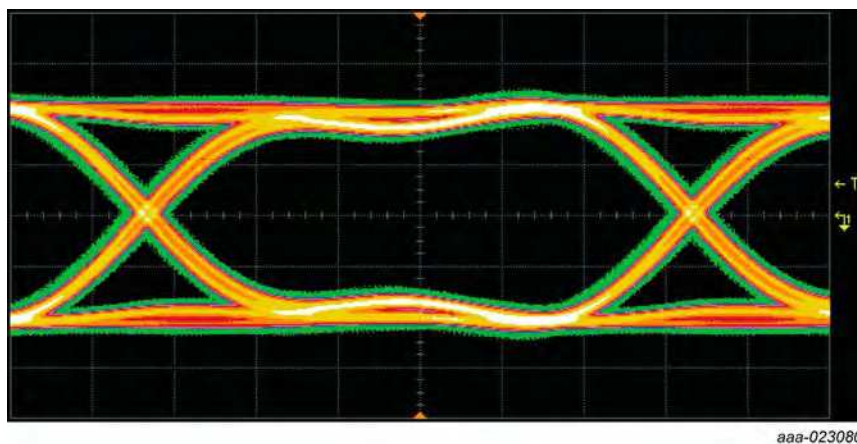
Data rate: 10 Gbit/s

Fig 5. USB 3.1 eye diagram, Printed-Circuit Board (PCB) with PUSB3AB4



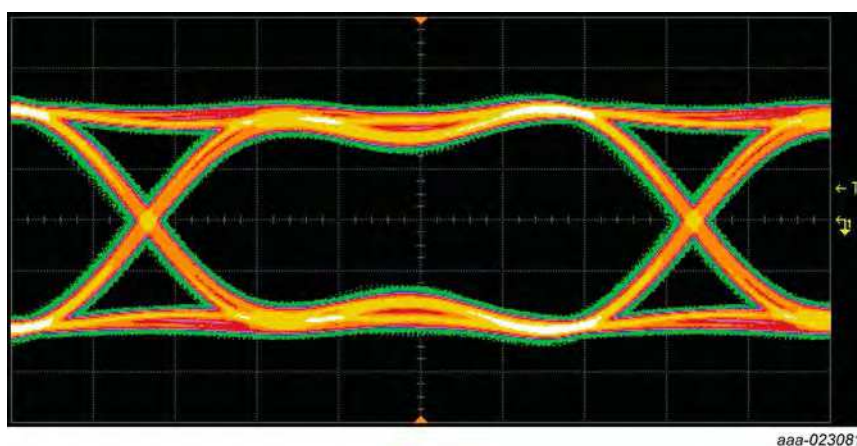
Data rate: 10 Gbit/s

Fig 6. USB 3.1 eye diagram, PCB without PUSB3AB4 (reference)



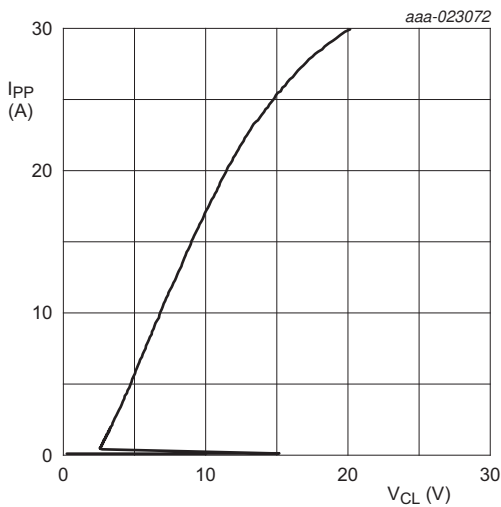
Test frequency: 148.5 MHz
Differential swing voltage: 840 mV
Horizontal scale: 25 ps/div

Fig 7. HDMI 2.0 TP1 eye diagram, PCB with PUSB3AB4



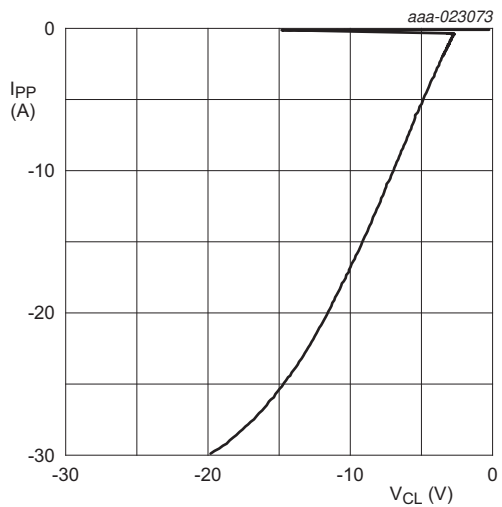
Test frequency: 148.5 MHz
Differential swing voltage: 906 mV
Horizontal scale: 25 ps/div

Fig 8. HDMI 2.0 TP1 eye diagram, PCB without PUSB3AB4



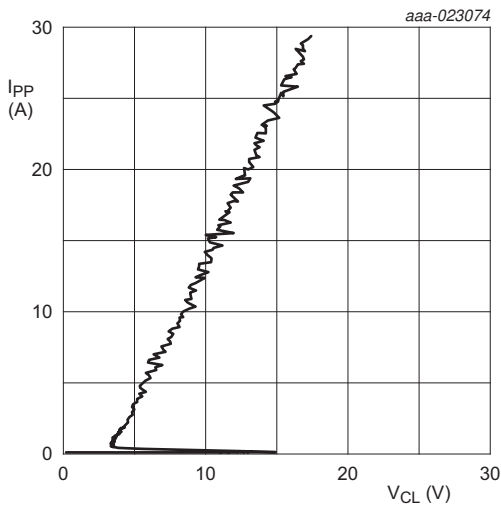
Transmission Line Pulse (TLP) = 100 ns

Fig 9. Dynamic resistance with positive clamping; typical values



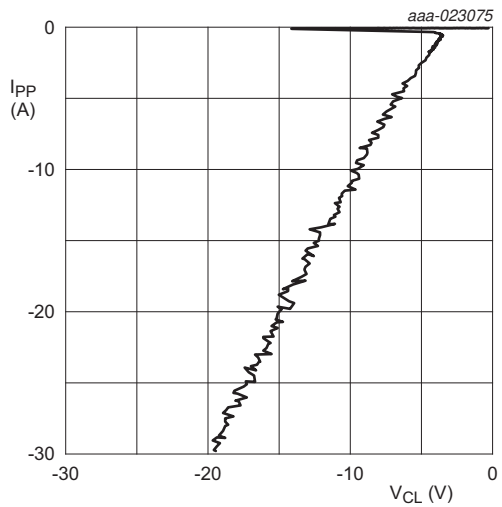
Transmission Line Pulse (TLP) = 100 ns

Fig 10. Dynamic resistance with negative clamping; typical values



Very-Fast Transmission Line Pulse (VF-TLP) = 5 ns

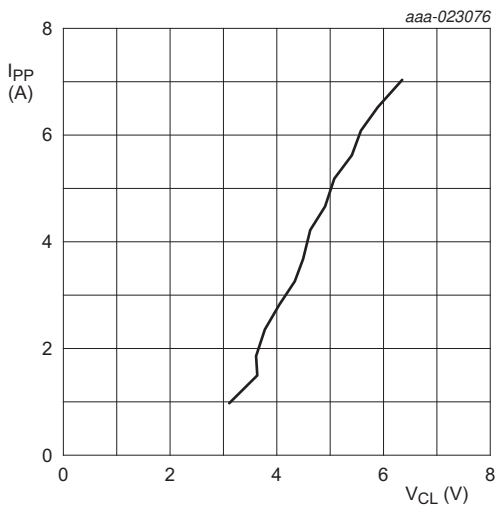
Fig 11. Dynamic resistance with positive clamping; typical values



Very-Fast Transmission Line Pulse (VF-TLP) = 5 ns

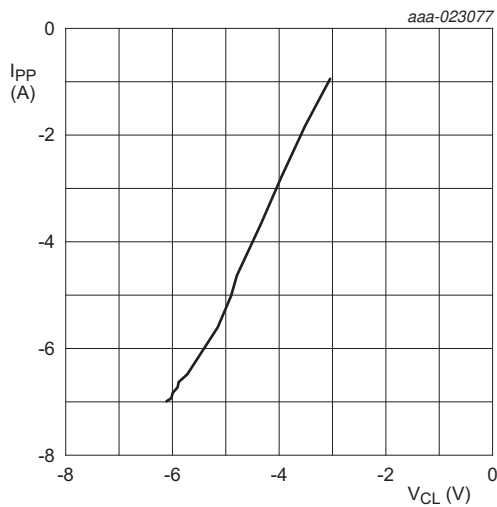
Fig 12. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snapback behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snapback state after exceeding breakdown voltage (due to an ESD pulse for instance).



According to IEC 61000-4-5 (8/20 μ s)

Fig 13. Dynamic resistance with positive clamping; typical values



According to IEC 61000-4-5 (8/20 μ s)

Fig 14. Dynamic resistance with negative clamping; typical values

7. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the PCB, give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

8. Package outline

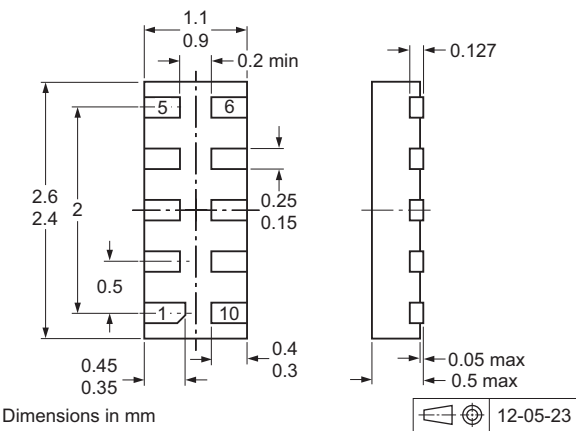


Fig 15. Package outline DFN2510A-10 (SOT1176-1)

9. Soldering

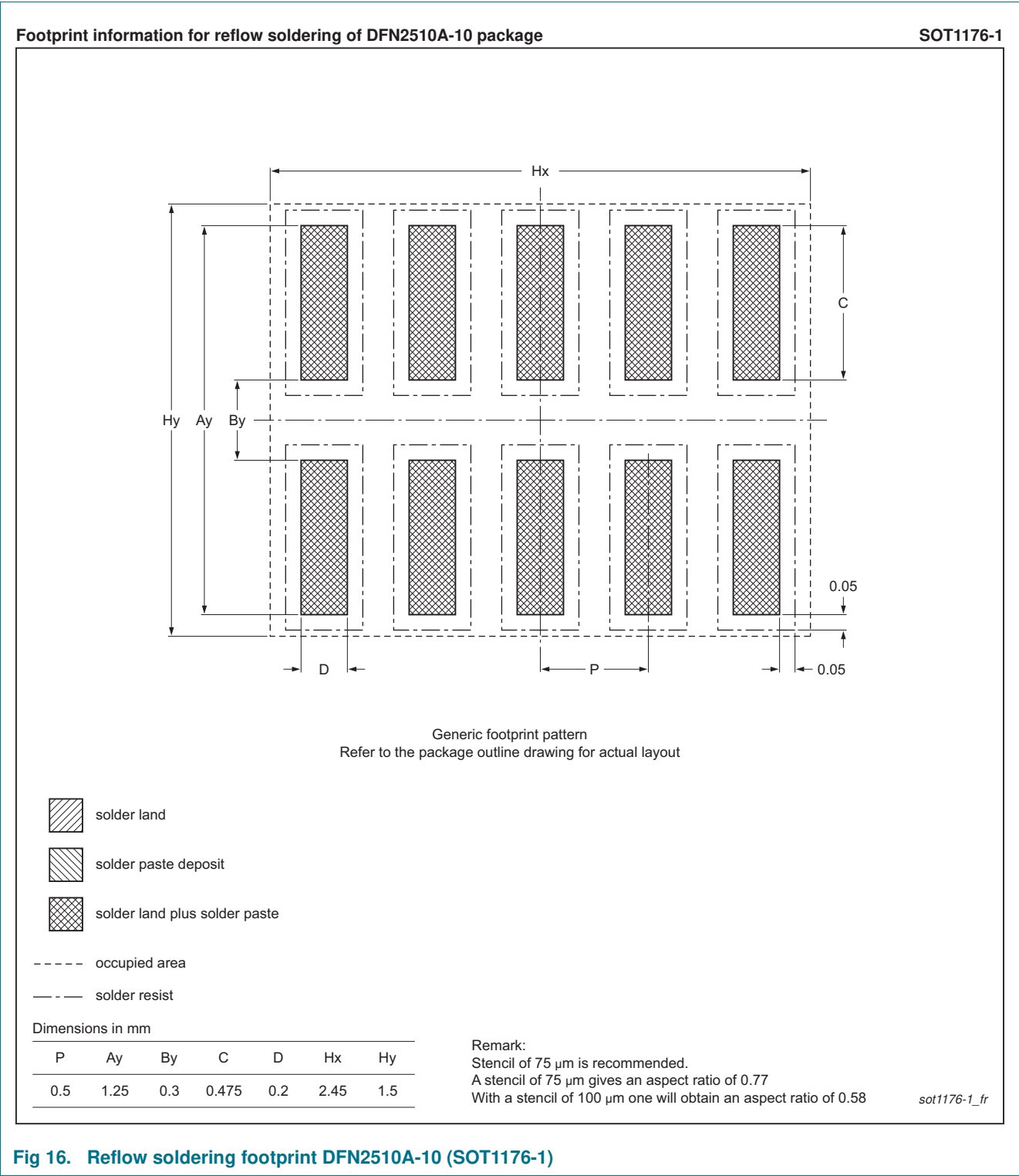


Fig 16. Reflow soldering footprint DFN2510A-10 (SOT1176-1)

10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3AB4 v.2	20160504	Product data sheet	-	PUSB3AB4 v.1
Modifications:	• Added Figure 1 to Figure 13			
PUSB3AB4 v.1	20150825	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
3	Ordering information	2
4	Marking	2
5	Limiting values	2
6	Characteristics	3
7	Application information	8
8	Package outline	8
9	Soldering	9
10	Revision history	10
11	Legal information	11
11.1	Data sheet status	11
11.2	Definitions	11
11.3	Disclaimers	11
11.4	Trademarks	12
12	Contact information	12
13	Contents	13