Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Document Number VYBRIDFSERIESEC
Rev 8, 11/2014

VYBRIDFSERIESEC

VF6xx, VF5xx, VF3xx

Features

- Operating characteristics
  - Voltage range 3 V to 3.6 V
  - Temperature range(ambient) -40 °C to 85 °C
- ARM® Cortex® A5 Core features
  - Up to 500 MHz ARM Cortex A5
  - 32 KB/32 KB I/D L1 Cache
  - 1.6 DMIPS/MHz based on ARMv7 architecture
  - NEON™ MPE (Media Processing Engine) Co-processor
  - Double Precision Floating Point Unit
  - 512 KB L2 cache (on selected part numbers only)
- ARM Cortex M4 Core features
  - Up to 167 MHz ARM Cortex M4
  - Integrated DSP capability
  - 64 KB Tightly Coupled Memory (TCM)
  - 16 KB/16 KB I/D L1 Cache
  - 1.25 DMIPS/MHz based on ARMv7 architecture
- Clocks
  - 24 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Internal reference clocks (128 KHz and 24 MHz)
  - Phase Locked Loops (PLLs)
  - Low Jitter Digital PLLs
- System debug, protection, and power management
  - Various stop, wait, and run modes to provide low power based on application needs
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Low voltage warning and detect with selectable trip points
  - Illegal opcode and illegal address detection with programmable reset or processor exception response
  - Hardware CRC module to support fast cyclic redundancy checks (CRC)
  - 128-bit unique chip identifier
  - Hardware watchdog
  - External Watchdog Monitor (EWM)
  - Dual DMA controller with 32 channels (with DMAMUX)
- Debug
  - Standard JTAG
  - 16-bit Trace port
- Timers
  - Motor control/general purpose timer (FTM)
  - Periodic Interrupt Timers (PITs)
  - Low-power timer (LPTMR0)
  - IEEE 1588 Timer per MAC interface (part of Ethernet Subsystem)
- Communications
  - Six Universal asynchronous receivers/transmitters (UART)/Serial communications interface (SCI) with LIN, ISO7816, IrDA, and hardware flow control
  - Four Deserial Serial peripheral interface (DSPI)
  - Four Inter-Integrated Circuit (I2C) with SMBUS support
  - Dual USB OTG Controller + PHY
  - Dual 4/8 bit Secure Digital Host controller
  - Dual 10/100 Ethernet with L2 Switch (IEEE 1588)
  - Dual FlexCAN3
- Security
  - ARM TrustZone including the TZ architecture
  - Cryptographic Acceleration and Assurance Module, incorporates 16 KB secure RAM (CAAM)
  - Secure Non-Volatile Storage, including Secure Real Time Clock (SNVS)
  - Real Time Integrity Checker (RTIC)
  - Tamper detection - supported by external pins, on-chip clock monitors, voltage and temperature tampers
  - TrustZone Watchdog (TZ WDOG)
  - Trust Zone Address Space Controller
  - Central Security Unit
  - Secure JTAG
  - High Assurance Boot (HAB) with support for encrypted boot
- Memory Interfaces
  - 8/16 bit DRAM Controller with support for LPDDR2/DDR3 - Up to 400 MHz (ECC supported for 8-bit only and not 16-bit)
  - 8/16 bit NAND Flash controller with ECC
  - 8/16/32 bit External bus (Flexbus)
  - Dual Quad SPI with XIP (Execute-In-Place)

- Display and Video
  - Dual Display Control Unit (DCU) with support for color TFT display up to SVGA
  - Segmented LCD (3V Glass only) configurable as 40x4, 38x8, and 36x6
  - Video Interface Unit (VIU) for camera
  - Open VG Graphics Processing Unit (GPU)
  - VideoADC
- Analog
  - Dual 12-bit SAR ADC with 1MS/s
  - Dual 12-bit DAC
- Audio
  - Four Synchronous Audio Interface (SAI)
  - Enhanced Serial Audio Interface (ESAI)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Asynchronous Sample Rate Converter (ASRC)
- Human-Machine Interface (HMI)
  - GPIO pins with interrupt support, DMA request capability, digital glitch filter.
  - Hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
- On-Chip Memory
  - 512 KB On-chip SRAM with ECC
  - 1 MB On-chip graphics SRAM (no ECC). This depends on the part selected. Alternate configuration could be 512 KB graphics and 512 KB L2 cache.
  - 96 KB Boot ROM

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web.

1. To determine the orderable part numbers for this device, go to www.freescale.com and search the required part number. The part numbering format is described in the section that follows.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Part Number Format

The figure below represents the format of part number of this device.

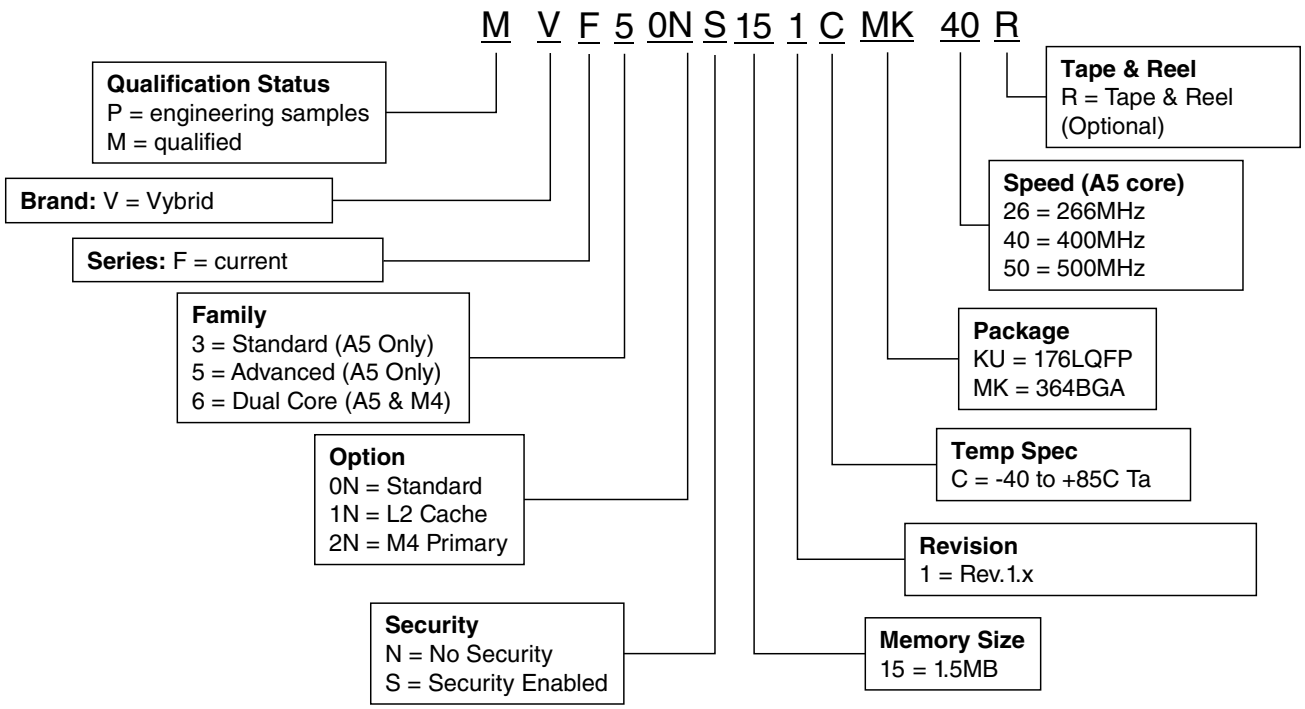


Figure 1. Part Number Format

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• P = Engineering samples • M = Qualified
B	Brand	• V = Vybrid
S	Series	• F = current
F	Family	• 3 = Standard (A5 Only) • 5 = Advanced (A5 Only) • 6 = Dual Core (A5 & M4)
O	Option	• 0N = Standard • 1N = L2 Cache • 2N = M4 Primary
S	Security	• N = No Security • S = Security Enabled
MM	Memory size	• 15 = 1.5 MB

Table continues on the next page...

Field	Description	Values
R	Revision	• 1 = Rev 1.x
T	Temperature range (°C)	• C = -40 °C to +85 °C T_a
PP	Package type	• KU = 176LQFP • MK = 364 MAPBGA
S	Speed	• Speed A5 Core • 26 = 266MHz • 40 = 400MHz • 50 = 500MHz

2.4 Part Numbers

This table lists the part numbers on the device.

Part Number	Package	Description
MVF30NN151CKU26	LQFP-EP 176 24*24*1.6	A5-266, No Security, 176LQFP
MVF30NS151CKU26	LQFP-EP 176 24*24*1.6	A5-266, Security, 176LQFP
MVF50NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, No Security, 364BGA
MVF50NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, Security, 364BGA
MVF50NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, No Security, 364BGA
MVF50NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, Security, 364BGA
MVF51NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, No Security, 364BGA
MVF51NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, Security, 364BGA
MVF60NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, No Security, 364BGA
MVF60NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, Security, 364BGA
MVF60NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, No Security, 364BGA
MVF60NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, Security, 364BGA
MVF61NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, No Security, 364BGA
MVF61NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, Security, 364BGA
MVF62NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, No Security, 364BGA

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

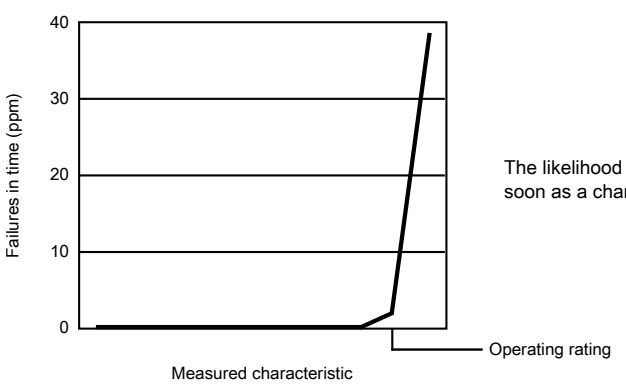
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

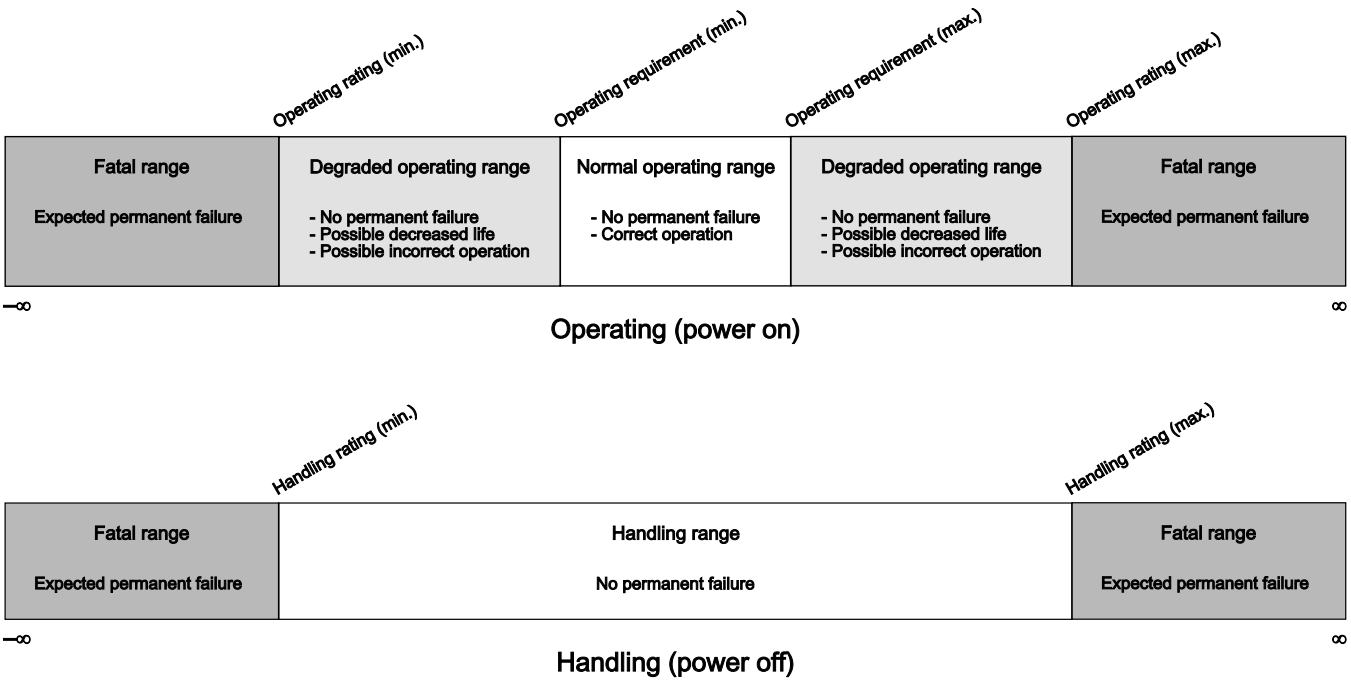
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

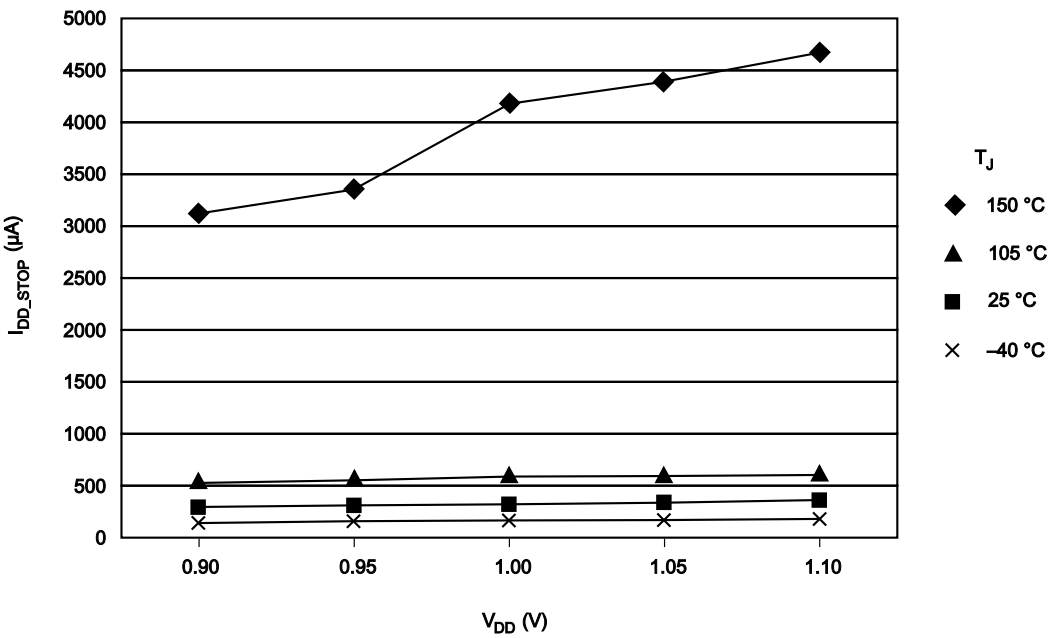
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Handling ratings

4.1 ESD Handling Ratings Table [JEDEC]

Symbol	Description	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	Corner pins: 750 Other pins: 500	V	2

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5 Operating Requirements

5.1 Thermal operating requirements

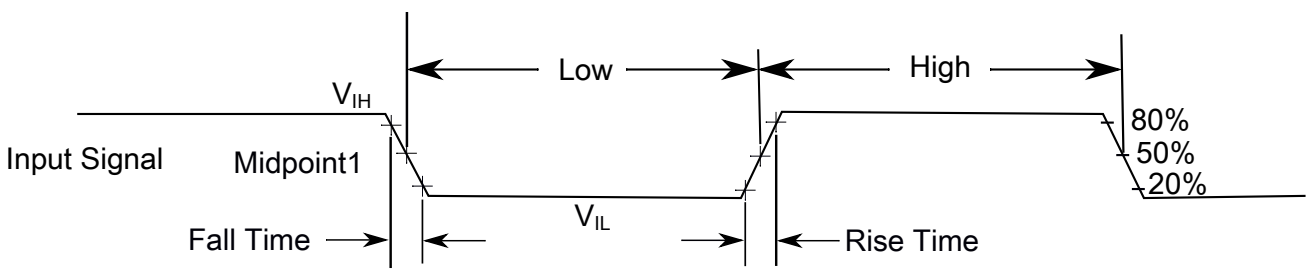
Table 1. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature	–40	85	°C
T_J	Junction temperature		105	°C

6 General

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

6.2 Nonswitching electrical specifications

6.2.1 VREG electrical specifications

6.2.1.1 HPREG electrical characteristics

Table 2. HPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	-
Current Consumption	-	1.2	1.5	mA	@ no load
	-	2.0	2.5	mA	@ full load
Output current capacity	-	600	1200[1]	mA	DC load current
Output voltage @ no load		1.23	1.26	V	
Output voltage @ full load	1.20	1.21		V	
External decoupling cap	4.7		-	µF	-
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total effective PAD+PCB trace resistances
PSRR with 4.7uF output cap					
@ DC @noload @ DC @full load @ worst case any frequency			-48 -40 -20	dB	

1. This is peak and not continuous maximum value.

6.2.1.2 LPREG electrical characteristics

Table 3. LPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	350	400		µA	@ no load
	-	500	650	µA	@ full load
Output current capacity		100	200	mA	DC load current
Output voltage @ no load		1.22	1.240	V	
Output voltage @ full load	1.180			V	
External decoupling cap	4.7			µF	
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total PAD+PCB trace resistance

Table continues on the next page...

Table 3. LPREG electrical characteristics (continued)

Parameters	Min	Typ	Max	Unit	Comments
PSRR with 4.7uF output cap					
@ DC @noload			-40	dB	
@ DC @full load			-35		
Worst case @ any frequency			-12		

6.2.1.3 ULPREG electrical characteristics

Table 4. ULPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	1.88	2.3	2.86	µA	@ no load
	-	610	670	µA	@ full load
Output current capacity			20	mA	DC load current
Output voltage @ no load			1.175	V	
Output voltage @ full load	1.125			V	
PSRR with 500 pF output cap	-20			dB	Worst case at any frequency across corners
@ DC @noload			-50	dB	
@200KHz @noload			-37		
@ DC @full load			-42		
@200KHz @full load			-37		
Worst case @ any frequency @ any load			-15		

6.2.1.4 WBREG electrical characteristics

Table 5. WBREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3	3.3	3.6	V	-
Current Consumption	-	2	5	µA	@ no load
	-	2	5	µA	@ full load
Output current capacity	-	1	2	mA	DC load current
Output voltage @ no load		1.4	1.425	V	
Output voltage @ full load	1.375	1.398		V	
Output voltage programmability	1.4	1.4	1.7	V	16 steps of 25 mV each

6.2.1.5 External NPN Ballast

The internal main regulator requires an external NPN ballast transistor to be connected as shown in the following figure as well as an external capacitance to be connected to the device in order to provide a stable 1.2V digital supply to the device. The HPREG design allows for collector voltage lower than VDDREG value. See AN4807 at www.freescale.com .

NOTE

To not overload BCTRL output, collector voltage should appear no later than VDDREG / VDD33 (3.3V).

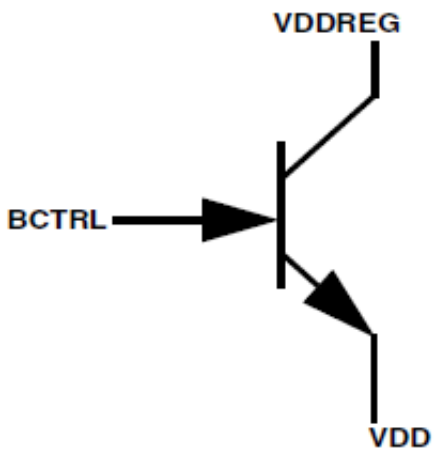


Figure 3. External NPN Ballast connections

Table 6. BCTRL OUTPUT specification

Parameter	Value	Comments
BCTRL OUTPUT specification	20mA	BCTRL driver can not drive more than 20mA current
Maximum pin voltage	VDDREG-0.5V	For Example, VDDREG =3.0V BCTRL should not exceed 2.5V.

Table 7. Assumptions For calculations

Parameter	Value
VDDREG	3.0V to 3.6V with typical value of 3.3V
Max DC Collector current	0.85A @85 °C
Emitter voltage	1.2V to 1.25V
Collector voltage	Equal to VDDREG

Table 8. General guidelines for selection of NPN ballast

Symbol	Parameters	Value	Unit	Comments
Hfe	Minimum DC current gain (Beta)	42.5		As BCTRL pin can not drive more than 20mA Minimum value of beta for a collector current of 0.85A comes out to be 42.5.
PD (Junction to ambient)	Minimum power dissipation @ TA=85 °C	2.04	W	Assuming 0.85A collector current with Collector voltage of Ballast 3.6V(max) we get VCE= 3.6V-1.2V=2.4V So power dissipated is 2.4V*0.85A=2.04W . This should be met for junction to ambient power dissipation spec of ballast
IcmaxDC peak	Maximum peak DC collector current	0.85	A	1.2A and above capacity device preferable
VBE	Maximum voltage that BCTRL pin can drive	1.25V for 0.85A @ 85 °C	V	For a VDDREG of 3.0 V (min.), BCTRL pin can drive voltage up to VDDREG - 0.5 V = 2.5 V. Since emitter of ballast is fixed at 1.25 V (max) if chosen ballast can supply 0.85 A collector current @ 85 °C with a base-to-emitter voltage of 1.25 V or lower, it is suitable for application.
Ft	Unity current gain Frequency of Ballast	50	MHz	

Reducing the collector-to-emitter voltage drop lowers the ballast transistor heat dissipation. This can be implemented in two ways:

1. By introducing series resistor or diode(s) between the collector and VDDREG (placed far enough from the transistor for proper cooling)
2. By connecting the collector to a separate lower-voltage supply

In both of the above cases the transistor has to stay away from the deep saturation region; otherwise, due to significant Hfe degradation, its base current exceeds the BCTRL output maximum value.

In general, the transistor must be selected such that its Vce saturation voltage is lower than the expected minimum Collector-Emitter voltage, and at the same time, the base current is less than 20 mA for the maximum expected collector current. More information can be found in collateral documentation at http://www.freescale.com

6.2.2 LVD electrical specifications

6.2.2.1 Main Supply electrical characteristics

Table 9. LVD_MAIN supply electrical characteristics

Main Supply LVD Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold (value @27°C)		2.76	2.915	V	
Lower voltage threshold (value @27°C)	2.656	2.73		V	
Time constant of RC filter at LVD input (0.69*RC)	3.3			µs	3.3 V noise rejection at LVD comparator input

6.2.2.2 LVD DIG characteristics

Table 10. LVD DIG electrical specifications [HPREG(RUN MODE) and LPREG(STOP MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.135	1.16	1.185	V	
Lower voltage threshold	1.105	1.13	1.155	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

Table 11. LVD DIG electrical specifications [ULPREG(STANDBY MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.105	1.13	1.155	V	
Lower voltage threshold	1.075	1.10	1.125	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

6.2.3 LDO electrical specifications

6.2.3.1 LDO_1P1

Table 12. LDO_1P1 parameters

Specification	Min	Typ	Max	Unit	Comments
VDDIO	3	3.3	3.6	V	IO supply
VDD1P1_OUT	0.9	1.1	1.2	V	Regulator output
I_out	-		150	mA	>= 300mV drop out
Regulator output programming range	0.8	1.1	1.4	V	Programmable in 25mV steps
Brownout Voltage	0.85	0.94		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

For additional information, see the device reference manual.

6.2.3.2 LDO_2P5

Table 13. LDO_2P5 parameters

Specification	Min	Typ	Max	Unit	Comments
VDDIO	3	3.3	3.6	V	IO supply
VDD2P5_OUT	2.3	2.5	2.6	V	Regulator output
I_out	-		350	mA	@500mV drop out
Regulator output programming range	2.0	2.5	2.75	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.25	2.33		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

For additional information, see the reference manual.

6.2.3.3 LDO_3P0

Table 14. LDO_3P0 parameters

Specification	Min	Typ	Max	Unit	Comments
Input OTG VBUS Supply	4.4		5.25	V	
Input HOST VBUS Supply	4.4		5.25	V	
VDD3P0_OUT	2.9	3.0	3.1	V	Regulator output at default setting
I_out	-		50	mA	500 mV drop-out voltage
Regulator output programming range	2.625		3.4	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.75	2.85		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

NOTE

These values are with Anadig_REG_3P0[ENABLE_ILIMIT]= 0 and Anadig_REG_3P0[ENABLE_LINREG]= 1. It is required to set these values before using USB.

6.2.4 Power consumption operating behaviors

Table 15. Power consumption operating behaviors

Symbol	Description	Typ.[1]	Max.[2]	Unit	Notes
I_{DD_RUN}	Run mode current — All functionalities of the chip available	400	850	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.3 V ± 10%	80	500	mA	3
I_{DD_LPRUN}	Low-power run mode current at 3.3 V ± 10%, 24MHz operation, PLL Bypass.	13	325	mA	4
I_{DD_ULPRUN}	Ultra-low-power run mode current at 3.3 V ± 10%	12	395	mA	5
I_{DD_STOP}	Stop mode current at 3.3 V ± 10%	7	300	mA	6
I_{DD_LPS3}	Low-power stop3 mode current at 3.3 V ± 10%	300	1300	uA	7
I_{DD_LPS2}	Low-power stop 2 mode current at 3.3 V ± 10%	50	875	uA	8
I_{DD_VBAT}	Battery backup mode	5	45	uA	9

1. The Typ numbers represent the average value taken from a matrix lot of parts across normal process variation at ambient temperature.

2. The Max numbers represent the single worst case value taken from a matrix lot of parts across normal process variation at maximum temperature.
3. CA5, CM4 cores halted
4. 24MHz operation, PLL Bypass
5. 32 kHz /128 kHz operation, PLL Off
6. Lowest power mode with all power retained, RAM retention and LVD protection.
7. Standby Mode. 64K RAM retention. I/O states held. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts. Fast IRC enabled.
8. Standby Mode 16K RAM retention. I/O states held. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts. Fast IRC enabled.
9. All supplies OFF, SRTC, 32kXOSC ON, tampers and monitors ON. 128k IRC optionally ON.

6.2.5 USB PHY current consumption

6.2.5.1 Power Down Mode

Everything powered down, including the VBUS valid detectors, typ condition.

Table 16. USB PHY Current Consumption in Normal Mode

	USBx_VBUS (3.0V) Avg	VDD33_LDOIN (2.5V) Avg	VDD33_LDOIN (1.1V) Avg
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the 2.5 voltage regulator and 3.0 voltage regulator were identified to be the voltage divider circuits in the USB-specific level shifters.

6.2.6 EMC radiated emissions operating behaviors

Table 17. EMC radiated emissions operating behaviors

Symbol	Condition[1]	Clocks	Frequency band [2]	Level (Typ)[3]	Unit
V_{EME}	Device Configuration, test conditions and EM testing per standard IEC 61967-2; Supply voltages: VDD= 5.0 V VDD33 = 3.3 V VDD15 = 1.5 V VDD12 = 1.2 V Temp = 25°C	FCPU = 396 MHz FBUS = 66 MHz External Crystal = 24 MHz	150 KHz – 50 MHz	22	dBµV
			50 MHz – 150 MHz	24	
			150 MHz – 500 MHz	25	
			500–1000	20	
			IEC level[4]	K	—

1. Measurements were made per IEC 61967-2 while the device was running basic application code.
2. Measurements were performed on the BGA364 version of the device

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV

6.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

6.2.8 Capacitance attributes

Table 18. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

7 I/O parameters

7.1 GPIO parameters

Table 19. GPIO DC operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi[1]	Core internal supply voltage		1.2		V
ovdd	I/O output supply voltage	3	3.3	3.6	V

1. This is internally controlled.

Table 20. GPIO DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voh	High-level output voltage	Ioh= -1mA	ovdd-0.15			V

Table continues on the next page...

Table 20. GPIO DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
		VOH/VOL values are with respect to DSE=001[1]				
Vol	Low-level output voltage	Iol= 1mA			0.15	V
Vih [2]	High-Level DC input voltage		0.7*ovdd		ovdd	V
Vil[2]	Low-Level DC input voltage		0		0.3*ovdd	V
Vhys	Input Hysteresis	ovdd=3.3 V	250			mV
Vt+[2, 3]	Schmitt trigger VT+		0.5*ovdd			V
Vt-[2, 3]	Schmitt trigger VT-				0.5*ovdd	V
Iin[4]	Input current (no pull-up/down)	Vin = ovdd or 0	-1		1	uA
Iin_22pu	Input current (22KOhm PU)	Vin = 0			212	uA
		Vin = ovdd			1	
Iin_47pu	Input current (47KOhm PU)	Vin = 0			100	
		Vin = ovdd			1	
Iin_100pu	Input current (100KOhm PU)	Vin = 0			50	
		Vin = ovdd			1	
Iin_100pd	Input current (100KOhm PD)	Vin = 0			1	
		Vin = ovdd			50	
R_Keeper	Keeper Circuit Resistance	Vin = 0.3 x OVDD VI = 0.7 x OVDD	105		175	Ohm
Issod	Sink current in open drain mode	Vin = ovdd			7	mA
Issop	Sink/source current in Push Pull mode	Vin = ovdd			7	mA

1. For details about Software MUX Pad Control Register DSE bit, see IOMUX Controller chapter of the device reference manual.
2. To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1ns to 1s. Vil and Vih do not apply when hysteresis is enabled.
3. Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
4. Typ condition: typ model, 3.3V, and 25°C. Max condition: bcs model, 3.6V, and -40°C. Min condition: wcs model, 3.0V and 85 °C. These values are for digital IO buffer cells.

Table 21. GPIO AC Electrical Characteristics (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Slew rate	Test conditions	Min	Max	Unit
tpr	IO Output Transition Times (PA1), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	1.70	1.81	ns
			fast		1.04	1.18	
		High 1 0 1	slow		2.30	2.44	
			fast		1.69	1.79	
		Medium 1 0 0	slow		3.07	3.31	
			fast		2.45	2.61	
		Low 0 1 1	slow		5.13	5.44	
			fast		4.79	5.18	
tpo	IO Output Propagation Delay (PA2), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	5.01	5.04	ns
			fast		3.06	3.10	
		High 1 0 1	slow		5.55	5.68	
			fast		3.52	3.55	
		Medium 1 0 0	slow		6.37	6.67	
			fast		4.04	4.11	
		Low 0 1 1	slow		7.39	7.60	
			fast		5.54	6.10	
tpv	Output Enable to Output Valid Delay, rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps, 0->1, 1->0 pad transitions	5.12	5.21	ns
			fast		3.18	3.28	
		High 1 0 1	slow		5.72	5.80	
			fast		3.67	3.71	
		Medium 1 0 0	slow		6.55	6.80	
			fast		4.06	4.09	
		Low 0 1 1	slow		7.80	8.19	
			fast		5.72	6.22	
tpi	Input Pad Propagation Delay rise/fall	without hysteresis	-	150f Cload on, input edge rate from pad =1.2ns	1.06	1.31	ns
		with hysteresis	-		1.22	1.41	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.1.1 Output Buffer Impedance measurement

Table 22. Output Buffer Average Impedance (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
Rdrv	Output driver impedance	0 0 1	116	150	220	Ohm
		0 1 0	58	75	110	
		0 1 1	39	50	73	

Table continues on the next page...

Table 22. Output Buffer Average Impedance (3.3V power mode) (continued)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
		1 0 0	30	37	58	
		1 0 1	24	30	46	
		1 1 0 Extra drive strength	20	25	38	
		1 1 1	17	20	32	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.2 DDR parameters

Table 23. DDR operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi	Core internal supply voltage	1.16	1.23	1.26	V
ovdd	I/O output supply voltage (DDR3 mode)	1.425	1.5	1.575	V
ovdd	I/O output supply voltage (LPDDR2 mode)	1.14	1.2	1.26	V
vdd2p5	I/O PD predriver and level shifters supply voltage	2.25	2.5	2.75	V

Table 24. LPDDR2 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.9*ovdd			V	Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.
Vol	Low-level output voltage				0.1*ovdd	V	
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	
Vih(dc)	DC input high voltage		Vref+0.13		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.13	V	
Vih(diff)	DC differential input logic high		0.26		Note[1]	V	
Vil(diff)	DC differential input logic low		Note[1]		-0.26	V	

Table continues on the next page...