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Data Sheet, DS3, Jan. 2003

IWE8

Interworking Element for 8 E1/T1 Lines

PXB 4219E, PXB 4220E, PXB 4221E, Version 3.4

Wired Communications

Infineon technologies

Never stop thinking.

Data Sheet

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1 Overview

The Interworking Element for
8 E1/T1 Lines PXB 4219E, PXB 4220E, PXB 4221E (IWE8) is a member of Infineon's ATM chip set. Together with framing and line interface components (e.g. Infineon's QuadFALC PEB 22554) the IWE8 serves as gateway between Asynchronous Transfer Mode (ATM) networks and timeslot based PDH networks.

Each of the 8 E1 or T1 input and output ports can be configured independently to operate in one of two basic modes:

ATM Mode

ATM mode ports operate as an ATM User Network Interface (UNI) at 2.048 Mbit/s (E1) or 1.544 Mbit/s (T1).

The device supports mapping of ATM cells in T1/E1 frames according to ITU-T G.804, "ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)" [26] and ATM Forum, "ATM on Fractional E1/T1" [9].

It implements all Transmission Convergence (TC) sublayer functions of the Physical Layer (PHY) defined in ITU-T I.432, "B-ISDN User-network Interface - Physical layer Specification" [32]

AAL Mode

AAL mode ports operate as an ATM Circuit Emulation Service Interworking Function (CES-IWF) between Constant Bit Rate (CBR) equipment and an ATM network as described by the ATM Forum, "Circuit Emulation Services Version 2.0" [10]. (only PXB 4220/4221)

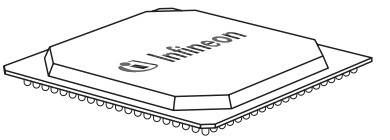
The CBR circuits are converted into ATM constant bit-rate virtual channels using the ATM Adaptation Layer type 1 (AAL1) as defined in I.363.1, "B-ISDN ATM Adaptation Layer Specification, Types 1 and 2" [31] or without any ATM Adaptation Layer overhead, which will be referred as AAL type 0 throughout the rest of this document.

The IWE8 provides the segmentation and reassembly function.

Both the "Unstructured DS1/E1 Service" and the "Structured DS1/E1 N x 64 kbit/s Basic Service" as described in the "Circuit Emulation Services Version 2.0" by the ATM Forum in [10] are supported. For simplicity reasons the shorthand notation "Unstructured CES" will be used to identify the "Unstructured DS1/E1 Service" while the "Structured DS1/E1 N x 64 kbit/s Service" will be referred to as "Structured CES" throughout the rest of this document.

Version 3.4

1.1 Features



P-BGA-256-2

- Full duplex ATM Packetizer/Depacketizer for 8 E1/T1 highways
- Configurable to T1 or E1 mode via external pin
- 8 T1/E1 ports configurable independently to ATM or AAL Mode
- ATM Mode (PXB 4219/4220/4221):
  - ATM cell mapping into PDH according to ITU-T G.804 [26]
  - B-ISDN User-Network interface - Physical Layer according to ITU-T I.432 [32]
  - B-ISDN User-Network interface - Physical Layer operation at 1544 KBit/s and 2048 KBit/s according to ITU-T I.432.3 [34]
- AAL Mode (PXB 4220/4221):
  - AAL1 according to ITU-T I.363.1 [31] or transparent without any adaptation layer overhead (AAL0)
  - T1/E1 unstructured service according to ATM Forum af-vtoa-0078.000 [10] section 3
  - Structured T1/E1 N x 64 kbit/s service according to [10] section 2 with M channels of N x 64 kbit/s (M,N = 1to 24 for T1) (M,N = 1to 32 for E1)
  - Channel Associated Signalling (CAS) support according to [10]
  - Echo Canceller Mode
  - Partially filled cells with programmable filling thresholds
  - Selectable Sequence Count Algorithm:
    - Robust/Fast according to ITU-T I.363.1 [30]
    - According to ETSI (prl-ETS 300353 annex D) [17]
    - Fast: Saves 6 ms during reassembly for 1 x 64 kbit/s connection
  - AAL0 option: 48 Bytes user payload per ATM Cell, without AAL overhead
  - Reassembly buffer can compensate up to +/- 4 ms Cell Delay Variation (CDV)
  - Statistics counters per channel for lost/misinserted/errored cells etc.

Type	Package
PXB 4219E, PXB 4220E, PXB 4221E	P-BGA-256

  - Internal clock recovery circuit using Synchronous Residual Time Stamp (SRTS, for fully filled cells only) or Adaptive Clock Method (ACM) for unstructured CES ports. For SRTS a patent fee needs to be paid. Optionally, it's possible to order the PXB 4221 device, which comes without SRTS clock recovery.
  - Trunk freezing and conditioning according to Bellcore TR-NWT-000170 [14]
- IMA interface:
  - Programmable threshold between read and write pointer of Mapping Buffer
  - Output Signal for buffer threshold crossing
  - Output Signal for discarded cell
  - Output pins for port number indication
- 8 generic framer interfaces with integrated transmit clock selector supporting
  - Synchronous Mode (SYM) for E1
  - Generic Interface Mode (GIM)
  - FALC Mode (FAM): Glue-less interface for Infineon's Framer and Line Interface Components (FALC)
  - Echo Canceller Mode (EC): ATM cells are duplicated internally and transmitted via two framer ports
- UTOPIA industry standard interface:
  - Level 2 in slave mode; 8 data, 5 address lines
  - Level 1 in master/slave mode
  - UTOPIA clock up to 38.88 MHz
- 16-bit generic microprocessor interface for control and configuration of the chip runs either in Intel 386EX or Motorola compatible mode
- External synchronous Flow-Through SSRAM 1 x 64k x 33 bit or 1 x 64k x 32 bit required
- Build-in data path loops for test
- Cell insertion/extraction via microprocessor interface
- 3.3 Volt power supply with 5 Volt tolerant inputs
- Typical power dissipation 1 Watt
- P-BGA-256 package
- Temperature range from -40° to +85°C

1.2 Logic Symbol

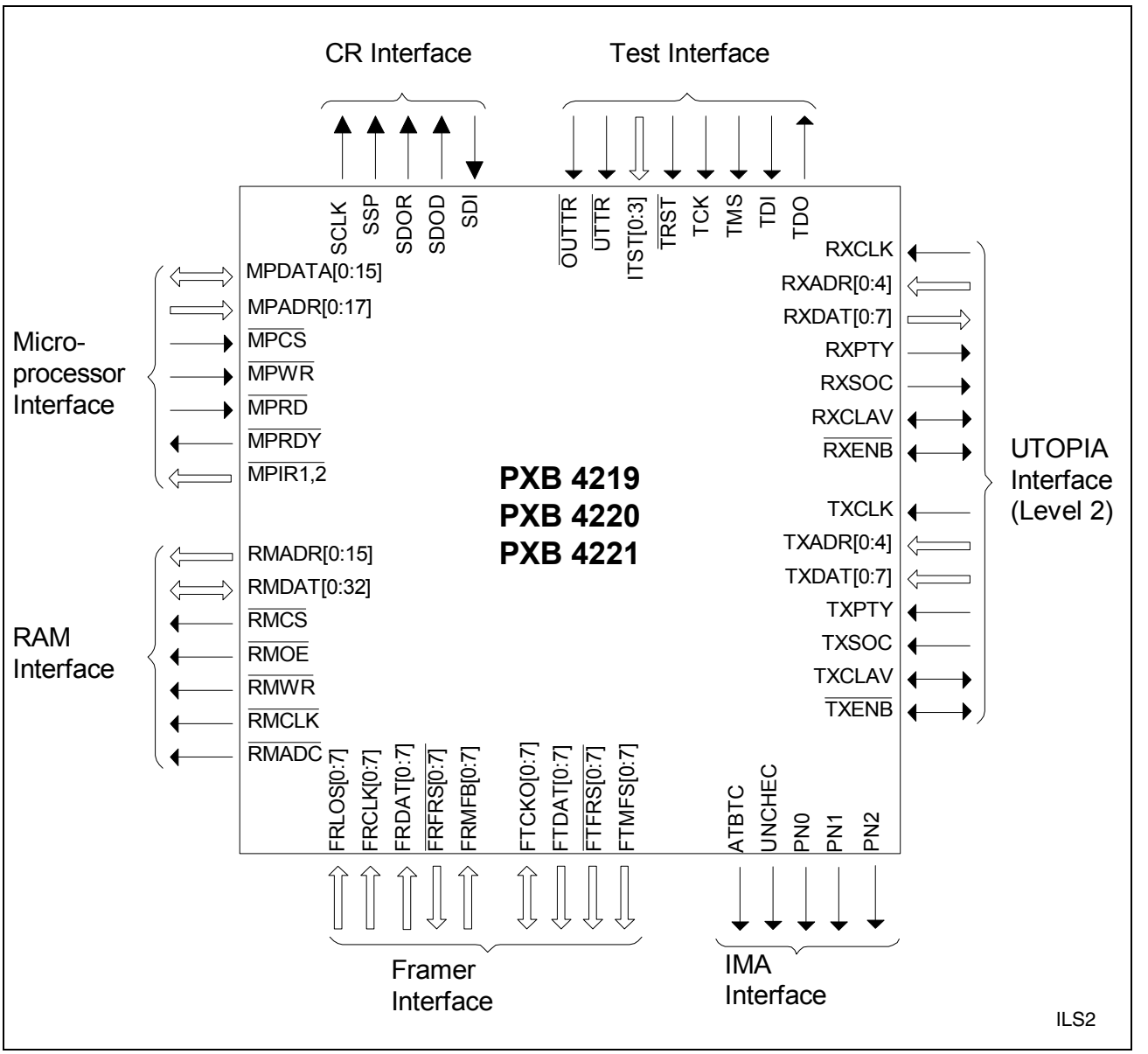


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 illustrates three typical application areas which utilize the IWE8 chip in Line Interface Cards (LICs) or Network Interface Controllers (NICs).

Application 1 utilizes the IWE8 as an internetworking device for communication between a narrowband Time-Slot based network and an ATM network.

Application 2 utilizes the IWE8 chip to enable the use of an existing T1/E1 access line for connection to an ATM network.

In application 3, the IWE8 chip enables terminals using a Leased Line or Time-Slot based service to convert from T1/E1 network connection to ATM network connection without noticeable changes to the subscriber.

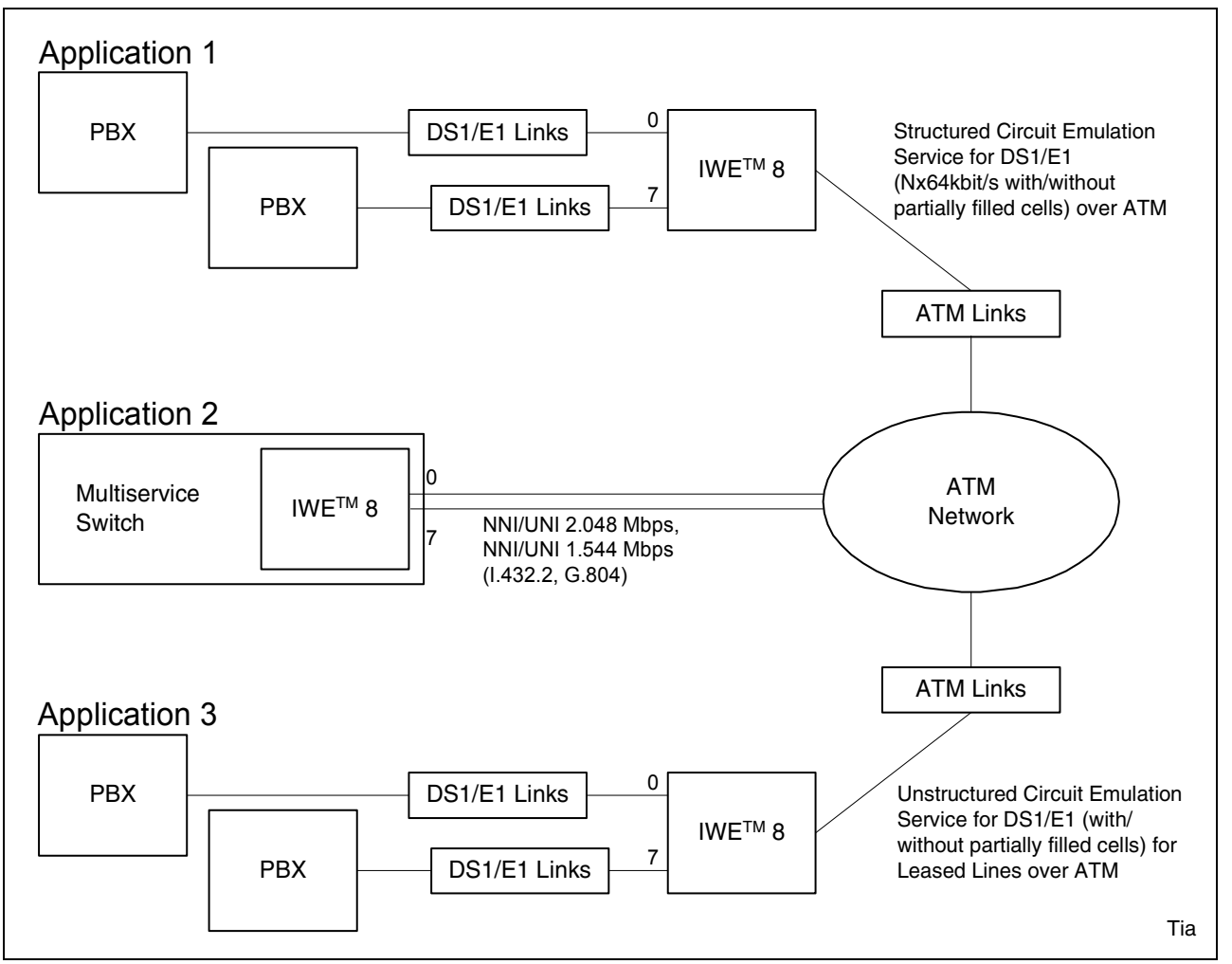


Figure 2 Typical IWE8 Applications

The PXB 4220 IWE8 chip is designed to handle up to eight T1/E1 ports. It transfers data between the Pulse Code Modulation (PCM)-highway and an UTOPIA ATM Interface.

1.3.1 Line Card

Figure 3 shows an example Line Interface Card (LIC) utilizing the IWE8 in a switch environment. Two Infineon Quad Framer and Line Interface Component (QuadFALC, PEB 22554) chips are connected at the PCM ports. An ATM Layer circuit is connected at the UTOPIA Interface port and could be implemented using Infineon PXB 4350 ATM Layer Processor (ALP) chip.

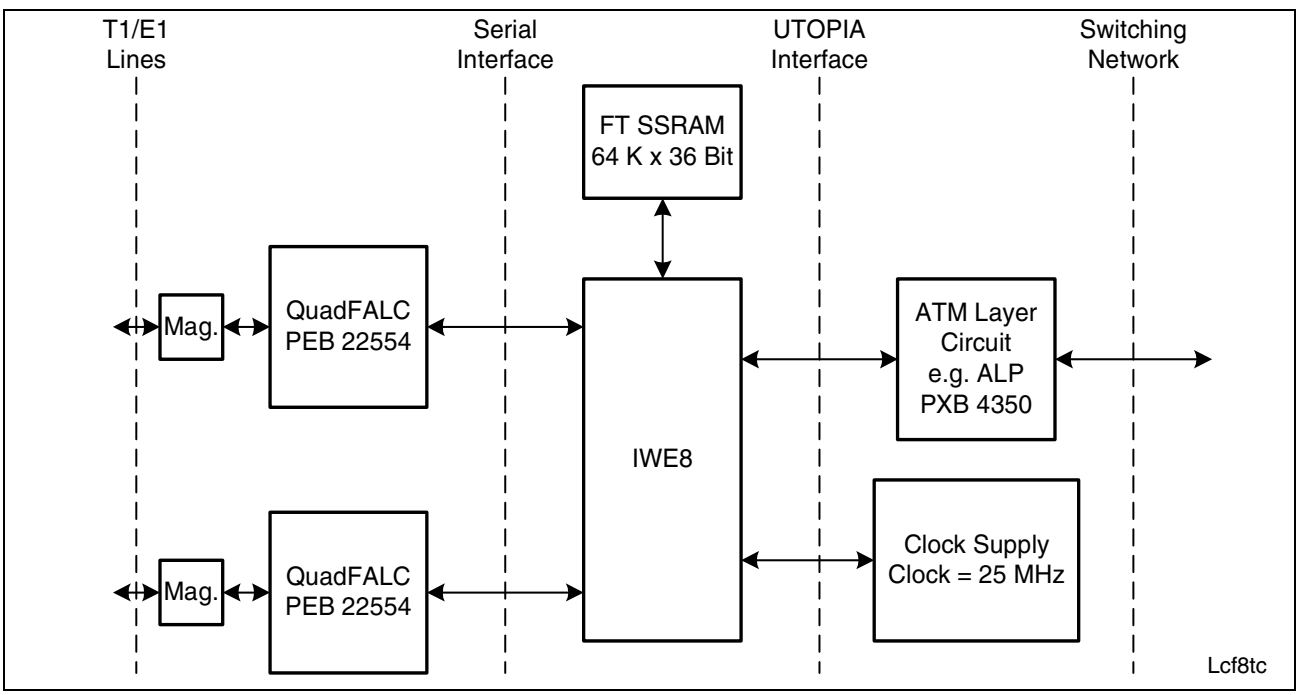


Figure 3 Line Card for 8 T1/E1 Channels

External synchronous SRAM is always required for proper IWE8 operation. The IWE8 requires only one main operating clock of 12 times the data rate of one port. An emergency clock of 32.768 MHz is optional. The Framer and Utopia interface clocks can be completely asynchronous with respect to the main clock. A microprocessor controls and operates the IWE8 via a generic 16-bit interface.

1.3.2 Echo Canceller

In communication links reflections resulting in an electrical echo are due to hybrid splits or imperfect terminations in subscriber loops. Acoustical echoes may occur due to poor isolation of microphone and speaker of some telephone systems. These electrical and acoustical echoes disturb the quality of the transmission. To ensure high quality, pure data transmission the ITU-T suggests in the recommendation G.131 [22] the use of echo cancellers. Echo cancellation is extremely desirable for data links with total round trip transmission times of more than 50 ms.

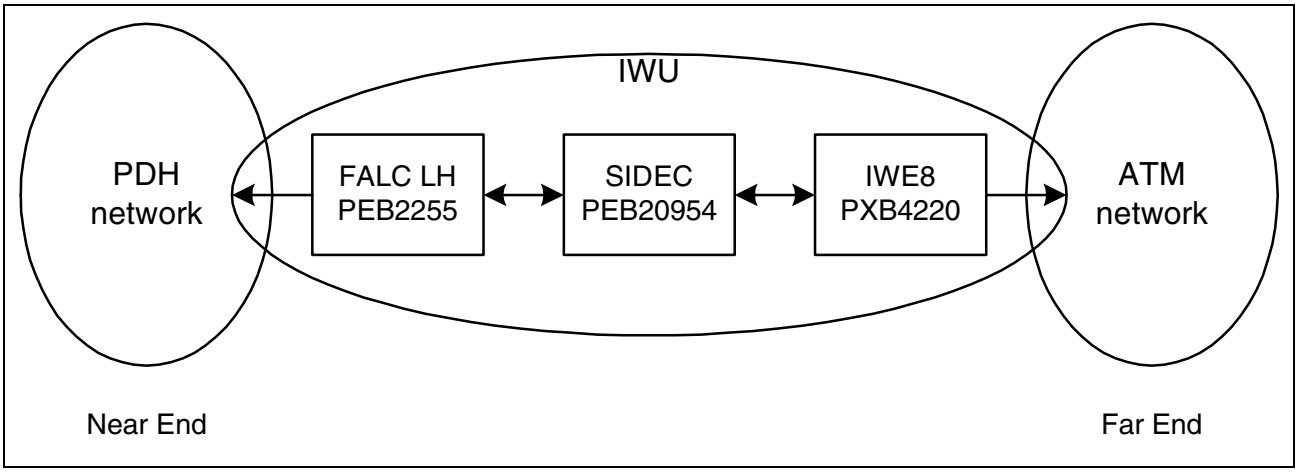


Figure 4 Echo Canceller Application

The echo cancelling function itself is performed in STM. In the application above the IWE8 is used to translate voice ATM channels into STM channels and vice versa. Infineon's Smart Integrated Digital Echo Canceller (SIDEC, PEB 20954) is used for cancellation of the echo that is generated by reflection on the near end side and heard by the far end speaker. The SIDEC can cancel end echo paths (SDH or PDH network on near end side) up to 128 ms. For details see [21]

1.4 Differences Between PXB4220 And PXB4219

The IWE8 type PXB 4219 does only support the ATM mode used for ITU-T G.804 compliant ATM cell mapping into the plesiochronous digital hierarchy (PDH) at line rates of 1544 kbit/s and 2048 kbit/s. The AAL mode is not available.

1.5 Differences Between PXB4220 And PXB4221

The IWE8 type PXB 4220 uses an internal clock recovery mechanism (SRTS) which is patented by Bellcore. SRTS is supported for fully filled cells only.

Related Patents are:

- Bellcore patent No. 5,260,978
  (Synchronous Residual Time Stamp for Timing Recovery in a broadband network)
- Bellcore patent No. 4,839,306
  (Method and apparatus for multiplexing circuit and packet traffic)

Infineon Technologies is not allowed to collect SRTS license fees on the IWE8 on behalf of Bellcore. Contacts for license issues are given in **Chapter 13**.

Every IWE8 customer must get in contact with Bellcore legal department by himself to clarify whether his application needs to license the SRTS functionality.

For customers who do not want to use the built-in SRTS mechanism, Infineon provides a special version of the IWE8. The name of this device is PXB 4221 and covers the same functionality (pin and register compatible) like the PXB 4220. SRTS is physically and permanently disabled, so that no patent fees have to be paid.

2 Pin Descriptions

2.1 Pin Diagram

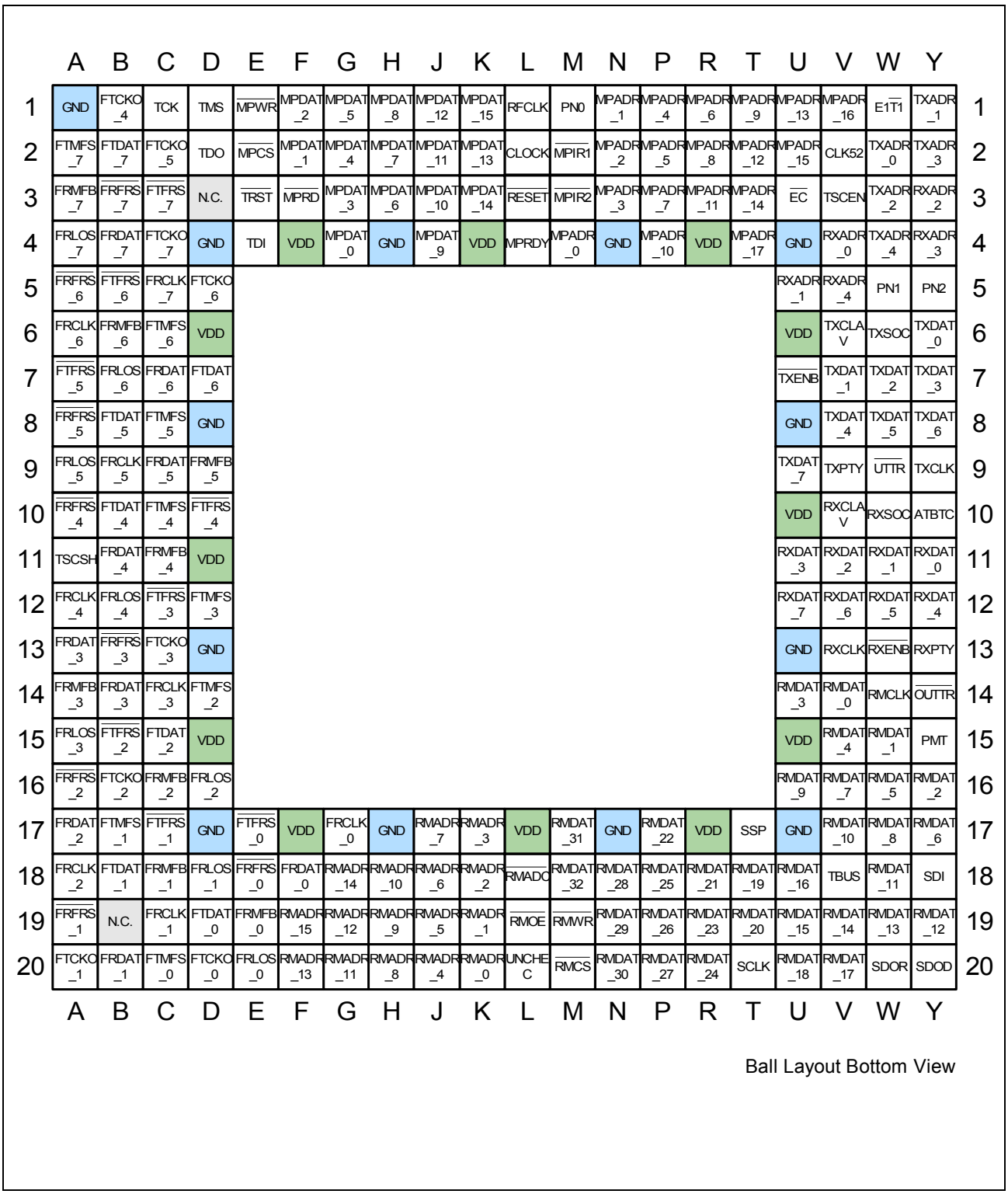


Figure 5 Pin Configuration

2.2 Pin Definitions and Functions

Output Pull Up and Pull Down Type Definitions

PUx	Pull Up of strength x (x = A, B) is implemented. The corresponding current is specified in **Chapter 9.4**
PDx	Pull Down of strength x (x = A) is implemented. The corresponding current is specified in **Chapter 9.4**
Tri	Tri-stated when inactive

2.2.1 Generic Framer Interface

Table 1 Generic Framer Interface (73 pins)

Pin No.	Symbol	Input (I) Output (O)	Function
C5, A6, B9, A12, C14, A18, C19, G17	FRCLK[7:0]	I	**Framer Receive Clock** Receive clock for the framer interface
B4, C7, C9, B11, B14, A17, B20, F18	FRDAT[7:0]	I PDA	**Framer Receive Data** Receive data input of the framer interface
A3, B6, D9, C11, A14, C16, C18, E19	FRMFB[7:0]	I PUA	**Framer Receive Multiframe Begin** Indication that a new multi-/superframe is available on the receive side of the framer interface
B3, A5, A8, A10, B13, A16, A19, E18	$\overline{\text{FRFRS}}$[7:0]	O PUA	**Framer Receive Frame Synchronization Pulse** Indication that a new frame is available on the receive side of the framer interface
A4,B7, A9, B12, A15, D16, D18, E20	FRLOS[7:0]	I PDA	**Framer Receive Loss of Signalling** Indication that CAS bits are invalid, IWE8 will start CAS freezing

Table 1 Generic Framer Interface (73 pins) (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
C4, D5, C2, B1, C13, B16, A20, D20	FTCKO[7:0]	O/I PDA	**Framer Transmit Clock** Transmit clock for the framer interface. • Recovered clock output from the ICRC • Framer receive clock output from pin FRCLKN • Output of the clock derived from RFCLK • Input for an external clock recovery device
B2, D7, B8, B10, A13, C15, B18, D19	FTDAT[7:0]	O PUA	**Framer Transmit Data** Transmit data output of the framer interface
A2, C6, C8, C10, D12, D14, B17, C20	FTMFS[7:0]	O PUA	**Framer Transmit Multiframe Synchronization** Indication that a new multi-/superframe is available on the transmit side of the framer interface
C3, B5, A7, D10, C12, B15, C17, E17	$\overline{\text{FTFRS}}$[7:0]	O PUA	**Framer Transmit Frame Synchronization Pulse** Indication that a new frame is available on the transmit side of the framer interface
L1	RFCLK	I	**Reference Clock** SYM and EC mode: Central framer interface clock for all framer ports FAM and GIM: Optional SRTS/ACM reference or emergency clock for the framer receive interface in case of clock failure

2.2.2 UTOPIA Interface

Table 2 UTOPIA Interface (36 pins)

Pin No.	Symbol	Input (I) Output (O)	Function
U12, V12, W12, Y12, U11, V11, W11, Y11	RXDAT[7:0]	O PUA	**UTOPIA Receive Data Bus** Byte-wide data driven from PHY to ATM layer. RxData[7] is the MSB.
Y13	RXPTY	O PUA	**UTOPIA Receive Odd Parity Bit** Odd parity for RXDAT[0:7] driven by the PHY layer.
W10	RXSOC	O PDA	**UTOPIA Receive Start-of-Cell** Active high signal asserted by the PHY layer when RXDAT[0:7] contains the first valid byte of a cell.
V10	RXCLAV	**Slave**: O **Master**: I PDA	**UTOPIA Receive Cell Available** **Slave**: RXCLAV is an active high signal asserted by the PHY layer to indicate that it has data available for transfer to the ATM layer. **Master**: RXCLAV is an active high signal asserted by the ATM layer to indicate that it has data available for transfer to the PHY layer.
V13	RXCLK	I	**UTOPIA Receive Clock** Transfer/synchronization clock from the ATM layer to the PHY layer for synchronizing transfers on RXDAT[0:7].
W13	$\overline{\text{RXENB}}$	**Slave**: I **Master**: O PUA	**UTOPIA Receive Enable** **Slave:** Active low signal asserted by the ATM layer to indicate that RXDAT[0:7] and RXSOC will be sampled at the end of the next cycle. **Master:** Active low signal asserted by the PHY layer to indicate that RXDAT[0:7] and RXSOC will be sampled at the end of the next cycle.