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IWE8

Interworking Element for
8 E1/T1 Lines

PXB 4219E, PXB 4220E, PXB
4221E, Version 3.4

Wired
Communications



Never stop thinking.

Data Sheet

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DS3

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Table of Contents	Page
1 Overview	14
1.1 Features	15
1.2 Logic Symbol	17
1.3 Typical Applications	18
1.3.1 Line Card	19
1.3.2 Echo Cancellor	19
1.4 Differences Between PXB4220 And PXB4219	21
1.5 Differences Between PXB4220 And PXB4221	21
2 Pin Descriptions	22
2.1 Pin Diagram	22
2.2 Pin Definitions and Functions	23
2.2.1 Generic Framer Interface	23
2.2.2 UTOPIA Interface	25
2.2.3 IMA Interface	27
2.2.4 Clock Recovery Interface	28
2.2.5 Microprocessor Interface	28
2.2.6 External RAM Interface	30
2.2.7 Test Interface	31
2.2.8 Miscellaneous	32
2.2.9 Power Supply	33
2.2.10 Not Connected Pins	33
3 Functional Description	34
3.1 Operating Modes	35
3.1.1 ATM Mode	35
3.1.2 AAL Mode	35
3.1.2.1 Unstructured CES Mode	35
3.1.2.2 Structured CES Mode	36
3.2 Functional Block Diagram	37
3.3 Functional Block Description	38
4 Operational Description	42
4.1 ATM Transmit Functions	42
4.1.1 Operation	42
4.1.1.1 ATM Transmit Buffer Filling Level	42
4.1.1.2 Cell Discarding	43
4.1.1.3 Cell rate de-coupling: Idle/Unassigned Cell Insertion	43
4.1.1.4 Cell Payload Scrambling	44
4.1.1.5 HEC Generation	44
4.1.2 Setup of ATM Transmit Ports	45
4.2 ATM Receive Functions	46
4.2.1 Operation	46
4.2.1.1 Cell Delineation	46

Table of Contents	Page
4.2.1.2 HEC Check: Header Error Detection and Correction	48
4.2.1.3 Cell Payload Descrambling	49
4.2.1.4 Idle, Physical Layer or Unassigned Cell Deletion	49
4.2.2 Setup of ATM Receive Ports	51
4.3 AAL Segmentation Functions	52
4.3.1 Operation	52
4.3.1.1 Segmentation Port Decorrelation	52
4.3.1.2 Segmentation	53
4.3.1.3 Transport of the Framing Port Number	53
4.3.1.4 Transport of CAS Information	54
4.3.1.5 CAS Conditioning and Freezing Upstream	54
4.3.1.6 Segmentation Buffer	55
4.3.1.7 Padding Partially Filled Cells	55
4.3.2 Setup of AAL Segmentation Channels	56
4.4 AAL Reassembly Functions	58
4.4.1 Operation	58
4.4.1.1 Port and Channel Identification	58
4.4.1.2 Sequence Number Protection field check	58
4.4.1.3 Sequence Number field check	59
4.4.1.4 RTS Extraction and Verification	59
4.4.1.5 Pointer Field Detection and Verification	59
4.4.1.6 CAS Conditioning and Freezing Downstream	60
4.4.1.7 Insertion of Dummy Cells at Cell Loss	60
4.4.1.8 Reassembly Buffer	60
4.4.1.9 Handling of Reassembly Buffer Overflow	61
4.4.1.10 Handling of Reassembly Buffer Underflow	61
4.4.1.11 Synchronization of SDT Structure with Port Structure	62
4.4.2 Setup	62
4.4.2.1 Setup of Reassembly Channels	62
4.4.2.2 Physical Reassembly Buffer Size	63
4.4.2.3 Initialization of the Reassembly Buffer	64
4.4.2.4 Re-Initialization of the Reassembly Buffer	69
4.5 Internal Clock Recovery Circuit (ICRC)	70
4.5.1 Data Flow	71
4.5.2 Frame Generator	71
4.5.3 Frame Receiver	72
4.5.4 RTS Receive FIFO	72
4.5.5 RTS Transmit FIFO	73
4.5.6 ICRC Loopback Modes	73
4.5.7 RTS Injection	73
4.5.8 Fractional Divider	74
4.5.9 Clocks	74

Table of Contents		Page
4.5.10	Power Management	74
4.5.11	PLL Block	74
4.5.11.1	PLL-SRTS:	74
4.5.11.2	PLL-FILTER	75
4.5.11.3	PLL-ACM	75
4.5.11.4	SRTS with ACM:	78
4.6	Internal Queues	79
4.6.1	Event Queue	79
4.6.2	Output Queue	79
4.6.3	Interrupt Queue	79
4.7	OAM Processing	80
4.8	Loopback Modes	81
4.8.1	Upstream Loop	81
4.8.2	Downstream Loop	81
4.8.3	Serial Loop	82
4.9	Cell Insertion	83
4.10	Cell Extraction	84
4.11	Mapping of Channels to Timeslots	85
4.11.1	ATM Mode	85
4.11.2	AAL Mode	86
4.11.2.1	Unstructured CES	86
4.11.2.2	Structured CES	87
4.11.2.3	Structured CES with CAS	88
5	Interface Description	91
5.1	Generic Framer Interface	91
5.1.1	FALC Mode (FAM)	91
5.1.1.1	T1 FALC Mode	94
5.1.1.2	E1 FALC Mode	95
5.1.2	Generic Interface Mode (GIM)	95
5.1.2.1	T1 Mode	95
5.1.2.2	E1 Mode	98
5.1.3	Synchronous Modes (SYM)	100
5.1.3.1	Synchronous Mode at 2.048 MHz (SYM2)	100
5.1.3.2	Synchronous Mode at 8.192 MHz (SYM8)	102
5.1.4	Echo Canceller Mode (EC)	103
5.2	UTOPIA Interface	105
5.2.1	Port Addresses	105
5.2.2	Back Pressure/ATM Cell Discarding	106
5.2.2.1	General Backpressure Mechanism	106
5.2.2.2	Port Specific Backpressure Mechanism	107
5.2.3	Sideband Signals of the UTOPIA Interface	107
5.3	IMA Interface	109

Table of Contents	Page
5.4	Clock Recovery Interface 110
5.5	Microprocessor Interface 112
5.5.1	Interrupt Handling 112
5.5.2	Microprocessor Interface Mode 113
5.6	External RAM Interface 115
5.7	Boundary Scan Interface 117
5.8	Master Clock 118
6	Memory Structure 119
6.1	Internal Configuration RAM's 120
6.1.1	RAM1: Receive Port Configuration 121
6.1.1.1	RAM1: ATM Receive Reference Slot 121
6.1.1.2	RAM1: ATM Receive Continuation Slot 122
6.1.1.3	RAM1: AAL Receive Reference Slot 123
6.1.1.4	RAM1: AAL Receive Continuation Slot 126
6.1.1.5	RAM1: ATM or AAL Receive Idle Slot 127
6.1.2	RAM2: Transmit Port Configuration 127
6.1.2.1	RAM2: ATM Transmit Reference Slot 127
6.1.2.2	RAM2: ATM Transmit Continuation Slot 128
6.1.2.3	RAM2: AAL Transmit Reference Slot 129
6.1.2.4	RAM2: AAL Transmit Continuation Slot 132
6.1.2.5	RAM2: ATM or AAL Transmit Idle Slot 133
6.1.3	RAM3: Transmit Port Configuration Extended 134
6.1.3.1	RAM3: AAL Transmit Reference Slot 134
6.1.4	RAM4: Transmit Port Configuration Extended 135
6.1.4.1	RAM4: AAL Transmit Conditioning Slot 136
6.2	External RAM 137
6.2.1	Statistics Counters 137
6.2.2	Statistics Counter thresholds 140
6.2.3	Interrupt Queue 141
6.2.4	Timers 142
6.2.5	Cell Insertion Buffer 143
6.2.6	Cell Extraction Buffer 144
6.2.7	Segmentation/ATM Receive Buffers 145
6.2.7.1	ATM Receive Buffer 146
6.2.7.2	Segmentation Buffer 146
6.2.8	Reassembly/ATM Transmit Buffers 146
7	Register Description 148
7.1	Port Configuration Registers (pcfN) 151
7.2	ASIC Configuration Register (acfg) 154
7.3	OAM Control Register (oamc) 156
7.4	OAM-Counter Enable Register for ATM Ports (catm) 157

Table of Contents	Page
7.5	OAM-Counter Enable Register for AAL Ports (caal) 158
7.6	Byte-Pattern Register bp3 and bp2 (bp32) 159
7.7	Byte-Pattern Register bp1 and bp0 (bp10) 160
7.8	ATM Control Register (atmc) 161
7.9	RX Idle/Unassigned Cell Control Register (rxid) 162
7.10	TX Idle/Unassigned Cell Control Register (txid) 163
7.11	Loopback Control Register (lpbc) 164
7.12	Cell Fill Register for Partially Filled Cells (cfil) 165
7.13	Interrupt Mask Register 1 (imr1) 166
7.14	Timer Enable Register (time) 167
7.15	Cell Delineation FSM Status Register (cdfs) 168
7.16	Version Register (vers) 169
7.17	Clock Monitor Register (ckmo) 170
7.18	Interrupt Status Register 1 (isr1) 171
7.19	Extended Interrupt Status 1 Register (eis1) 173
7.20	Extended Interrupt Status 2 Register (eis2) 174
7.21	Extended Interrupt Status 3 Register (eis3) 175
7.22	Extended Interrupt Status 4 Register (eis4) 176
7.23	Interrupt Status Register 2 (isr2) 177
7.24	Operation Mode Register (opmo) 178
7.25	FT Clock Select Register (ftcs) 180
7.26	Cell Filter VCI Pattern 1 Register (cfvp1) 181
7.27	Cell Filter VCI Mask 1 Register (cfvm1) 182
7.28	Cell Filter VCI Pattern 2 Register (cfvp2) 183
7.29	Cell Filter VCI Mask 2 Register (cfvm2) 184
7.30	Cell Filter Payload Type Register (cfpt) 185
7.31	Command Register (cmd) 186
7.32	Cell Filter Read Pointer Register (cfrp) 187
7.33	Threshold Register (thrshld) 188
7.34	UTOPIA Configuration Register (utconf) 189
7.35	CAS 1 Register (cas1) 191
7.36	CAS 2 Register (cas2) 192
7.37	CAS 3 Register (cas3) 193
7.38	Threshold Register for Ports 0 and 1 (thrsp01) 194
7.39	Threshold Register for Ports 2 and 3 (thrsp23) 195
7.40	Threshold Register for Ports 4 and 5 (thrsp45) 196
7.41	Threshold Register for Ports 6 and 7 (thrsp67) 197
7.42	Extended Interrupt Status 0 Register (eis0) 198
7.43	LCD Timer Register (lcdtimer) 199
7.44	Interrupt Source Register (irs) 200
7.45	Interrupt Mask (irm) 201
7.46	Internal Clock Recovery Circuit Configuration Register (icrcconf) 202

Table of Contents	Page	
7.47	Configuration Register Downstream of Port N (condN)	204
7.48	Interrupt Source of Port N (irsN)	206
7.49	Interrupt Mask of Port N (irmN)	207
7.50	Test Input of Port N (tsinN)	208
7.51	Configuration Register Upstream Direction of Port N (conuN)	209
7.52	Average Buffer Filling of Port N (avbN)	210
7.53	ACM Shift Factor of Port N (asfN)	211
7.54	Time of Initial Free Run of Port N (tiniN)	212
7.55	Threshold Out of Lock Detection of Port N (tresh)	213
7.56	ICRC Parity Errors at Clock Recovery Interface (per)	214
7.57	ICRC Synchronization Errors at Clock Recovery Interface (scri)	215
7.58	ICRC Clock Recovery Interface FIFO Overflow (crifo)	216
7.59	ICRC Version Register (icrcv)	217
7.60	SRTS Receive FIFO Underflow of Port N (sruN)	218
7.61	SRTS Receive FIFO Overflow of Port N (sroN)	219
7.62	SRTS Generator Reset of Port N (srrN)	220
7.63	SRTS Invalid Value Processed of Port N (sriN)	221
7.64	ACM Data Too Late of Port N (atlN)	222
7.65	Out Of Lock Register of Port N (oolN)	223
7.66	Status Register of Port N (statN)	224
7.67	Test Output Register of Port N (tsoutN)	225
8	Application Hints	226
8.1	Clock Concept	226
8.2	Translating AAL Statistics Counters into the ATMF CES Version 2 MIB	228
8.3	Jitter Characteristics of the Internal Clock Recovery Circuit	230
8.3.1	ACM Jitter Tolerance in E1 Mode	230
8.3.2	ACM Jitter Tolerance in T1 Mode	231
8.3.3	SRTS Jitter Tolerance in E1 Mode	233
8.3.4	SRTS Jitter Tolerance in T1 Mode	234
8.3.5	ACM Jitter Transfer in E1 Mode	236
8.3.6	ACM Jitter Transfer in T1 Mode	237
8.3.7	SRTS Jitter Transfer in E1 Mode	239
8.3.8	SRTS Jitter Transfer in T1 Mode	240
9	Electrical Characteristics	242
9.1	Absolute Maximum Ratings	242
9.2	Operating Range	243
9.3	Thermal Package Characteristics	244
9.4	DC Characteristics	245
9.5	Capacitances	246
9.6	AC Characteristics	247
9.6.1	Clock and Reset Interface	247

Table of Contents	Page
9.6.2 Framer Interface	248
9.6.2.1 Framer Interface in FAM	248
9.6.2.2 Framer Interface in GIM	251
9.6.2.3 Framer Interface in SYM Mode	254
9.6.2.4 Framer Interface in EC Mode	256
9.6.3 UTOPIA Interface	256
9.6.4 IMA Interface	260
9.6.5 Clock Recovery Interface	261
9.6.6 Microprocessor Interface	262
9.6.6.1 Intel Mode	262
9.6.6.2 Motorola Mode	264
9.6.7 RAM Interface	265
9.6.8 Boundary-Scan Test Interface	267
10 Testmode	268
10.1 Device Identification Register	268
10.2 Instruction Register	268
10.3 Boundary-Scan Register	268
11 Package Outlines	273
12 Appendix	274
12.1 ATM Adaptation Layer 1	274
12.2 Synchronous Residual Time Stamp SRTS	278
12.3 Adaptive Clock Method ACM	280
12.4 Channel Associated Signalling	281
12.4.1 E1	281
12.4.2 DS1	282
13 Contacts for SRTS Patent Fee	284
14 Glossary	285
15 Bibliography	288

List of Figures	Page
Figure 1	Logic Symbol 17
Figure 2	Typical IWE8 Applications 18
Figure 3	Line Card for 8 T1/E1 Channels 19
Figure 4	Echo Canceller Application 20
Figure 5	Pin Configuration 22
Figure 6	Block Diagram 37
Figure 7	Cell delineation state diagram (Figure 5/I.432.1) 47
Figure 8	Maintenance state transitions for cell delineation (Figure 2/ I.432.3) . . 47
Figure 9	HEC: Receiver mode of Operation (Figure 3/ITU I.432.1) 48
Figure 10	HEC Detection According to ATM Forum 49
Figure 11	Pre-assigned cell header values at the UNI (Table 1/I.361) 50
Figure 12	Pre-defined header field values [11] 50
Figure 13	SAR-PDU of AAL Type 0 53
Figure 14	Synchronization of SRTS Generation with the Start of Segmentation . 57
Figure 15	Reassembly Buffer Initialization: No CDV 64
Figure 16	Reassembly Buffer Initialization: positive CDV at Start Up 65
Figure 17	Reassembly Buffer Initialization: Negative CDV at Start Up 66
Figure 18	Reassembly Buffer Initialization for SDT: positive CDV at Start Up. . . 67
Figure 19	Block Diagram of the ICRC 71
Figure 20	Transient Parameters 76
Figure 21	Influence of Damping on Lock in Time. 77
Figure 22	Connection of IWE8 to QuadFALC 91
Figure 23	Framer Interface in FAM 94
Figure 24	Framer Interface in GIM T1 97
Figure 25	Framer Interface in GIM E1 99
Figure 26	Framer Interface in SYM2 E1 101
Figure 27	Framer Interface in SYM8 E1 103
Figure 28	Framer Interface in EC Mode. 104
Figure 29	UTOPIA Receive and Transmit Interfaces in Slave Mode 105
Figure 30	Utopia Sideband Signals 108
Figure 31	IMA Interface Protocol 109
Figure 32	Connection of IWE8 to an Intel Type Microprocessor 113
Figure 33	Connection of IWE8 to an Motorola Type Microprocessor 114
Figure 34	External RAM Connection 115
Figure 35	RAM Interface Protocol 116
Figure 36	Memory Model 119
Figure 37	Structure of the IWE8 external RAM 137
Figure 38	Clock Concept 226
Figure 39	ACM Jitter Tolerance in E1 Mode without Jitter Attenuator 230
Figure 40	ACM Jitter Tolerance in E1 Mode with Jitter Attenuator 231
Figure 41	ACM Jitter Tolerance in T1 Mode without Jitter Attenuator 232
Figure 42	ACM Jitter Tolerance in T1 Mode with Jitter Attenuator 232

List of Figures	Page
Figure 43	SRTS Jitter Tolerance in E1 Mode without Jitter Attenuator 233
Figure 44	SRTS Jitter Tolerance in E1 Mode with Jitter Attenuator. 234
Figure 45	SRTS Jitter Tolerance in T1 Mode without Jitter Attenuator 235
Figure 46	SRTS Jitter Tolerance in T1 Mode with Jitter Attenuator. 235
Figure 47	ACM Jitter Transfer in E1 Mode without Jitter Attenuator 236
Figure 48	ACM Jitter Transfer in E1 Mode with Jitter Attenuator. 237
Figure 49	ACM Jitter Transfer in T1 Mode without Jitter Attenuator 238
Figure 50	ACM Jitter Transfer in T1 Mode with Jitter Attenuator. 238
Figure 51	SRTS Jitter Transfer in E1 Mode without Jitter Attenuator 239
Figure 52	SRTS Jitter Transfer in E1 Mode with Jitter Attenuator 240
Figure 53	SRTS Jitter Transfer in T1 Mode without Jitter Attenuator 241
Figure 54	SRTS Jitter Transfer in T1 Mode with Jitter Attenuator 241
Figure 55	Input/Output Waveforms for AC Measurements 247
Figure 56	Clock and Reset Interface Timing Diagram 247
Figure 57	Framer Receive Interface Timing in FAM 248
Figure 58	Framer Transmit Interface Timing in FAM 250
Figure 59	Framer Receive Interface Timing in GIM 251
Figure 60	Framer Transmit Interface Timing in GIM 252
Figure 61	Framer Interface Timing for SYM 2.048 MHz 254
Figure 62	Framer Interface Timing in SYM 8.192 MHz 255
Figure 63	Framer Interface Timing in EC Mode. 256
Figure 64	Setup and hold time definition (single- and multi PHY) 257
Figure 65	Tri-state timing (multi-PHY, multiple devices only). 257
Figure 66	Timing of the IMA Interface 260
Figure 67	Clock Recovery Interface Timing Diagram 261
Figure 68	Intel Mode Write Cycle Timing Diagram 262
Figure 69	Intel Mode Read Cycle Timing Diagram 263
Figure 70	Motorola Mode Timing Diagram. 264
Figure 71	RAM Interface Timing Diagram 265
Figure 72	Boundary-Scan Test Interface Timing Diagram. 267
Figure 73	Package Outline: P-BGA-256 (Plastic Metric Quad Flat Package) 273
Figure 74	Structure of the AAL1 SAR-PDU 274
Figure 75	Informative and Example Algorithm State Machine (Fig. III.2/I.363.1) 276
Figure 76	The Concept of SRTS (Fig. 5/I.363.1) 278
Figure 77	Generation of Residual Time Stamp (RTS) (Fig.6/ I.363.1). 279
Figure 78	Example Multiframe Structure for 3x64 kbit/s E1 with CAS. 282
Figure 79	Example Multiframe Structure for 1x64 kbit/s DS1 with CAS. 283

List of Tables	Page
Table 1	Generic Framer Interface (73 pins) 23
Table 2	UTOPIA Interface (36 pins) 25
Table 3	IMA Interface 27
Table 4	Clock Recovery Interface 28
Table 5	Microprocessor Interface 28
Table 6	External RAM Interface 30
Table 7	Test Interface 31
Table 8	Miscellaneous 32
Table 9	Power Supply 33
Table 10	Not Connected Pins 33
Table 11	Functions of IWE8 Blocks 38
Table 12	ATM Cell Discarding 43
Table 13	Activation sequence for ATM transmit ports 45
Table 14	Activation sequence for ATM receive ports 51
Table 15	Definition of the CAS Signalling Conditioning Nibbles. 54
Table 16	Relationship betw. Cell Filling & Segmentation Buffer Subblock Size . 55
Table 17	Cell Filling level values. 56
Table 18	Activation sequence for AAL segmentation channels 56
Table 19	Activation sequence for AAL reassembly channels 63
Table 20	Relationship betw. Cell Filling and Reassembly Buffer Subblock Size 63
Table 21	Coding of Slot Type in internal configuration RAMs 85
Table 22	RAM slot positions for ITU-T G.804 compliant ATM mapping 85
Table 23	AAL Idle slot positions for structured CES in AAL mode 87
Table 24	AAL Idle slot positions for structured CES with CAS in AAL mode . . . 89
Table 25	Time slot Mapping in T1 Translation Mode 0 94
Table 26	F-Channel Format in T1 Mode 95
Table 27	Clock Recovery Interface frame format 110
Table 28	Configuration of the Microprocessor Interface Mode 113
Table 29	Master Clock Frequency Depending on Mode. 118
Table 30	Statistics Counters for ATM Ports 138
Table 31	Statistics Counters for AAL Ports. 138
Table 32	Internal Registers. 148
Table 33	Absolute Maximum Ratings 242
Table 34	Clock and Reset Interface AC Timing Characteristics 247
Table 35	Framer Receive Interface Timing in FAM 249
Table 36	Framer Transmit Interface Timing in FAM 250
Table 37	Framer Receive Interface Timing in GIM 251
Table 38	Framer Transmit Interface Timing in GIM 253
Table 39	Framer Interface AC Timing Characteristics in SYM2 Mode 254
Table 40	Framer Interface Timing in SYM8 255
Table 41	Framer Interface Timing in EC Mode. 256
Table 42	Transmit Timing (8-Bit Data Bus, 33 MHz, Single PHY) 258

List of Tables	Page
Table 43	Receive Timing (8-Bit Data Bus, 33 MHz, Single PHY) 258
Table 44	Transmit Timing (8-Bit Data Bus, 33 MHz, Multi-PHY) 259
Table 45	Receive Timing (8-Bit Data Bus, 33 MHz, Multi-PHY) 259
Table 46	IMA Interface AC Timing Characteristics 261
Table 47	Clock Recovery Interface AC Timing Characteristics 261
Table 48	Intel Mode Write Cycle AC Characteristics 262
Table 49	Intel Mode Read Cycle AC Timing Characteristics 263
Table 50	Motorola Mode AC Timing Characteristics 264
Table 51	RAM Interface AC Timing Characteristics 266
Table 52	Boundary-Scan Test Interface AC Timing Characteristics 267
Table 53	Boundary Scan Register 268
Table 54	Bit allocation of E1 time slot 16 for CAS 281
Table 55	Allocation of CAS Bits to 24 Frame Multiframe 283

1 Overview

The Interworking Element for

8 E1/T1 Lines PXB 4219E, PXB 4220E, PXB 4221E (IWE8) is a member of Infineon's ATM chip set. Together with framing and line interface components (e.g. Infineon's QuadFALC PEB 22554) the IWE8 serves as gateway between Asynchronous Transfer Mode (ATM) networks and timeslot based PDH networks.

Each of the 8 E1 or T1 input and output ports can be configured independently to operate in one of two basic modes:

ATM Mode

ATM mode ports operate as an ATM User Network Interface (UNI) at 2.048 Mbit/s (E1) or 1.544 Mbit/s (T1).

The device supports mapping of ATM cells in T1/E1 frames according to ITU-T G.804, "ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)" [26] and ATM Forum, "ATM on Fractional E1/T1" [9].

It implements all Transmission Convergence (TC) sublayer functions of the Physical Layer (PHY) defined in ITU-T I.432, "B-ISDN User-network Interface - Physical layer Specification" [32]

AAL Mode

AAL mode ports operate as an ATM Circuit Emulation Service Interworking Function (CES-IWF) between Constant Bit Rate (CBR) equipment and an ATM network as described by the ATM Forum, "Circuit Emulation Services Version 2.0" [10]. (only PXB 4220/4221)

The CBR circuits are converted into ATM constant bit-rate virtual channels using the ATM Adaptation Layer type 1 (AAL1) as defined in I.363.1, "B-ISDN ATM Adaptation Layer Specification, Types 1 and 2" [31] or without any ATM Adaptation Layer overhead, which will be referred as AAL type 0 throughout the rest of this document.

The IWE8 provides the segmentation and reassembly function.

Both the "Unstructured DS1/E1 Service" and the "Structured DS1/E1 N x 64 kbit/s Basic Service" as described in the "Circuit Emulation Services Version 2.0" by the ATM Forum in [10] are supported. For simplicity reasons the shorthand notation "Unstructured CES" will be used to identify the "Unstructured DS1/E1 Service" while the "Structured DS1/E1 N x 64 kbit/s Service" will be referred to as "Structured CES" throughout the rest of this document.

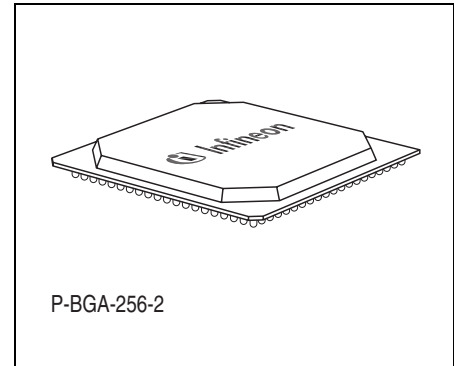
Interworking Element for 8 E1/T1 Lines IWE8

**PXB 4219E, PXB
4220E, PXB 4221E**

Version 3.4

1.1 Features

- Full duplex ATM Packetizer/Depacketizer for 8 E1/T1 highways
- Configurable to T1 or E1 mode via external pin
- 8 T1/E1 ports configurable independently to ATM or AAL Mode
- ATM Mode (PXB 4219/4220/4221):
 - ATM cell mapping into PDH according to ITU-T G.804 [26]
 - B-ISDN User-Network interface - Physical Layer according to ITU-T I.432 [32]
 - B-ISDN User-Network interface - Physical Layer operation at 1544 KBit/s and 2048 KBit/s according to ITU-T I.432.3 [34]
- AAL Mode (PXB 4220/4221):
 - AAL1 according to ITU-T I.363.1 [31] or transparent without any adaptation layer overhead (AAL0)
 - T1/E1 unstructured service according to ATM Forum af-vtoa-0078.000 [10] section 3
 - Structured T1/E1 N x 64 kbit/s service according to [10] section 2 with M channels of N x 64 kbit/s (M,N = 1 to 24 for T1) (M,N = 1 to 32 for E1)
 - Channel Associated Signalling (CAS) support according to [10]
 - Echo Canceller Mode
 - Partially filled cells with programmable filling thresholds
 - Selectable Sequence Count Algorithm:
 - Robust/Fast according to ITU-T I.363.1 [30]
 - According to ETSI (prl-ETS 300353 annex D) [17]
 - Fast: Saves 6 ms during reassembly for 1 x 64 kbit/s connection
 - AAL0 option: 48 Bytes user payload per ATM Cell, without AAL overhead
 - Reassembly buffer can compensate up to +/- 4 ms Cell Delay Variation (CDV)
 - Statistics counters per channel for lost/misinserted/errored cells etc.



Type	Package
PXB 4219E, PXB 4220E, PXB 4221E	P-BGA-256

- Internal clock recovery circuit using Synchronous Residual Time Stamp (SRTS, for fully filled cells only) or Adaptive Clock Method (ACM) for unstructured CES ports. For SRTS a patent fee needs to be paid. Optionally, it's possible to order the PXB 4221 device, which comes without SRTS clock recovery.
- Trunk freezing and conditioning according to Bellcore TR-NWT-000170 [14]
- IMA interface:
 - Programmable threshold between read and write pointer of Mapping Buffer
 - Output Signal for buffer threshold crossing
 - Output Signal for discarded cell
 - Output pins for port number indication
- 8 generic framer interfaces with integrated transmit clock selector supporting
 - Synchronous Mode (SYM) for E1
 - Generic Interface Mode (GIM)
 - FALC Mode (FAM): Glue-less interface for Infineon's Framer and Line Interface Components (FALC)
 - Echo Canceller Mode (EC): ATM cells are duplicated internally and transmitted via two framer ports
- UTOPIA industry standard interface:
 - Level 2 in slave mode; 8 data, 5 address lines
 - Level 1 in master/slave mode
 - UTOPIA clock up to 38.88 MHz
- 16-bit generic microprocessor interface for control and configuration of the chip runs either in Intel 386EX or Motorola compatible mode
- External synchronous Flow-Through SSRAM 1 x 64k x 33 bit or 1 x 64k x 32 bit required
- Build-in data path loops for test
- Cell insertion/extraction via microprocessor interface
- 3.3 Volt power supply with 5 Volt tolerant inputs
- Typical power dissipation 1 Watt
- P-BGA-256 package
- Temperature range from -40° to +85°C

1.2 Logic Symbol

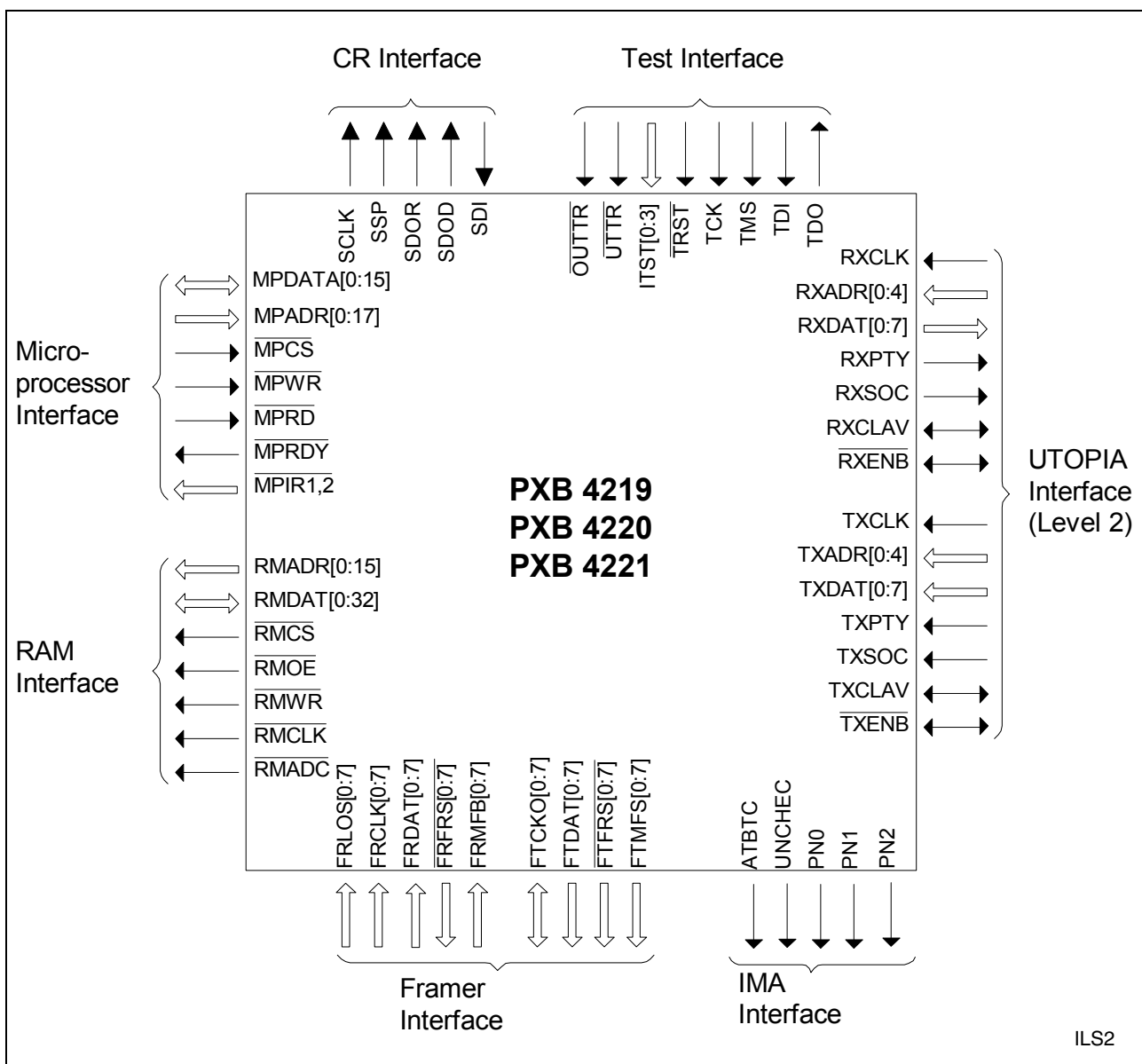


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 illustrates three typical application areas which utilize the IWE8 chip in Line Interface Cards (LICs) or Network Interface Controllers (NICs).

Application 1 utilizes the IWE8 as an internetworking device for communication between a narrowband Time-Slot based network and an ATM network.

Application 2 utilizes the IWE8 chip to enable the use of an existing T1/E1 access line for connection to an ATM network.

In application 3, the IWE8 chip enables terminals using a Leased Line or Time-Slot based service to convert from T1/E1 network connection to ATM network connection without noticeable changes to the subscriber.

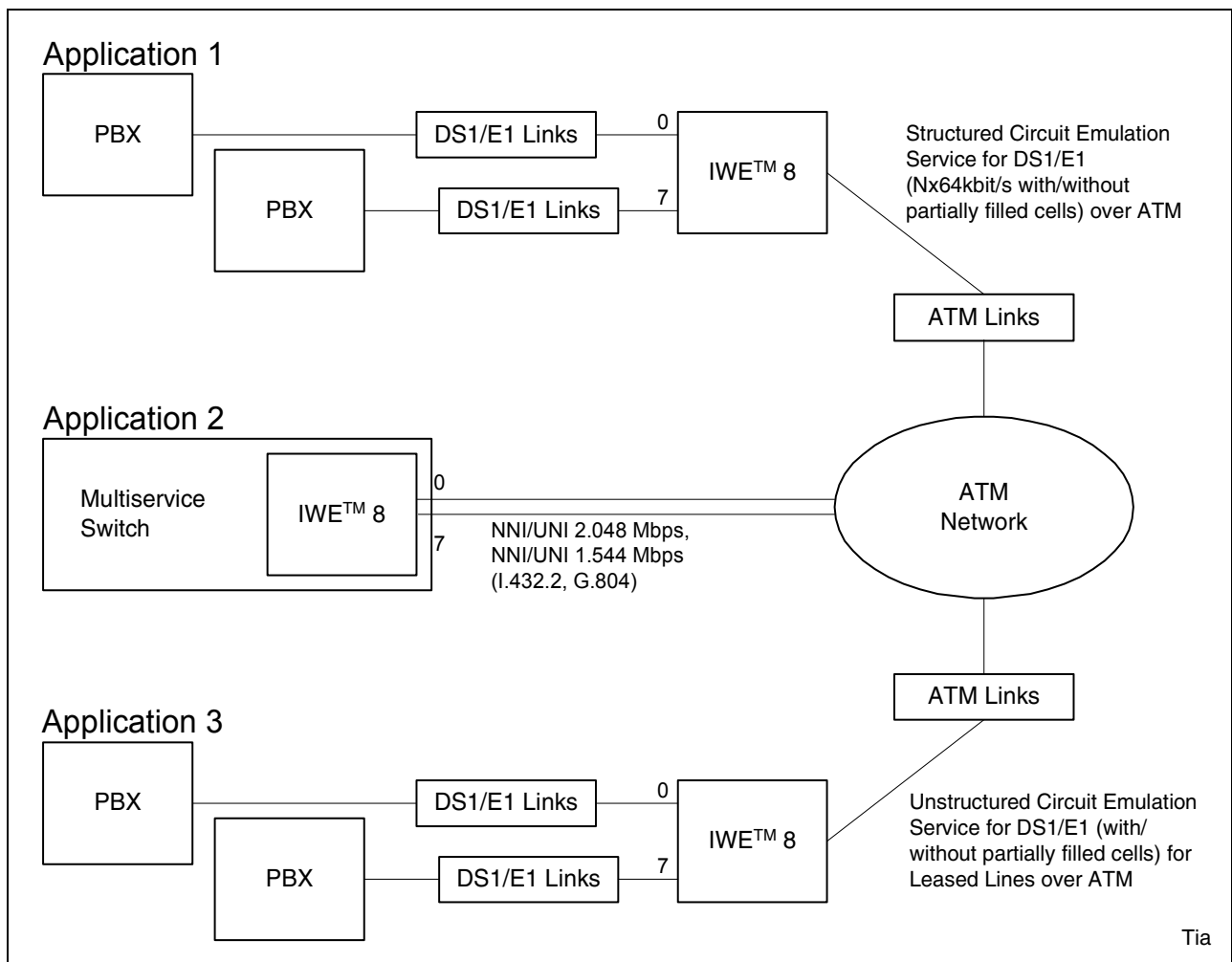


Figure 2 Typical IWE8 Applications

The PXB 4220 IWE8 chip is designed to handle up to eight T1/E1 ports. It transfers data between the Pulse Code Modulation (PCM)-highway and an UTOPIA ATM Interface.

1.3.1 Line Card

Figure 3 shows an example Line Interface Card (LIC) utilizing the IWE8 in a switch environment. Two Infineon Quad Framer and Line Interface Component (QuadFALC, PEB 22554) chips are connected at the PCM ports. An ATM Layer circuit is connected at the UTOPIA Interface port and could be implemented using Infineon PXB 4350 ATM Layer Processor (ALP) chip.

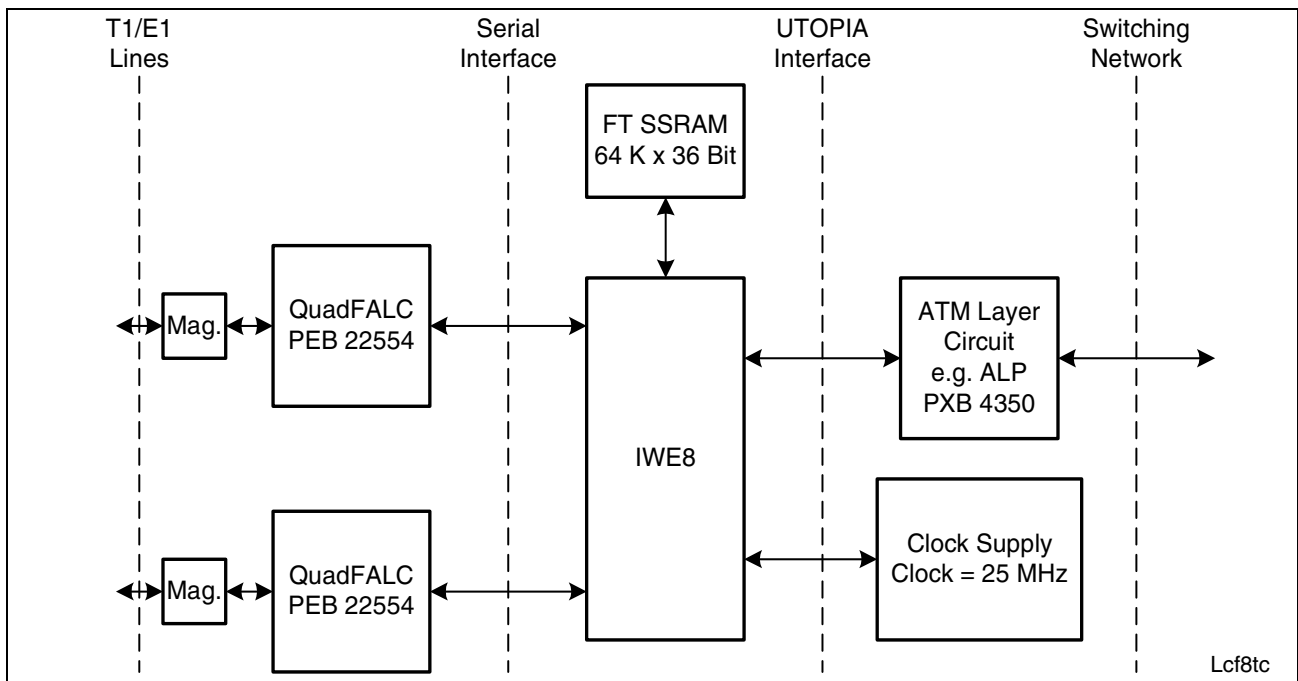


Figure 3 Line Card for 8 T1/E1 Channels

External synchronous SRAM is always required for proper IWE8 operation. The IWE8 requires only one main operating clock of 12 times the data rate of one port. An emergency clock of 32.768 MHz is optional. The Framer and Utopia interface clocks can be completely asynchronous with respect to the main clock. A microprocessor controls and operates the IWE8 via a generic 16-bit interface.

1.3.2 Echo Canceller

In communication links reflections resulting in an electrical echo are due to hybrid splits or imperfect terminations in subscriber loops. Acoustical echoes may occur due to poor isolation of microphone and speaker of some telephone systems. These electrical and acoustical echoes disturb the quality of the transmission. To ensure high quality, pure data transmission the ITU-T suggests in the recommendation G.131 [22] the use of echo cancellers. Echo cancellation is extremely desirable for data links with total round trip transmission times of more than 50 ms.

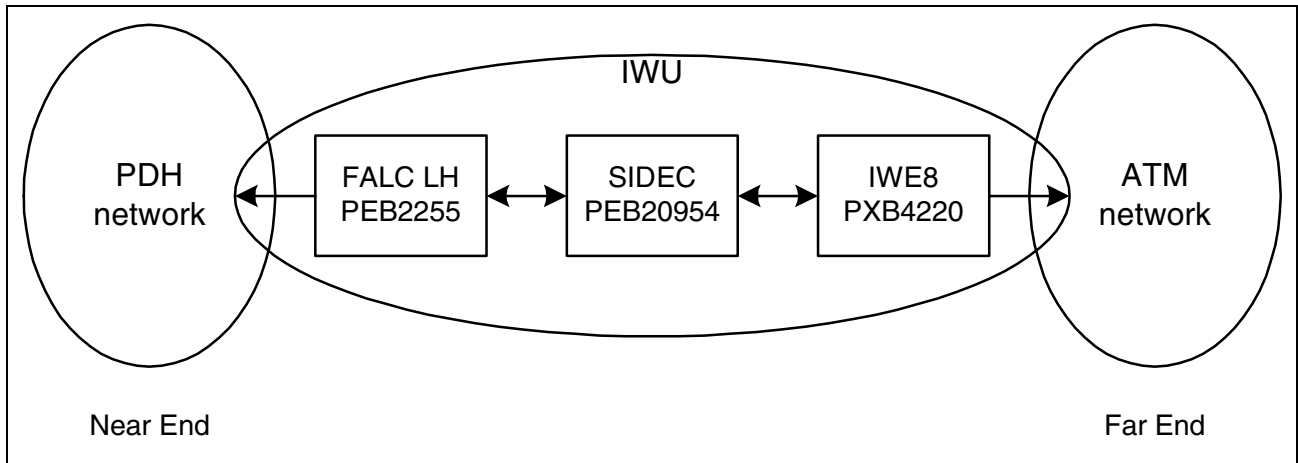


Figure 4 Echo Canceller Application

The echo cancelling function itself is performed in STM. In the application above the IWE8 is used to translate voice ATM channels into STM channels and vice versa. Infineon's Smart Integrated Digital Echo Canceller (SIDEC, PEB 20954) is used for cancellation of the echo that is generated by reflection on the near end side and heard by the far end speaker. The SIDEC can cancel end echo paths (SDH or PDH network on near end side) up to 128 ms. For details see [21]

1.4 Differences Between PXB4220 And PXB4219

The IWE8 type PXB 4219 does only support the ATM mode used for ITU-T G.804 compliant ATM cell mapping into the plesiochronous digital hierarchy (PDH) at line rates of 1544 kbit/s and 2048 kbit/s. The AAL mode is not available.

1.5 Differences Between PXB4220 And PXB4221

The IWE8 type PXB 4220 uses an internal clock recovery mechanism (SRTS) which is patented by Bellcore. SRTS is supported for fully filled cells only.

Related Patents are:

- Bellcore patent No. 5,260,978
(Synchronous Residual Time Stamp for Timing Recovery in a broadband network)
- Bellcore patent No. 4,839,306
(Method and apparatus for multiplexing circuit and packet traffic)

Infineon Technologies is not allowed to collect SRTS license fees on the IWE8 on behalf of Bellcore. Contacts for license issues are given in [Chapter 13](#).

Every IWE8 customer must get in contact with Bellcore legal department by himself to clarify whether his application needs to license the SRTS functionality.

For customers who do not want to use the built-in SRTS mechanism, Infineon provides a special version of the IWE8. The name of this device is PXB 4221 and covers the same functionality (pin and register compatible) like the PXB 4220. SRTS is physically and permanently disabled, so that no patent fees have to be paid.

2 Pin Descriptions

2.1 Pin Diagram

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y			
1	GND	FTCKO _4	TCK	TMS	MPWPR	MPDAT _2	MPDAT _5	MPDAT _8	MPDAT _12	MPDAT _15	RFCLK	PN0	MPADR _1	MPADR _4	MPADR _6	MPADR _9	MPADR _13	MPADR _16	E1T1	TXADR _1	1		
2	FTMFS _7	FTDAT _7	FTCKO _5	TDO	MPCS	MPDAT _1	MPDAT _4	MPDAT _7	MPDAT _11	MPDAT _13	CLOCK	MPIR1	MPADR _2	MPADR _5	MPADR _8	MPADR _12	MPADR _15	CLK52	TXADR _0	TXADR _3	2		
3	FRMFB _7	FRFRS _7	FTFRS _7	N.C.	TRST	MPRD	MPDAT _3	MPDAT _6	MPDAT _10	MPDAT _14	RESET	MPIR2	MPADR _3	MPADR _7	MPADR _11	MPADR _14	EC	TSCEN	TXADR _2	RXADR _2	3		
4	FRLOS _7	FRDAT _7	FTCKO _7	GND	TDI	VDD	MPDAT _0	GND	MPDAT _9	VDD	MPRDY	MPADR _0	GND	MPADR _10	VDD	MPADR _17	GND	RXADR _0	TXADR _4	RXADR _3	4		
5	FRFRS _6	FTFRS _6	FRCLK _7	FTCKO _6														RXADR _1	RXADR _4	PN1	PN2	5	
6	FRCLK _6	FRMFB _6	FTMFS _6	VDD														VDD	TXCLA V	TXSOC	TXDAT _0	6	
7	FTFRS _5	FRLOS _6	FRDAT _6	FTDAT _6															TXENB	TXDAT _1	TXDAT _2	TXDAT _3	7
8	FRFRS _5	FTDAT _5	FTMFS _5	GND															GND	TXDAT _4	TXDAT _5	TXDAT _6	8
9	FRLOS _5	FRCLK _5	FRDAT _5	FRMFB _5															TXDAT _7	TXPTY	UTTR	TXCLK	9
10	FRFRS _4	FTDAT _4	FTMFS _4	FTFRS _4															VDD	RXCLA V	RXSOC	ATBTC	10
11	TSCSH	FRDAT _4	FRMFB _4	VDD															RXDAT _3	RXDAT _2	RXDAT _1	RXDAT _0	11
12	FRCLK _4	FRLOS _4	FTFRS _3	FTMFS _3															RXDAT _7	RXDAT _6	RXDAT _5	RXDAT _4	12
13	FRDAT _3	FRFRS _3	FTCKO _3	GND															GND	RXCLK	RXENB	RXPTY	13
14	FRMFB _3	FRDAT _3	FRCLK _3	FTMFS _2															RMDAT _3	RMDAT _0	RMCLK	OUTTR	14
15	FRLOS _3	FTFRS _2	FTDAT _2	VDD															VDD	RMDAT _4	RMDAT _1	PMT	15
16	FRFRS _2	FTCKO _2	FRMFB _2	FRLOS _2															RMDAT _9	RMDAT _7	RMDAT _5	RMDAT _2	16
17	FRDAT _2	FTMFS _1	FTFRS _1	GND	FTFRS _0	VDD	FRCLK _0	GND	RMDAT _7	RMDAT _3	VDD	RMDAT _31	GND	RMDAT _22	VDD	SSP	GND	RMDAT _10	RMDAT _8	RMDAT _6		17	
18	FRCLK _2	FTDAT _1	FRMFB _1	FRLOS _1	FRFRS _0	FRDAT _0	RMDAT _14	RMDAT _10	RMDAT _6	RMDAT _2	RMDAT _0	RMDAT _32	RMDAT _28	RMDAT _25	RMDAT _21	RMDAT _19	RMDAT _16	TBUS	RMDAT _11	SDI		18	
19	FRFRS _1	N.C.	FRCLK _1	FTDAT _0	FRMFB _0	RMDAT _15	RMDAT _12	RMDAT _9	RMDAT _5	RMDAT _1	RMDAT _0	RMOC	RMDAT _29	RMDAT _26	RMDAT _23	RMDAT _20	RMDAT _15	RMDAT _14	RMDAT _13	RMDAT _12		19	
20	FTCKO _1	FRDAT _1	FTMFS _0	FTCKO _0	FRLOS _0	RMDAT _13	RMDAT _11	RMDAT _8	RMDAT _4	RMDAT _0	UNCHE C	RMCS	RMDAT _30	RMDAT _27	RMDAT _24	SCLK	RMDAT _18	RMDAT _17	SDOR	SDOD		20	

Ball Layout Bottom View

Figure 5 Pin Configuration

2.2 Pin Definitions and Functions

Output Pull Up and Pull Down Type Definitions

PUx	Pull Up of strength x (x = A, B) is implemented. The corresponding current is specified in Chapter 9.4
PDx	Pull Down of strength x (x = A) is implemented. The corresponding current is specified in Chapter 9.4
Tri	Tri-stated when inactive

2.2.1 Generic Framer Interface

Table 1 Generic Framer Interface (73 pins)

Pin No.	Symbol	Input (I) Output (O)	Function
C5, A6, B9, A12, C14, A18, C19, G17	FRCLK[7:0]	I	Framer Receive Clock Receive clock for the framer interface
B4, C7, C9, B11, B14, A17, B20, F18	FRDAT[7:0]	I PDA	Framer Receive Data Receive data input of the framer interface
A3, B6, D9, C11, A14, C16, C18, E19	FRMFB[7:0]	I PUA	Framer Receive Multiframe Begin Indication that a new multi-/superframe is available on the receive side of the framer interface
B3, A5, A8, A10, B13, A16, A19, E18	FRFRS[7:0]	O PUA	Framer Receive Frame Synchronization Pulse Indication that a new frame is available on the receive side of the framer interface
A4, B7, A9, B12, A15, D16, D18, E20	FRLOS[7:0]	I PDA	Framer Receive Loss of Signalling Indication that CAS bits are invalid, IWE8 will start CAS freezing

Pin Descriptions

Table 1 Generic Framer Interface (73 pins) (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
C4, D5, C2, B1, C13, B16, A20, D20	FTCKO[7:0]	O/I PDA	Framer Transmit Clock Transmit clock for the framer interface. <ul style="list-style-type: none"> Recovered clock output from the ICRC Framer receive clock output from pin FRCLKN Output of the clock derived from RFCLK Input for an external clock recovery device
B2, D7, B8, B10, A13, C15, B18, D19	FTDAT[7:0]	O PUA	Framer Transmit Data Transmit data output of the framer interface
A2, C6, C8, C10, D12, D14, B17, C20	FTMFS[7:0]	O PUA	Framer Transmit Multiframe Synchronization Indication that a new multi-/superframe is available on the transmit side of the framer interface
C3, B5, A7, D10, C12, B15, C17, E17	$\overline{\text{FTFRS}}[7:0]$	O PUA	Framer Transmit Frame Synchronization Pulse Indication that a new frame is available on the transmit side of the framer interface
L1	RFCLK	I	Reference Clock SYM and EC mode: Central framer interface clock for all framer ports FAM and GIM: Optional SRTS/ACM reference or emergency clock for the framer receive interface in case of clock failure

2.2.2 UTOPIA Interface

Table 2 UTOPIA Interface (36 pins)

Pin No.	Symbol	Input (I) Output (O)	Function
U12, V12, W12, Y12, U11, V11, W11, Y11	RXDAT[7:0]	O PUA	UTOPIA Receive Data Bus Byte-wide data driven from PHY to ATM layer. RxData[7] is the MSB.
Y13	RXPTY	O PUA	UTOPIA Receive Odd Parity Bit Odd parity for RXDAT[0:7] driven by the PHY layer.
W10	RXSOC	O PDA	UTOPIA Receive Start-of-Cell Active high signal asserted by the PHY layer when RXDAT[0:7] contains the first valid byte of a cell.
V10	RXCLAV	Slave: O Master: I PDA	UTOPIA Receive Cell Available Slave: RXCLAV is an active high signal asserted by the PHY layer to indicate that it has data available for transfer to the ATM layer. Master: RXCLAV is an active high signal asserted by the ATM layer to indicate that it has data available for transfer to the PHY layer.
V13	RXCLK	I	UTOPIA Receive Clock Transfer/synchronization clock from the ATM layer to the PHY layer for synchronizing transfers on RXDAT[0:7].
W13	$\overline{\text{RXENB}}$	Slave: I Master: O PUA	UTOPIA Receive Enable Slave: Active low signal asserted by the ATM layer to indicate that RXDAT[0:7] and RXSOC will be sampled at the end of the next cycle. Master: Active low signal asserted by the PHY layer to indicate that RXDAT[0:7] and RXSOC will be sampled at the end of the next cycle.