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date 08/18/2014

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SERIES: PYB30 | **DESCRIPTION:** DC-DC CONVERTER

FEATURES

- up to 30 W isolated output
- industry standard pinout
- 4:1 input range (9~36 Vdc, 18~75 Vdc)
- smaller package
- single/dual/triple regulated outputs
- 1,500 Vdc isolation
- continuous short circuit, over current protection, over voltage protection
- temperature range (-40~85°C)
- six-sided metal shielding
- efficiency up to 90%

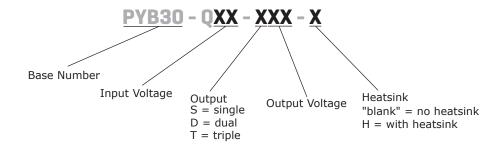




MODEL		nput oltage	output voltage		itput rrent	output power	ripple and noise¹	efficiency
	typ (Vdc)	range (Vdc)	(Vdc)	min (mA)	max (mA)	max (W)	max (mVp-p)	typ (%)
PYB30-Q24-S5	24	9~36	5	300	6000	30	100	88
PYB30-Q24-S12	24	9~36	12	125	2500	30	100	88
PYB30-Q24-S15	24	9~36	15	100	2000	30	100	90
PYB30-Q24-D5	24	9~36	±5	±150	±3000	30	100	86
PYB30-Q24-D12	24	9~36	±12	±63	±1250	30	100	89
PYB30-Q24-D15	24	9~36	±15	±50	±1000	30	100	90
PYB30-Q24-T312	24	9~36	3.3 ±12	175 ±31	3500 ±625	26.5	100	85
PYB30-Q24-T315	24	9~36	3.3 ±15	175 ±25	3500 ±500	26.5	100	86
PYB30-Q24-T512	24	9~36	5 ±12	150 ±31	3000 ±625	30	100	88
PYB30-Q24-T515	24	9~36	5 ±15	150 ±25	3000 ±500	30	100	88
PYB30-Q48-S5	48	18~75	5	300	6000	30	100	88
PYB30-Q48-S12	48	18~75	12	125	2500	30	100	88
PYB30-Q48-S15	48	18~75	15	100	2000	30	100	89
PYB30-Q48-D5	48	18~75	±5	±150	±3000	30	100	86
PYB30-Q48-D12	48	18~75	±12	±63	±1250	30	100	87
PYB30-Q48-D15	48	18~75	±15	±50	±1000	30	100	87
PYB30-Q48-T312	48	18~75	3.3 ±12	175 ±31	3500 ±625	26.5	100	85
PYB30-Q48-T315	48	18~75	3.3 ±15	175 ±25	3500 ±500	26.5	100	85
PYB30-Q48-T512	48	18~75	5 ±12	150 ±31	3000 ±625	30	100	88
PYB30-Q48-T515	48	18~75	5 ±15	150 ±25	3000 ±500	30	100	87

Notes: 1. Ripple and noise are measured at 20 MHz BW by "parallel cable" method with 1 μ F ceramic and 10 μ F electrolytic capacitors on the output.

PART NUMBER KEY



INPUT

parameter	conditions/description	min	typ	max	units
operating input voltage	24 Vdc input models 48 Vdc input models	9 18	24 48	36 75	Vdc Vdc
start-up voltage	24 Vdc input models 48 Vdc input models (single/dual output models) 48 Vdc input models (triple output models)			9 18 17.8	Vdc Vdc Vdc
under voltage shutdown ¹	24 Vdc input models 48 Vdc input models	7.8 16			Vdc Vdc
surge voltage	for maximum of 1 second 24 Vdc input models 48 Vdc input models	-0.7 -0.7		50 100	Vdc Vdc
start-up time			10		ms
filter	pi filter				
	models ON (CTRL open or connect high level, 2.5~1	2 Vdc)			
CTRL ²	models OFF (CTRL connect GND or low level, 0~1.2 Vdc)				
	input current (models OFF)		1		mA

Notes:

- 1. Contact CUI if you are planning to use this feature in your application. 2. CTRL pin voltage is referenced to GND.

OUTPUT

onditions/description	min	typ	max	units
full load, input voltage from low to high single and dual output models triple output models (main output) triple output models (auxiliary outputs)		±0.2	±0.5 ±1 ±5	% % %
% to 100% load, nominal input ingle and dual output models riple output models (main output) riple output models (auxiliary outputs)		±0.5	±1 ±2 ±5	% % %
ual output models: nain output 50% load, secondary output from 0% to 100% load			±5	%
ingle and dual output models riple output models (main output) riple output models (auxiliary outputs)		±1 ±1 ±3	±3 ±3 ±5	% % %
		±10		%
WM mode		400		kHz
5% load step change		300	500	μs
5% load step change		±3	±5	%
00% load, single and dual output models 00% load, triple output models			±0.02 ±0.03	%/°C %/°C
i ~ ~ () i ~ ~ () i ~ ~ () i ~ ()	ingle and dual output models riple output models (main output) riple output models (auxiliary outputs) % to 100% load, nominal input ringle and dual output models riple output models (main output) riple output models (auxiliary outputs) ual output models: nain output 50% load, secondary output from 0% to 100% load ringle and dual output models riple output models (main output) riple output models (main output) riple output models (auxiliary outputs) WM mode 5% load step change 5% load step change 00% load, single and dual output models	ingle and dual output models riple output models (main output) riple output models (auxiliary outputs) % to 100% load, nominal input ringle and dual output models riple output models (main output) riple output models (auxiliary outputs) ual output models: riain output 50% load, secondary output from 0% to 100% load ringle and dual output models riple output models (main output) riple output models (main output) riple output models (auxiliary outputs) WM mode 5% load step change 5% load step change 00% load, single and dual output models	ingle and dual output models ±0.2 riple output models (main output) riple output models (auxiliary outputs) % to 100% load, nominal input ringle and dual output models (main output) riple output models (main output) riple output models (auxiliary outputs) ual output models: riain output 50% load, secondary output from 0% to 100% load rigle and dual output models riple output models (main output) riple output models (main output) riple output models (auxiliary outputs) ±1 riple output models (auxiliary outputs) ±10 WM mode 400 5% load step change 300 5% load step change ±3 00% load, single and dual output models	rigle and dual output models

3. For dual output models, unbalanced load can not exceed $\pm 5\%$. If $\pm 5\%$ is exceeded, it may not meet all specifications. Notes:

^{4.} Output trimming available on single and dual output models only.

PROTECTIONS

parameter	conditions/description	min	typ	max	units
short circuit protection	hiccup, continuous, automatic recovery				
over current protection			150		%
	3.3 Vdc output models		3.9		Vdc
over voltage protection	5 Vdc output models		6.2		Vdc
	12 Vdc output models		15		Vdc
	15 Vdc output models		18		Vdc

SAFETY AND COMPLIANCE

parameter	conditions/description	min	typ	max	units
isolation voltage	for 1 minute at 1 mA max.	1,500			Vdc
isolation resistance	at 500 Vdc	1,000			МΩ
conducted emissions	CISPR22/EN55022, class A, class B (external circuit required, see Figure 1-b)				
radiated emissions	CISPR22/EN55022, class A, class B (exter	CISPR22/EN55022, class A, class B (external circuit required, see Figure 1-b)			
ESD	IEC/EN61000-4-2, class B, contact ± 4kV				
radiated immunity	IEC/EN61000-4-3, class A, 10V/m	IEC/EN61000-4-3, class A, 10V/m			
EFT/burst	IEC/EN61000-4-4, class B, ± 2kV (externa	al circuit required, see F	igure 1-a)		
surge	IEC/EN61000-4-5, class B, ± 2kV (externa	al circuit required, see F	igure 1-a)		
conducted immunity	IEC/EN61000-4-6, class A, 3 Vr.m.s				
voltage dips & interruptions	IEC/EN61000-4-29, class B, 0%-70%				
MTBF	as per MIL-HDBK-217F @ 25°C	1,000,000			hours
RoHS	2011/65/EU				

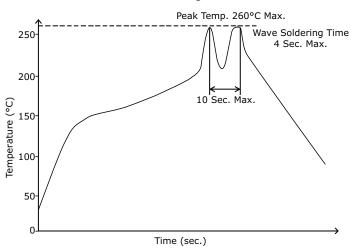
ENVIRONMENTAL

parameter	conditions/description	min	typ	max	units
operating temperature	see derating curve	-40		85	°C
storage temperature		-55		125	°C
storage humidity	non-condensing	5		95	%
case temperature	at full load, Ta=71°C			105	°C

SOLDERABILITY

parameter	conditions/description	min	typ	max	units
hand soldering	1.5 mm from case for 10 seconds			300	°C
wave soldering	see wave soldering profile			260	°C





MECHANICAL

parameter	conditions/description	min	typ	max	units
dimensions	board mount: $50.8 \times 40.6 \times 11.8$ board mount with heatsink: $50.8 \times 40.6 \times 16.3$				mm mm
case material	aluminum alloy				
weight	board mount board mount with heatsink		50 70		g g

MECHANICAL DRAWING

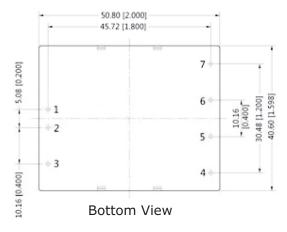
BOARD MOUNT

units: mm[inch]

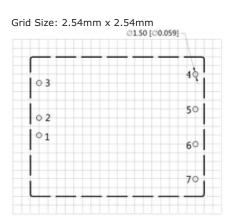
tolerance: $\pm 0.25[\pm 0.010]$

pin diameter tolerance: $\pm 0.10[\pm 0.004]$ pin height tolerance: $\pm 0.50[\pm 0.020]$

PIN CONNECTIONS			
PIN	Single Output	Dual Output	Triple Output
1	Vin	Vin	Vin
2	GND	GND	GND
3	CTRL	CTRL	CTRL
4	Trim	Trim	-Vo2
5	0V	-Vo	0V
6	+Vo	0V	+Vo1
7	NP	+Vo	+Vo2







PCB Layout Top View

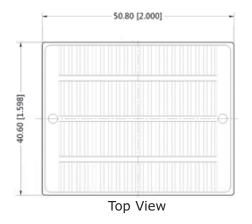
BOARD MOUNT WITH HEATSINK

units: mm[inch]

tolerance: $\pm 0.3[\pm 0.012]$

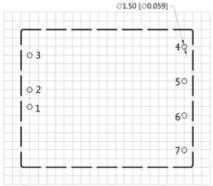
pin diameter tolerance: ±0.10[±0.004] pin height tolerance: $\pm 0.50[\pm 0.020]$

	PIN CONNECTIONS			
PIN	Single Output	Dual Output	Triple Output	
1	Vin	Vin	Vin	
2	GND	GND	GND	
3	CTRL	CTRL	CTRL	
4	Trim	Trim	-Vo2	
5	0V	-Vo	0V	
6	+Vo	0V	+Vo1	
7	NP	+Vo	+Vo2	



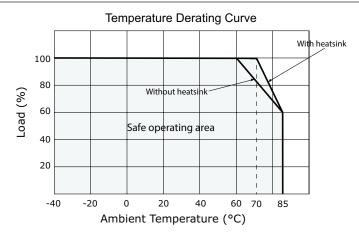
4.10 [0.161] 16.30[0.642] Ø 1.00 [Ø 0.039] Front View

Grid Size: 2.54mm x 2.54mm



PCB Layout Top View

DERATING CURVES



EMC RECOMMENDED CIRCUIT

Figure 1 Single Output LDM FUSE _с3 Vin +Vo EUT LOAD C2 TVS GND O GND 0 V (b) (a) C4 **Dual Output** LDM LCM FUSE <u></u>С3 Vin O LOAD EUT _{0V} TVS LOAD GND O GND (b) (a) -Vo C4 Triple Output +Vo1 LDM ∔cз FUSE +Vo2 Vin O Vin LOAD LOAD EUT C2 0 V TVS GND O LOAD GND (b) (a) ⁼C4 -Vo2

Table 1

Recomm	Recommended external circuit components				
Vin (Vdc)	24	48			
FUSE	Choose according	to input current			
MOV	10D560K	10D101K			
LDM	56µH	56µH			
TVS	SMCJ48A	SMCJ90A			
C0	120μF/50V	120μF/100V			
C1	4.7µF/50V	2.2µF/100V			
LCM	2.2mH	2.2mH			
C2	4.7μF/50V	2.2µF/100V			
C3*	1nF/2kV	1nF/2kV			
C4*	1nF/2kV	1nF/2kV			

Note: *2nF/2kV capacitors for triple output, 48 Vdc input

TEST CONFIGURATION

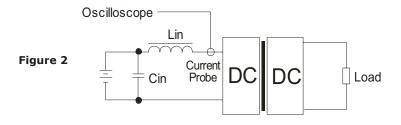


Table 2

External components		
Lin 4.7µH		
Cin	220μF, ESR < 1.0Ω at 100 kHz	

Note: Input reflected-ripple current is measured with an inductor Lin and Capacitor Cin to simulate source impedance.

APPLICATION NOTES

Recommended circuit

This series has been tested according to the following recommended testing circuit before leaving the factory. This series should be tested under load (see Figure 3). If you want to further decrease the input/output ripple, you can increase the capacitance accordingly or choose capacitors with low ESR (see Table 3). However, the capacitance of the output filter capacitor must be appropriate. If the capacitance is too high, a startup problem might arise. For every channel of the output, to ensure safe and reliable operation, the maximum capacitance must be less than the maximum capacitive load (see Table 4).

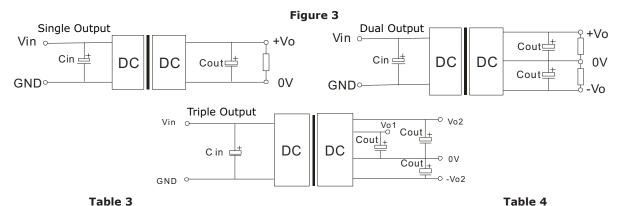


Table 3

Single Vout (Vdc)	Cin (µF)	Cout (µF)	Dual Vout (Vdc)	Cin (µF)	Cout¹ (µF)	Triple Vout (Vdc)	Cin (µF)	Cout¹ (µF)
						3.3	10	10
5	10	10	±5	10	10	5	10	10
12	10	4.7	±12	10	4.7	±12	10	4.7
15	10	4.7	±15	10	4.7	±15	10	4.7

Note:

1. For each output.

Single Vout (Vdc)	Max. Capacitive Load (µF)	Dual Vout (Vdc)	Max. Capacitive Load¹ (µF)	Triple Vout (Vdc)	Max. Capacitive Load¹ (μF)
				3.3/±12	4700/300
5	6000	5	2000	3.3/±15	4700/220
12	2500	12	1250	5/±12	4700/300
15	1100	15	680	5/±15	4700/220

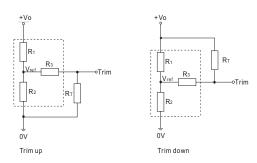
1. For each output. Note:

Output voltage trimming

Leave open if not used.

Figure 4

Application Circuit for Trim pin (part in broken line is the interior of models)



Formula for Trim Resistor

up:
$$R_T = \frac{aR_2}{R_2 - a} - R_3$$
 $a = \frac{Vref}{Vo' - Vref} \cdot R_1$

 $a = \frac{\text{Vo'} - \text{Vref}}{\text{Note of }} \cdot R_2$ down: $R_T = \frac{aR_1}{R_1-a} -R_3$

Note: Value for R1, R2, R3, and Vref refer to Table 5 R₊: Trim Resistor

> a: User-defined parameter, no actual meanings Vo': The trim up/down voltage

Table 5

Vout (Vdc)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	Vref (V)
5	2.883	2.864	10	2.5
12	10.971	2.864	17.8	2.5
15	14.497	2.864	17.8	2.5

1. Minimum load shouldn't be less than 5%, otherwise ripple may increase dramatically. Operation under minimum load will not damage the converter, however, they may Note: not meet all specifications listed.

2. Maximum capacitive load is tested at input voltage range and full load.

3. All specifications are measured at Ta=25°C, humidity<75%, nominal input voltage and rated output load unless otherwise specified.

REVISION HISTORY

rev.	description	date
1.0	initial release	06/26/2013
1.01	updated spec	08/15/2013
1.02	updated spec	08/18/2014

The revision history provided is for informational purposes only and is believed to be accurate.



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