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### **Precision Mixed-Signal** 32-bit Microcontroller

#### Introduction

Q32M210 is a precision, mixed-signal 32-bit microcontroller. The microcontroller is built on the high performance  $ARM^{(B)}$  Cortex  $^{m}$ -M3 processor.

The microcontroller incorporates a highly configurable sensor interface designed to work directly with a wide range of sensors having multiple characteristics, including specialized electrochemical sensors. The sensor interface includes dual programmable gain amplifiers, dual 16-bit Analog-to-Digital converters, triple 10-bit Digital-to-Analog converters (for voltage waveform generation and other applications) and three uncommitted, low-noise opamps with configurable signal multiplexing. Flexible connectivity to external non-volatile memory, personal computers, wireless devices, LCD displays and a wide range of other peripherals is enabled by several digital interfaces including I<sup>2</sup>C, USB (2.0 full-speed compliant) and a high-speed SPI/SQI interface.

The microcontroller features flexible clocking options as well as intelligent failure monitoring of power and application interruptions required by high performance, portable, battery operated applications. All necessary clocks including an internal oscillator, real-time clock and a dedicated clock for USB operation are available on-chip (external crystals required for RTC and USB).

An embedded power management unit, which incorporates several low power modes, allows application developers to minimize both standby and active power under a wide range of operating conditions. The ultra-low sleep current makes the microcontroller ideal for applications that remain inactive for long periods of time.

A large on-chip non-volatile flash memory (256 kB) combined with on-chip SRAM (48 kB) supports complex applications and simplifies application development. The flash contains built-in hardware error checking and correction (ECC) for application reliability. Additionally, a configurable DMA unit which supports independent peripheral-to-memory, memory-to-memory, and memory-to- peripheral channels provides flexible, low power data transfers without processor intervention.

A suite of industry-standard development tools, hands-on training and full technical support are available to reduce design cycle time and speed time-to-market.

• The Q32M210 Microcontroller is Pb–Free, Halogen Free/BFR Free and RoHS Compliant



See detailed ordering and shipping information in the package dimensions section on page 50 of this data sheet.

#### Contents

Introduction	. 1
Key Features	. 2
Functional Overview	. 4
Pin Definition and Descriptions	. 11
Recommended Operating Conditions	. 19
ESD and Latch-up Characteristics	. 19
Electrical Characteristics	. 20
Typical Operating Characteristics	. 33
Detailed Function Descriptions	. 38
Example Application Diagrams	46

#### **Key Features**

#### Ultra Low-Power and Smart Power Management

- $\bullet\,$  Less than 400  $\mu A$  / MHz, up to 16 MHz clock speed
- Reliable operation down to 1.8 V; 3.3 V nominal supply voltage
- Ultra-low-current sleep mode with Real-time Clock active (< 750 nA)
- Low-current standby mode with register and SRAM retention (< 26 µA)
- Integrated power supplies minimize need for external components. Only a minimum of external passives is required

### Efficient, Powerful and Robust Processing Architecture

- 32-bit ARM Cortex-M3 CPU
- 256 kB on-chip flash with integrated hardware ECC for program and user data storage
- 48 kB on-chip SRAM
- Flexible DMA, 4 general–purpose timers, CRC calculator
- No external voltage required for flash write operation

### Low-Noise, Low-Leakage, Low-Temperature Drift, Configurable Sensor Interface

- Triple ultra low-noise opamps with low-leakage inputs and configurable outputs
- Dual on-chip Programmable Gain Amplifiers (PGA) and ADCs with flexible input multiplexing and wide dynamic range
- Reconfigurable voltage detection unit
- Optimal dynamic range scaling of sensor signals
- Flexible on-chip signal routing for dynamic reconfigurability
- Minimal temperature drift of gain and offset errors allows for precise calibration
- Built-in Temperature Sensor

#### **Predictable Operation**

• Dedicated brown-out protection circuit prevents execution of code outside of operating range

- Integrated hardware-based ECC for on-chip flash maintains code and data integrity
- Watchdog timer

### High Precision Analog-to-Digital Conversion and Digital-to-Analog Conversion

- Dual 16-bit ADCs with on-the-fly data rate configurability
- Triple 10-bit DACs with configurable dynamic range

#### **Precision Voltage Reference**

• On-chip, low temperature drift (< 50 ppm/°C) voltage reference for ADCs and DACs

#### Flexible On-Chip Clocking

• Processor supports speeds up to 16 MHz provided either through internal oscillator or externally supplied clock

#### Flexible Sensor Interconnections

- Triple low R<sub>on</sub> analog multiplexers, including an 8:1 input mux
- Quad SPST and quad multi-switches for effective simultaneous connection to different sensors

#### USB 2.0 Full-Speed Interface

• Built-in transceiver for 2.0 Full-speed compatible (12 Mbps) operation with dedicated power supply

#### Flexible External Interfaes

- Configurable Interface Wakeup pins with configurable pull-ups and pull-downs
- 8 Configurable GPIO interrupts
- Dual UARTs, dual SPI, SQI, I<sup>2</sup>C, PCM (including I2S mode), GPIOs

#### LCD Interface

• Up to 112 segments with integrated charge pump and backlight driver (up to 10 mA)

#### Packaging

• Available in 140-pin TLLGA



Figure 1. Functional Overview

#### FUNCTIONAL OVERVIEW

#### **Operating Modes**

Three low-power operating modes are available

- Run mode used during normal program execution; the entire device is fully operational in run mode
- 2. Standby mode used for lower current consumption, with paused program execution and fast wakeup
- 3. Sleep mode used for ultra low current consumption, with no program execution and restart after wakeup

Each mode is designed to provide the lowest possible current consumption, while maintaining power to specific parts of the device.

#### Run Mode

Run mode provides a low power mode where the entire system is fully functional. In run mode, the device enables the on-chip VDDD Digital Supply Regulator to provide power to the ARM Cortex-M3 Processor. The processor is clocked from either an internal or an external clock source. The program can be executed from the internal flash or SRAM.

The application can selectively enable or disable sensor interface components, including supply regulators and references, as required. The application may also adjust the device clock frequency through the internal oscillator or through clock divisors to minimize power consumption. The digital and analog interfaces may be configured as required in run mode. Internal clock dividers provide all the necessary clocks to the sensor interface and peripherals.

While in run mode, the application may switch into either sleep mode or standby mode.

#### Standby Mode

Standby mode provides a low power mode where the digital system state is retained. In standby mode, the ARM Cortex–M3 Processor execution is paused. The VDDD Digital Supply Regulator voltage is reduced. The contents of all the registers and SRAM are retained.

The power supervisor automatically disables and powers down the sensor interface components, including the analog supply regulators and references. The application may selectively enable or disable the RTC, RTC alarm, and the Wakeup controller. The internal oscillator is automatically disabled.

When in standby mode, the device may be switched into run mode by either the RTC alarm or by up to four external events (through the Wakeup controller).

#### Sleep Mode

Sleep mode provides an ultra-low power mode where the system is waiting for a wakeup event. In sleep mode, the power supervisor automatically disables and powers down the digital and analog supply regulators, the internal oscillator, and all the sensor interface components. The application may selectively enable or disable the RTC, RTC alarm, and the Wakeup controller.

When in sleep mode, the device may be switched into run mode by either the RTC alarm or by up to four external events (through the Wakeup controller). After exiting sleep mode, the system state is reset and execution starts from the beginning of the ROM program.

A general purpose retention register is available to store state. The retention register contents are retained after exiting sleep mode. This register may be used by the application to quickly restore its state.

#### **Power Supply**

The device can powered from a single battery supply such as a 2032 lithium coin cell. The device supplies all required regulated voltages and references on-chip. This allows the device to operate directly from a single battery supply without the need for external regulators or switches.

#### VBAT and VBATA

The main power supply input for the device is VBAT. The supplied voltage to VBAT is typically 3.3 V but it can be supplied with any voltage between 1.8 V and 3.6 V. The device will operate reliably across this entire power supply range. This flexibility allows for a wide range of battery types to be directly connected to the device.

The sensor interface power supply for the device is VBATA. VBATA is typically 3.3 V but it can be supplied with any voltage between 1.8 V and 3.6 V. The sensor interface will operate reliably across this entire power supply range however the performance of the sensor interface may be reduced when VBATA drops below 2.2 V. VBATA also powers the IF5 pins.

In a typical application, VBATA and VBAT are both connected directly to the battery supply. To increase the useful operating life of the battery VBATA may be externally connected to the on-chip charge pump output (VDBL) instead of the battery. In this configuration the sensor interface power supply remains nominally 3.5 V even as the battery voltage drops.

VBAT is monitored by the built-in power supervisor. VBATA is not directly monitored but may be measured through the sensor interface.

#### Regulators

All required voltages for normal device operation are generated on-chip.

#### VDDD

The VDDD Digital Supply Regulator (VDDD) provides a nominal 1.8 V power supply for the ARM Cortex–M3 Processor, digital peripheral and memories, including the on–chip flash. VDDD is generated on–chip and is connected to the digital components internally. It is also available externally. Flash memory reads and writes require only a minimum voltage of 1.8 V. No external power management circuitry is required to support flash access.

#### VADC

The VADC Analog Supply Regulator (VADC) provides a nominal 1.8 V power supply for the ADCs and PGAs. This separate supply ensures noise immunity between the analog and digital subsystems. VADC may be enabled or disabled as required to save power.

#### VDBL

The VDBL Charge Pump (VDBL) provides a nominal 3.5 V power supply under any normal operating range battery voltage. VDBL is powered from the dedicated on-chip Charge Pump Supply Regulator (VCP). This separate supply ensures noise immunity between VDBL, the other on-chip power supplies as well as from the battery. VDBL is normally used to power an LCD segment display and associated backlight or any other external devices requiring a fixed, high voltage rail. VDBL may also be used to power the sensor interface. This is useful when a fixed, higher voltage rail is required for the sensor interface compared to the battery voltage.

#### ILV

An on-chip programmable current sink (ILV) is available to adjust the amount of current from VDBL through an LED backlight. In a typical configuration an LED is connected between VDBL and ILV. The application controls the LED brightness by adjusting the current setting.

#### **VREF Precision Voltage Reference**

The device provides an on-chip low-temperature drift reference voltage, VREF. VREF is factory calibrated to 0.9 V. VREF is available externally and is also connected internally to the ADCs and DACs for their reference voltages.

#### I/O Pin Supplies

The device's I/O pins are powered from multiple supplies. This allows the device to match its I/O voltage levels to external devices as required.

One bank of digital I/O pins is powered from VDDIO0. The voltage applied to VDDIO0 determines the logic level for the associated pins. A second bank of mixed signal I/O pins is powered from VDDIO1.

The voltage applied to VDDIO1 determines the digital logic level for the associated pin. When the mixed signal I/O pins are configured for LCD operation, VDDIO1 must be at or above VLCD supply voltage for proper operation.

The USB pins USBDP and USBDN are powered directly from VDDUSB.

The IF5 pins are powered directly from VBATA.

All analog signal pins are powered directly from VBATA.

### Power Supervisor, Power-on Reset, and Brown-Out Protection

The device contains a dedicated hardware power supervisor for monitoring the supply voltages. The power

supervisor ensures the device operates deterministically, and without any unexpected behavior during all supply conditions.

The power supervisor releases the internal Power-on Reset (POR) when the supply voltage on VBAT exceeds the minimum threshold for proper operation. The release of POR enables the VDDD Digital Supply Regulator. The power supervisor continues to monitor VBAT. If VBAT drops below the minimum threshold for proper operation the device is reset.

No external circuitry is required for proper device startup. All required start-up delays and reset thresholds are generated on-chip. The RSTB pin may be left floating during startup.

The ARM Cortex–M3 Processor and all digital subsystem components including the flash, SRAM, and peripherals will operate reliability down to a nominal VDDD supply voltage of 1.8 V. In run mode, the power supervisor continually monitors VDDD. If VDDD drops below the minimum threshold for proper operation the device is reset.

The power supervisor is automatically disabled in sleep mode and standby mode to save power.

#### Supply Monitor

During run mode, the actual voltage levels for VBAT, VBATA, VREF, and VADC can be measured through either one of the ADC channels. This allows the application to determine the actual supply levels and appropriately handle the graceful shutdown of the system when the battery approaches its useful end-of-life. Additional voltages may be monitored through one of the auxiliary inputs.

In a system configuration where the sensor interface may be supplied from either the battery or the VDBL Charge Pump, the application can use the measured VBAT voltage level to determine whether to enable VDBL or continue to supply the sensor interface from the battery.

#### External Reset

The device contains an external reset pin (RSTB). When RSTB is asserted, the digital subsystem including the ARM Cortex-M3 Processor is reset. The real-time clock counters are not reset by an external reset. The RSTB function is only available in run mode. Asserting the RSTB pin during the Power-on Reset sequence will prevent the ARM Cortex-M3 Processor from running. The system will be held in reset until the pin is released. RSTB can be left floating.

#### System Wakeup

Wakeup occurs when the device is switched from standby mode or sleep mode into run mode. This can be accomplished through one of the wakeup mechanisms. The wakeup controller allows for up to four external events to wake up the system. Two IF5 pins (IF5.0, IF5.1) will wakeup the system when a High-to-Low transition is detected. Two IF5 pins (IF5.2, IF5.3) will wakeup the system when a Lowto-High transition is detected. The RTC Alarm can also be configured to wakeup the system at a predetermined time.

#### Clocking

The device contains several clock generators and clock I/O capability. After Power–on Reset, the device selects the internal oscillator as the system clock source. The default clock frequency at POR is 3 MHz. After boot, the application may select another frequency or switch to another clock source. The device may select the real–time crystal oscillator (32.768 kHz) as the clock source, when low operating frequencies are required to save power.

#### Internal Oscillator

The device contains a reconfigurable, factory calibrated internal oscillator. The calibration settings are stored in the on-chip flash. Settings are available for all integer frequencies in the normal operating range (1 MHz to 16 MHz). Finer calibration is possible.

The default setting after Power-on Reset is 3 MHz. The application can switch to any operating frequency after entering run mode.

#### External Clock

The device contains an external clock I/O pin (EXT\_CLK). EXT\_CLK may be used as a clock source for the entire system or as a clock output. The application may switch to use an externally supplied clock or output a clock after boot. If neither function is desired EXT\_CLK may be left floating.

An external clock detection circuit is included that will automatically switch the system to the internal oscillator, if the external clock is selected, but no clock signal is detected.

When EXT\_CLK is used as an output, the frequency of the output clock can be divided before EXT\_CLK is output.

#### Real-Time Clock

The device contains an ultra low-power real-time clock (RTC). The RTC includes a real-time crystal oscillator, read-write RTC counters, and a configurable alarm. The real-time crystal oscillator utilizes a 32.768 kHz external crystal.

The RTC may be enabled or disabled in each of the three operating modes. The RTC is powered directly from VBAT. This allows the RTC to continue to run when the VDDD Digital Supply Regulator voltage is reduced in standby mode or disabled in sleep mode and thus the system date and time information are always maintained. The RTC is reset after the initial Power–on Reset but remains operational through a digital reset (RSTB or watchdog) and operating mode switching.

The alarm function can be configured to wake-up the system from standby mode or sleep mode at a pre-determined time. The alarm will also generate an interrupt to the ARM Cortex-M3 Processor. The alarm can be configured for absolute mode or relative mode. In relative mode, the alarm is automatically reloaded after each alarm trigger. This is useful for extremely low-duty-cycle applications that require periodic polling.

#### **USB Crystal Oscillator**

The device contains a dedicated USB crystal oscillator. The oscillator requires an external 48 MHz crystal for compliance with the USB interface specification. The clock output is used internally for the USB PHY and USB core.

During USB operation the ARM Cortex-M3 Processor and all other system blocks continue to run on the slower system clock. This allows the device to achieve low system current even while the USB interface is active.

The USB Crystal Oscillator can be enabled or disabled.

#### **Clock Divisors**

On-chip clock divisors and prescalers are available to provide selectable frequencies to the ARM Cortex-M3 Processor, sensor interface, peripherals and external interfaces. These divided clocks are derived from the root clock source and may be configured independently. This adjustability allows the optimum clock frequency to be selected for each system component.

#### Sensor Interface

#### Opamps

Three uncommitted low-noise opamps are available. Each opamp is directly powered from the VBATA supply for achieving high input dynamic range for sensor interface signals. Each of the opamp's positive and negative terminals is brought out to a dedicated input pin on the device. Each opamp output terminal is connected to two dedicated output pins. An internal switch selects between output to one or both of the output pins, allowing for dynamic reconfigurability of the external opamp feedback network.

#### Signal Multiplexing

A comprehensive input multiplexing scheme allows for flexible interconnection of a wide range of sensors and external circuits to be connected to the sensor interface. The input multiplexing consists of:

- An 8:1 analog multiplexer Connects one of 8 low-leakage input pins to an opamp negative terminal
- A 3:1 analog multiplexer Connects one of 3 low-leakage input pins to an alternate sensor node (ALT0) and optionally to an opamp negative terminal
- A 5:1 analog multiplexer Connects one of 5 low–leakage input pins to an alternate sensor node (ALT1) and optionally to an opamp negative terminal

Each multiplexer signal path features low Ron characteristics providing nearly transparent signal routing for any external sensor. The input multiplexer configuration may be changed on-the-fly by the application.

#### Dual PGA and ADC

Two independent 16-bit Analog-to-Digital Converters (ADCs) are available. The ADCs provide a very high resolution, a high degree of linearity, as well as low gain and offset temperature drifts. Each ADC is coupled with a

Programmable Gain Amplifier (PGA) allowing signals to be sampled without external buffering. The ADC data rate is reconfigurable and a wide range of data rates are possible. Each ADC conversion takes a fixed time resulting in a deterministic, periodic sampling. Lower data rates may be configured to achieve a higher effective dynamic range.

The ADCs operate rail-to-rail from 0 V to VADC (1.8 V) using the internal VREF Precision Voltage Reference (0.9 V). Unsigned or two's complement output samples are provided to the ARM Cortex-M3 Processor and synchronized to the periodic ADC interrupt. The DMA may also be used to transfer samples directly from the ADC to SRAM.

Each PGA and ADC has 16 multiplexed inputs allowing a wide range of sensor interface signals to be measured. In addition, power supply voltages are available as measurement inputs for application level supply monitoring.

#### Programmable Gain Amplifiers

A PGA is used to directly feed each of the ADC inputs. The PGAs operate in either single–ended mode or differential mode. Single–ended operation is obtained by setting one PGA input to VSS. Differential operation is obtained by routing signals to each of the two PGA inputs. The resulting voltage is amplified, anti–alias filtered, and output into the ADC. A wide range of gain steps from 0 dB to 36 dB allow for optimal adjustment of the PGA output to match the dynamic range of the ADC.

PGA1 operates in one of three input modes. Each input mode provides a different common-mode voltage range with linearity characteristics and tradeoffs. The application may choose different PGA1 operating modes depending on the type of measurement being made. PGA0 operates in a single input mode only.

#### **Automatic Voltage Detection**

Automatic voltage detection is available on PGA0. When enabled, the PGA0 will output an interrupt to the ARM Cortex–M3 Processor when the PGA0 output voltage exceeds the configured threshold. To save power the ADCs may be disabled while waiting for the detection signal.

#### **Auxiliary Inputs**

Three auxiliary inputs provide a direct connection to the PGA and ADC multiplexers. External voltages such as thermistor networks may be connected to any of these high impedance inputs for direct measurement with the ADC.

#### **Triple DAC**

Three independent 10-bit DACs are available. Each DAC output is individually controlled by the ARM Cortex-M3 Processor. The DACs provide a high degree of linearity, low gain and offset temperature drift, and are monotonic within the normal operating range.

The dynamic range of DAC0 is reconfigurable. The 10-bit output range may be mapped into one of three ranges: 1 x VREF, 2 x VREF, or 3 x VREF. This reconfigurable

dynamic mapping allows a tradeoff between LSB resolution and dynamic range.

The dynamic range of DAC1 and DAC2 is fixed to 2 x VREF.

#### **Temperature Sensor**

The device contains a built–in temperature sensor. The temperature sensor works by generating a differential voltage that varies linearly with temperature. The voltage is routed into the PGA resulting in a single–ended output voltage measurable by the ADC.

The temperature sensor is calibrated during factory production by ON Semiconductor. The calibration value is stored in the flash. The device junction temperature may be determined based on the calibration factor and converted ADC output value.

#### **SPST Switches**

The device contains four analog general-purpose, low-leakage, low-Ron, single-pole single-throw switches (SPSTs). Each SPST consists of 2 ports – A and B. The SPST connection is determined by the application and may be changed in real-time. Port A can be connected or disconnected from Port B.

The SPSTs can be used for routing both power supplies and signals. Each SPST is designed to conduct a continuous current of up to  $\pm$  10 mA. This provides sufficient current bandwidth to supply power to external devices such as LCD displays or wireless transceivers.

When routing signals through the SPST, the low-leakage characteristics allow the switch to create a high isolation between a measurement node and the sensor interface. The application may connect the measurement node to the sensor interface through the SPST as required. The low-leakage characteristics allow the SPST to be added to the signal chain without interfering with the impedance properties of the measurement node.

#### Multi-Switches

The device contains four analog general-purpose, low-leakage, low-Ron multi-switches (MSWs). Each MSW consists of 3 ports – Port A, Port B, and Port C (Common). The MSW connection is determined by the application and may be changed in real-time. The MSW may be configured to connect A to C, B to C, A and B to C, or neither to C. A signal of interest may be connected to the common port, and selectively routed to A, B, or A and B. Alternately, two signals of interest may be connected to A and B, respectively, and either one selectively routed to C.

The MSWs may be used for routing both power supplies and signals. Each MSW is designed to conduct a continuous current of up to 10 mA. This provides sufficient current bandwidth to supply power to external devices such as LCD displays or wireless transceivers.

The MSWs may be configured to switch based on the on-chip reconfigurable pulse-width modulator (PWM).

The PWM On/Off duty cycle time can be configured by the application allowing the MSWs to act as a power regulator.

#### **ARM Cortex-M3 Processor**

The ARM Cortex-M3 processor is a 32-bit RISC controller specifically designed to meet the needs of advanced, high-performance, low-power applications. The ARM Cortex-M3 processor provides outstanding computational performance and exceptional system response to interrupts while providing small core footprint, industry leading code density enabling smaller memories, reduced pin count and low power consumption.

The Q32M210 implementation of the ARM Cortex–M3 Processor contains all necessary peripherals and bus systems to provide a complete device optimized for battery powered sensor interface applications.

#### Memories

#### **Flash Memory**

256 kB flash is available for storage of application code and data. Flash memory can be written one or more words at a time. Each page must be erased between writes to a flash word. The flash memory can be erased as a set all at once or in individual 2 kB pages. An additional reserved block of flash memory is used to store factory calibration information provided by ON Semiconductor. This block can not be written by the application.

The ARM Cortex-M3 processor executes application code directly from flash with zero wait states.

#### Flash Error Checking and Correction

A dedicated hardware block performs real-time error checking and correction of the flash. Additional parity bits are stored automatically for each word in the flash. The hardware ECC is able to detect up to 2-bit errors per word or detect and correct 1-bit error per word. The hardware ECC operates as each word is read from the flash. An interrupt can be generated upon correction of a bit error and a bus fault will be generated when a bit error is detected, but cannot be corrected.

#### SRAM

48 kB of low-power SRAM is available for storage of intermediate data as well as application code.

#### ROM

An on-chip ROM includes boot functionality as well as firmware routines supporting writing to flash in an application.

#### **External Interrupt Controller**

Eight configurable external interrupt sources may be connected to any eight GPIO pins on the device. This is in addition to a dedicated interrupt for the wakeup controller. Each interrupt may be individually configured for positive edge triggering, negative edge triggering, high level triggering, or low level triggering. A dedicated non-maskable interrupt (NMI) pin is connected directly to the ARM Cortex-M3 Processor. A logic high level on this pin will trigger the interrupt handler for the NMI.

#### DMA

A flexible DMA unit supports low overhead data exchange between system blocks. Memory-to-Peripheral, Peripheral-to-Memory, and Memory-to-Memory modes are available. Four simultaneous DMA channels can be established with configurable sources and sinks.

The DMA can be used with the UART, SPI, SQI, I<sup>2</sup>C, USB, and PCM interfaces, as well as the ADCs and DACs.

The DMA operates in the background allowing the ARM Cortex–M3 Processor to execute other applications or to reduce its operating frequency to conserve power.

#### General-Purpose Timers

The device contains four general-purpose timers. Each timer features a 12-bit countdown mode, an external interrupt to the ARM Cortex-M3 Processor, a dedicated prescaler, and the ability to poll the counter value. These four general-purpose timers are in addition to the 24-bit SYSTICK timer included as part of the ARM Cortex-M3 Processor.

#### **CRC Engine**

A 16-bit hardware CRC engine is available. The CRC engine may be used to ensure data integrity of application code and data. The CRC engine's input port and output port are directly accessible from the ARM Cortex–M3 Processor. The starting vector may be set to any value. Subsequently, data words of multiple bit lengths can be added to the CRC. The 16-bit CRC–CCITT polynomial is used.

#### Watchdog Timer

The device contains a digital watchdog timer. The watchdog timer is intended to prevent an indefinite system hang when an application error occurs. The application must periodically refresh the watchdog counter during operation. If a watchdog timeout occurs an initial alert interrupt is generated. If a subsequent watchdog timeout occurs, a system reset is generated. The initial alert may be used to gracefully shut down the system.

#### Dual UART

Two general-purpose UART interfaces are available. The UARTs support the standard RS232 protocol and baud rates at the VDDIO0 voltage level. The UART format is fixed at one start bit, eight data bits, and one stop bit. The baud rate is configurable over a wide range of baud rates up to 250 kbaud using a 1 MHz source clock.

The UART interfaces may be used either directly from the ARM Cortex-M3 Processor or through the DMA Controller.

#### Dual SPI

Two SPI interfaces are available supporting both master and slave operation. Each synchronous 4-wire interface provides a clock, chip select, serial data in, and serial data out connection. The SPI interface can be used to interface with external devices such as non-volatile memories, displays, and wireless transceivers.

The SPI interfaces can be used either directly from the ARM Cortex–M3 Processor or through the DMA Controller

#### SQI

The primary SPI interface can be configured to operate in SQI (serial quad interface) mode. In SQI mode 4 bits are interchanged simultaneously instead of 1 bit in SPI mode. In this way, the throughput of the interface is increased by a factor of 4 for the same clock frequency. The SQI interface is typically used to access large, external NVM arrays.

#### l<sup>2</sup>C

The I<sup>2</sup>C interface supports both master and slave operation. The interface operates at normal speed (100 kbit/sec) and high speed (400 kbit/sec). On-chip pull-up resistors are available on the SDA and SCL pins.

The  $I^2C$  interface can be used either directly from the ARM Cortex-M3 Processor or through the DMA Controller. The  $I^2C$  slave address is programmable by the application.

#### PCM

The pulse-code modulation (PCM) interface provides a data connection between the device and external devices such as Bluetooth or audio processors. The PCM interface can operate both in master and slave mode. The master device of a PCM transfer generates the frame signal.

The PCM interface can be used either directly from the ARM Cortex–M3 Processor or through the DMA controller. Two DMA channels are used with the PCM interface – one for RX, and one for TX.

The PCM interface supports a wide variety of interface protocols by reconfiguring the frame type and width, word size and clock polarities. The PCM interface supports the I2S data format directly for connecting to an I2S compatible audio device. Audio data can be streamed to and from the audio device over the PCM interface in I2S mode.

#### GPIO

GPIO pins can be configured as input or output signals. The pins are powered from VDDIO0, VDDIO1, or VBATA providing flexibility in the I/O voltage levels available. Different I/O voltage levels may be supplied to VDDIO0 and VDDIO1 within the normal operating range. GPIO functionality is shared with alternate functions on most GPIO pins. The GPIO or alternate function is selected through the application.

#### USB

The USB interface provides connectivity between the ARM Cortex–M3 Processor and a USB host. The USB interface operates as a USB Full Speed Device (12 Mbit/sec). The USB physical interface (PHY) is powered directly from VDDUSB. A minimum supply of 3 V is required. Typically VDDUSB will be powered from the +5 V provided by the USB bus regulated down to 3.3 V.

The interface requires a 48 MHz clock which is provided through the USB crystal oscillator. An external 48 MHz crystal is required for this interface to operate. The USB interface operates on a separate clock domain allowing the rest of the system to continue to run on the slower internal oscillator or external clock source. This enables reduced power consumption, since the ARM Cortex–M3 Processor can operate at a lower frequency than the USB clock when USB is operational.

The USB interface interfaces to the ARM Cortex-M3 Processor through memory-mapped control registers and interrupts. The DMA may be used to transfer data between the USB interface and the SRAM directly.

#### LCD

The device provides an on-chip LCD driver capable of driving up to 112 display segments of a 1/3 bias, 1/4 duty cycle LCD display. The interface consists of four common (COM) lines and twenty-eight (28) segment (SEG) lines. The drive voltages are sourced from VLCD and consist of four voltages (0 V, 1/3 x VLCD, 2/3 x VLCD, and VLCD).

#### LCD Backlight

The LCD backlight driver provides an application controlled current sink. It is programmable to sink nominally between 0 mA to 10 mA. An LCD backlight may be connected between VDBL and ILV. The current passing through the LED is regulated based on the current setting set by the application.

#### JTAG

The device contains a dedicated JTAG port for interfacing to the ARM Cortex-M3 Processor and memories. The device implements the standard JTAG-DP protocol provided by ARM, providing compatibility with many external debugging systems.



Figure 2. Pin Definition and Descriptions

Pin				Dull un /		Function			
140 TLLGA	Pin Name (Note 6)	Type (Note 1)	Direction (Note 2)	Pull-Down (Note 3)	Pin Power Supply	Primary (Note 4)	Alternate 1	Alternate 2	Alternate 3
B4	USBDP	D	I/O	-	VDDUSB	USBDP	-	-	-
A5	USBDN	D	I/O	-	VDDUSB	USBDN	-	-	-
B44	SCL	D	I/O	PU	VDDIO0	SCL	-	-	-
A51	SDA	D	I/O	PU	VDDIO0	SDA	-	-	-
A48	IF0.0	D	I/O	PU	VDDIO0	SPI0_CLK	GPIO32	-	-
A53	IF0.1	D	I/O	PU	VDDIO0	SPI0_CS	GPIO33	USRCLK0	-
A57	IF0.2	D	I/O	PU	VDDIO0	SPI0_SI	GPIO34	USRCLK1	SQI_SIO[1]
A56	IF0.3	D	I/O	PU	VDDIO0	SPI0_SO	GPIO35	USRCLK2	SQI_SIO[0]
A47	IF1.0	D	I/O	PU	VDDIO0	SPI1_CLK	GPIO36	PCM_CLK	-
B39	IF1.1	D	I/O	PU	VDDIO0	SPI1_CS	GPIO37	PCM_FR	-
A52	IF1.2	D	I/O	PU	VDDIO0	SPI1_SI	GPIO38	PCM_SI	-
B45	IF1.3	D	I/O	PU	VDDIO0	SPI1_SO	GPIO39	PCM_SO	-
B48	IF2.0	D	I/O	PU	VDDIO0	UART0_TX	GPIO40	-	-
A49	IF2.1	D	I/O	PU	VDDIO0	UART0_RX	GPIO41	-	-
B41	IF3.0	D	I/O	PU	VDDIO0	UART1_TX	GPIO42	SQI_SIO[2]	-
A54	IF3.1	D	I/O	PU	VDDIO0	UART1_RX	GPIO43	SQI_SIO[3]	-
A2	IF4.0	М	I/O	PD	VDDIO1	GPIO0	COM0	-	-
A1	IF4.1	М	I/O	PD	VDDIO1	GPIO1	COM1	-	-
B1	IF4.2	М	I/O	PD	VDDIO1	GPIO2	COM2	-	-
A76	IF4.3	М	I/O	PD	VDDIO1	GPIO3	COM3	-	-
B64	IF4.4	М	I/O	PD	VDDIO1	GPIO4	SEG0	-	-
A75	IF4.5	М	I/O	PD	VDDIO1	GPIO5	SEG1	-	-
B63	IF4.6	М	I/O	PD	VDDIO1	GPIO6	SEG2	-	-
A74	IF4.7	М	I/O	PD	VDDIO1	GPIO7	SEG3	-	-
A72	IF4.8	М	I/O	PD	VDDIO1	GPIO8	SEG4	-	-
B61	IF4.9	М	I/O	PD	VDDIO1	GPIO9	SEG5	-	-
B60	IF4.10	М	I/O	PD	VDDIO1	GPIO10	SEG6	-	-
A70	IF4.11	М	I/O	PD	VDDIO1	GPIO11	SEG7	-	-
B59	IF4.12	М	I/O	PD	VDDIO1	GPIO12	SEG8	-	-
A69	IF4.13	М	I/O	PD	VDDIO1	GPIO13	SEG9	-	-
B58	IF4.14	М	I/O	PD	VDDIO1	GPIO14	SEG10	-	-
A68	IF4.15	М	I/O	PD	VDDIO1	GPIO15	SEG11	-	-
B57	IF4.16	М	I/O	PD	VDDIO1	GPIO16	SEG12	-	-
A67	IF4.17	М	I/O	PD	VDDIO1	GPIO17	SEG13	-	-
B56	IF4.18	М	I/O	PD	VDDIO1	GPIO18	SEG14	-	-
A66	IF4.19	М	I/O	PD	VDDIO1	GPIO19	SEG15	-	-
B55	IF4.20	М	I/O	PD	VDDIO1	GPIO20	SEG16	-	-
A65	IF4.21	М	I/O	PD	VDDIO1	GPIO21	SEG17	-	-

Types: D – Digital, M – Mixed signal, A – Analog, S – Supply
 Direction: I – Input, O – Output, I/O – Input or Output
 PU – Pull-up, PD – Pull-down. Most Pull-up and Pull-downs may be disconnected in firmware
 Primary function is the power-on default. Alternate functions may be selected in firmware
 TEST must be connected to VSS for proper device operation

6. All pins with the same name must be shorted together for proper device operation7. IF5.0 can be used as an analog external input to programmable gain amplifiers

Pin				Dull up /		Function			
140 TLLGA	Pin Name (Note 6)	Type (Note 1)	Direction (Note 2)	Pull-Down (Note 3)	Pin Power Supply	Primary (Note 4)	Alternate 1	Alternate 2	Alternate 3
A64	IF4.22	М	I/O	PD	VDDIO1	GPIO22	SEG18	-	-
A63	IF4.23	М	I/O	PD	VDDIO1	GPIO23	SEG19	-	-
B53	IF4.24	М	I/O	PD	VDDIO1	GPIO24	SEG20	PWM0	-
A62	IF4.25	М	I/O	PD	VDDIO1	GPIO25	SEG21	PWM1	-
B52	IF4.26	М	I/O	PD	VDDIO1	GPIO26	SEG22	PWM2	-
A61	IF4.27	М	I/O	PD	VDDIO1	GPIO27	SEG23	PWM3	-
B51	IF4.28	М	I/O	PD	VDDIO1	GPIO28	SEG24	-	-
A60	IF4.29	М	I/O	PD	VDDIO1	GPIO29	SEG25	-	-
B50	IF4.30	М	I/O	PD	VDDIO1	GPIO30	SEG26	-	-
A59	IF4.31	М	I/O	PD	VDDIO1	GPIO31	SEG27	-	-
B47	NMI	D	I	PD	VDDIO0	NMI	-	-	-
A12	IF5.0 (Note 7)	М	I/O	PU	VBATA	WAKEUP0	GPIO44	-	-
B10	IF5.1	D	I/O	PU	VBATA	GPIO45	WAKEUP1	-	-
A11	IF5.2	D	I/O	PD	VBATA	GPIO46	WAKEUP2	-	_
B9	IF5.3	D	I/O	PD	VBATA	GPIO47	WAKEUP3	-	-
B42	RSTB	D	I	PU	VDDIO0	RSTB	-	-	-
B38	JTDI	D	I	PD	VDDIO0	JTDI	-	-	-
B40	JTDO	D	0	-	VDDIO0	JTDO	-	-	-
A46	JTMS	D	I	PU	VDDIO0	JTMS	-	-	-
A55	JTCK	D	I		VDDIO0	JTCK	-	-	-
A45	JRSTB	D	I	PU	VDDIO0	JRSTB	-	-	-
A20	DAC0	А	0	-	VBATA	DAC0	-	-	-
A21	DAC1	А	0	-	VBATA	DAC1	-	-	-
B18	DAC2	А	0	-	VBATA	DAC2	-	-	-
A29	AUX_IN0	А	I	-	VBATA	AUX_IN0	-	-	-
B24	AUX_IN1	А	I	-	VBATA	AUX_IN1	-	-	-
A23	AUX_IN2	А	I	-	VBATA	AUX_IN2	-	-	-
A37	AAF0	А	I/O	-	VBATA	AAF0	-	-	-
B32	AAF1	А	I/O	-	VBATA	AAF1	-	-	-
B17	MSW0_A	А	I/O	-	VBATA	MSW0_A	-	-	-
B16	MSW0_B	А	I/O	-	VBATA	MSW0_B	-	-	-
A19	MSW0_C	А	I/O	-	VBATA	MSW0_C	-	-	-
A18	MSW1_A	А	I/O	-	VBATA	MSW1_A	-	-	-
A17	MSW1_B	A	I/O	-	VBATA	MSW1_B	-	-	-
B15	MSW1_C	А	I/O	-	VBATA	MSW1_C	-	-	-
B14	MSW2_A	А	I/O	-	VBATA	MSW2_A	-	-	-
B13	MSW2_B	А	I/O	-	VBATA	MSW2_B	-	-	_

Types: D – Digital, M – Mixed signal, A – Analog, S – Supply
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 PU – Pull–up, PD – Pull–down. Most Pull–up and Pull–downs may be disconnected in firmware
 Primary function is the power-on default. Alternate functions may be selected in firmware
 TEST must be connected to VSS for proper device operation
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 All pins with the same name must be shorted together for proper device operation

7. IF5.0 can be used as an analog external input to programmable gain amplifiers

Pin				Dull un (		Function			
140 TLLGA	Pin Name (Note 6)	Type (Note 1)	Direction (Note 2)	Pull-Down (Note 3)	Pin Power Supply	Primary (Note 4)	Alternate 1	Alternate 2	Alternate 3
A16	MSW2_C	А	I/O	-	VBATA	MSW2_C	-	-	-
A15	MSW3_A	А	I/O	-	VBATA	MSW3_A	-	-	-
B12	MSW3_B	А	I/O	-	VBATA	MSW3_B	-	-	-
A14	MSW3_C	А	I/O	-	VBATA	MSW3_C	-	-	-
A58	NC	-	-	-	-	NC	-	-	-
A8	VDBL	S	0	-	-	VDBL	-	-	-
A10	VBATA	S	I	-	-	VBATA	-	-	-
B20	VBATA	S	I	-	-	VBATA	-	-	-
A73	VBATA	S	I	-	-	VBAT	-	-	-
B62	VDDD	S	0	-	-	VDDD	-	-	-
A7	ILV	A	I/O	-	VLCD	ILV	-	-	-
A44	VDDIO0	S	I	-	-	VDDIO0	-	-	-
B37	VDDIO0	S	I	-	-	VDDIO0	-	-	-
A50	VDDIO0	S	I	-	-	VDDIO0	-	-	-
B43	VDDIO0	S	I	-	-	VDDIO0	-	-	-
B3	VDDIO1	S	I	-	-	VDDIO1	-	-	-
B49	VDDIO1	S	I	-	-	VDDIO1	-	-	-
B54	VDDIO1	S	I	-	-	VDDIO1	-	-	-
A71	VDDIO1	S	I	-	-	VDDIO1	-	-	-
A4	VDDUSB	S	I	-	-	VDDUSB	-	-	-
A38	VREF	S	0	-	-	VREF	-	-	-
A13	IREF	S	0	-	-	IREF	-	-	-
A39	VADC	S	0	-	-	VADC	-	-	-
B6	VLCD0	A	0	-	VLCD	VLCD0	-	-	-
A6	VLCD1	А	0	-	VLCD	VLCD1	-	-	-
B5	VLCD	S	I	-	-	VLCD	-	-	-
B8	CP0	Α	0	-	VLCD	CP0	-	-	-
B7	CP1	Α	0	-	VLCD	CP1	-	-	-
A9	VCP	S	0	-	-	VCP	-	-	-
B2	USBXTAL0	А	I/O	-	VDDIO1	USBXTAL0	-	-	-
A3	USBXTAL1	А	I/O	-	VDDIO1	USBXTAL1	-	-	-
B19	RTCXTAL0	Α	I/O	-	VBAT	RTCXTAL0	-	-	-
A22	RTCXTAL1	Α	I/O	-	VBAT	RTCXTAL1	-	-	-
B46	EXTCLK	D	I/O	-	VDDI00	EXTCLK	-	-	-
B25	ALT0	A	I/O	-	VBATA	ALT0	-	-	-
A30	ALT1	A	I/O	-	VBATA	ALT1	-	-	-
A31	A0_IN0	Α	I/O	-	VBATA	A0_IN0	-	-	-
B26	A0_IN1	А	I/O	-	VBATA	A0_IN1	-	-	-

Types: D – Digital, M – Mixed signal, A – Analog, S – Supply
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7. IF5.0 can be used as an analog external input to programmable gain amplifiers

Pin				Dull up /		Function			
140 TLLGA	Pin Name (Note 6)	Type (Note 1)	Direction (Note 2)	Pull-Down (Note 3)	Pin Power Supply	Primary (Note 4)	Alternate 1	Alternate 2	Alternate 3
A32	A0_IN2	А	I/O	-	VBATA	A0_IN2	-	-	-
B27	A0_IN3	А	I/O	-	VBATA	A0_IN3	-	-	-
A33	A0_IN4	А	I/O	-	VBATA	A0_IN4	-	-	-
B28	A0_IN5	А	I/O	-	VBATA	A0_IN5	-	-	-
A34	A0_IN6	А	I/O	-	VBATA	A0_IN6	-	-	-
B29	A0_IN7	А	I/O	-	VBATA	A0_IN7	-	-	-
A35	A0_IN	А	ļ	-	VBATA	A0_IN	-	-	-
A28	A1_IN	А	I	-	VBATA	A1_IN	-	-	-
A26	A2_IN	А	ļ	-	VBATA	A2_IN	-	-	-
B30	A0_REF	А	I	-	VBATA	A0_REF	-	-	-
B22	A1_REF	А	I	-	VBATA	A1_REF	-	-	-
A24	A2_REF	А	ļ	-	VBATA	A2_REF	-	-	-
B31	A0_OUTA	А	0	-	VBATA	A0_OUTA	-	-	-
A36	A0_OUTB	А	0	-	VBATA	A0_OUTB	-	-	-
B23	A1_OUTA	А	0	-	VBATA	A1_OUTA	-	-	-
A27	A1_OUTB	А	0	-	VBATA	A1_OUTB	-	-	-
B21	A2_OUTA	А	0	-	VBATA	A2_OUTA	-	-	-
A25	A2_OUTB	А	0	-	VBATA	A2_OUTB	-	-	-
A43	SPST0_A	А	I/O	-	VBATA	SPST0_A	-	-	-
B36	SPST0_B	А	I/O	-	VBATA	SPST0_B	-	-	-
A42	SPST1_A	А	I/O	-	VBATA	SPST1_A	-	-	-
B35	SPST1_B	А	I/O	-	VBATA	SPST1_B	-	-	-
A41	SPST2_A	А	I/O	-	VBATA	SPST2_A	-	-	-
B34	SPST2_B	А	I/O	-	VBATA	SPST2_B	-	-	-
A40	SPST3_A	А	I/O	-	VBATA	SPST3_A	-	-	-
B33	SPST3_B	A	I/O	-	VBATA	SPST3_B	-	-	-
B11	TEST (Note 5)	A	I	-	-	TEST (connect to VSS)	-	-	-
Thermal	VSS	S	-	-	-	VSS	-	-	_

Types: D – Digital, M – Mixed signal, A – Analog, S – Supply
 Direction: I – Input, O – Output, I/O – Input or Output
 PU – Pull-up, PD – Pull-down. Most Pull-up and Pull-downs may be disconnected in firmware

4. Primary function is the power-on default. Alternate functions may be selected in firmware

TEST must be connected to VSS for proper device operation
 All pins with the same name must be shorted together for proper device operation

7. IF5.0 can be used as an analog external input to programmable gain amplifiers

#### Table 2. DETAILED PIN DESCRIPTIONS

Pin Name	Description
USBDP	USB interface positive terminal
USBDN	USB interface negative terminal
SCL	I <sup>2</sup> C interface clock
SDA	I <sup>2</sup> C interface data
IF0.0	Primary SPI interface clock / General purpose I/O
IF0.1	Primary SPI interface chip select / General purpose I/O / User clock output
IF0.2	Primary SPI interface data input / General purpose I/O / User clock output / SQI serial I/O 1
IF0.3	Primary SPI interface data output / General purpose I/O / User clock output / SQI serial I/O 0
IF1.0	Secondary SPI interface clock line / General purpose I/O / PCM interface clock
IF1.1	Secondary SPI interface chip select / General purpose I/O / PCM interface frame
IF1.2	Secondary SPI interface data input / General purpose I/O / PCM interface data input
IF1.3	Secondary SPI interface data output / General purpose I/O / PCM interface data output
IF2.0	Primary UART transmit line / General purpose I/O
IF2.1	Primary UART receive line / General purpose I/O
IF3.0	Secondary UART transmit line / General purpose I/O / SQI serial I/O 2
IF3.1	Secondary UART receive line / General purpose I/O / SQI serial I/O 3
IF4.0	LCD backplane drive output (COM0) / General purpose I/O
IF4.1	LCD backplane drive output (COM1) / General purpose I/O
IF4.2	LCD backplane drive output (COM2) / General purpose I/O
IF4.3	LCD backplane drive output (COM3) / General purpose I/O
IF4.4	LCD segment output / General purpose I/O
IF4.5	LCD segment output / General purpose I/O
IF4.6	LCD segment output / General purpose I/O
IF4.7	LCD segment output / General purpose I/O
IF4.8	LCD segment output / General purpose I/O
IF4.9	LCD segment output / General purpose I/O
IF4.10	LCD segment output / General purpose I/O
IF4.11	LCD segment output / General purpose I/O
IF4.12	LCD segment output / General purpose I/O
IF4.13	LCD segment output / General purpose I/O
IF4.14	LCD segment output / General purpose I/O
IF4.15	LCD segment output / General purpose I/O
IF4.16	LCD segment output / General purpose I/O
IF4.17	LCD segment output / General purpose I/O
IF4.18	LCD segment output / General purpose I/O
IF4.19	LCD segment output / General purpose I/O
IF4.20	LCD segment output / General purpose I/O
IF4.21	LCD segment output / General purpose I/O
IF4.22	LCD segment output / General purpose I/O
IF4.23	LCD segment output / General purpose I/O
IF4.24	LCD segment output / General purpose I/O / Pulse-Width Modulator 0 output
IF4.25	LCD segment output / General purpose I/O / Pulse-Width Modulator 1 output
IF4.26	LCD segment output / General purpose I/O / Pulse-Width Modulator 2 output
IF4.27	LCD segment output / General purpose I/O / Pulse-Width Modulator 3 output

#### Table 2. DETAILED PIN DESCRIPTIONS

Pin Name	Description
IF4.28	LCD segment output / General purpose I/O
IF4.29	LCD segment output / General purpose I/O
IF4.30	LCD segment output / General purpose I/O
IF4.31	LCD segment output / General purpose I/O
NMI	Non-maskable interrupt
IF5.0	Wakeup input 0, Falling Edge / General purpose I/O / External signal to programmable gain amplifiers
IF5.1	Wakeup input 1, Falling Edge / General purpose I/O
IF5.2	Wakeup input 2, Rising Edge / General purpose I/O
IF5.3	Wakeup input 3 Rising Edge / General purpose I/O
RSTB	Reset input
JTDI	JTAG data input
JTDO	JTAG data output
JTMS	JTAG mode select
JTCK	JTAG clock
JRSTB	JTAG reset
DAC0	Digital-to-Analog Converter 0 output
DAC1	Digital-to-Analog Converter 1 output
DAC2	Digital-to-Analog Converter 2 output
AUX_IN0	Auxiliary Input 0 – External signal input to programmable gain amplifiers
AUX_IN1	Auxiliary Input 1 – External signal input to programmable gain amplifiers
AUX_IN2	Auxiliary Input 2 – External signal input to programmable gain amplifiers
AAF0	External capacitor filter node for programmable gain amplifier 0 (Anti-aliasing)
AAF1	External capacitor filter node for programmable gain amplifier 1 (Anti-aliasing)
MSW0_A	Multi-switch 0 A terminal
MSW0_B	Multi-switch 0 B terminal
MSW0_C	Multi-switch 0 Common terminal
MSW1_A	Multi-switch 1A terminal
MSW1_B	Multi-switch 1 B terminal
MSW1_C	Multi-switch 1 Common terminal
MSW2_A	Multi-switch 2 A terminal
MSW2_B	Multi-switch 2 B terminal
MSW2_C	Multi-switch 2 Common terminal
MSW3_A	Multi-switch 3 A terminal
MSW3_B	Multi-switch 3 B terminal
MSW3_C	Multi-switch 3 Common terminal
VDBL	Output voltage from on-chip charge pump; filtering capacitor required
VBATA	Main power supply input (analog)
VBAT	Main power supply input (digital and related support blocks)
VCP	Output voltage from charge pump regulator; filtering capacitor required
VDDD	Output voltage from digital supply regulator; filtering capacitor required
ILV	Programmable current sink for LED backlight drive and intensity trimming
VDDIO0	Power supply input for digital I/O pins, excluding IF4
VDDIO1	Power supply input for IF4 mixed-signal LCD I/O pins
VREF	Output voltage from on-chip precision voltage reference; filtering capacitor required

#### Table 2. DETAILED PIN DESCRIPTIONS

Pin Name	Description
IREF	Output current from on-chip current reference; reference resistor (300 k $\Omega$ , low-TC) required
VADC	Output voltage from ADC power supply regulator; filtering capacitor required
VLCD0	Output voltage from LCD driver (33%); filtering capacitor required
VLCD1	Output voltage from LCD driver (66%); filtering capacitor required
VLCD	Power supply input for LCD and backlight current driver
CP0	Charge pump flyback capacitor connection
CP1	Charge pump flyback capacitor connection
VSS	Ground pin in the center of the package
USBXTAL0	48 MHz USB crystal connection
USBXTAL1	48 MHz USB crystal connection
RTCXTAL0	32.768 kHz real-time-clock crystal connection
RTCXTAL1	32.768 kHz real-time-clock crystal connection
EXTCLK	External clock I/O
ALT0	Sensor Interface 3:1 MUX Common terminal (Connection to A0_IN0, A0_IN1, A0_IN2)
ALT1	Sensor Interface 5:1 MUX Common terminal (Connection to A0_IN3, A0_IN4, A0_IN5, A0_IN6, A0_IN7)
A0_IN0	Sensor Interface 8:1 MUX 0 terminal
A0_IN1	Sensor Interface 8:1 MUX 1 terminal
A0_IN2	Sensor Interface 8:1 MUX 2 terminal
A0_IN3	Sensor Interface 8:1 MUX 3 terminal
A0_IN4	Sensor Interface 8:1 MUX 4 terminal
A0_IN5	Sensor Interface 8:1 MUX 5 terminal
A0_IN6	Sensor Interface 8:1 MUX 6 terminal
A0_IN7	Sensor Interface 8:1 MUX 7 terminal
A0_IN	Opamp A0 negative input terminal (common terminal for Sensor Interface 8:1 MUX)
A1_IN	Opamp A1 negative input terminal
A2_IN	Opamp A2 negative input terminal
A0_REF	Opamp A0 positive input terminal
A1_REF	Opamp A1 positive input terminal
A2_REF	Opamp A2 positive input terminal
A0_OUTA	Opamp A0 output (primary)
A0_OUTB	Opamp A0 output (secondary)
A1_OUTA	Opamp A1 output (primary)
A1_OUTB	Opamp A1 output (secondary)
A2_OUTA	Opamp A2 output (primary)
A2_OUTB	Opamp A2 output (secondary)
SPST0_A	Single-pole single-throw switch 0 A terminal
SPST0_B	Single-pole single-throw switch 0 B terminal
SPST1_A	Single-pole single-throw switch 1 A terminal
SPST1_B	Single-pole single-throw switch 1 B terminal
SPST2_A	Single-pole single-throw switch 2 A terminal
SPST2_B	Single-pole single-throw switch 2 B terminal
SPST3_A	Single-pole single-throw switch 3 A terminal
SPST3_B	Single-pole single-throw switch 3 B terminal
TEST	Test input; Short to VSS required

#### **Pin Connections**

The following table describes the required and recommended external connections and components. These connections and components are required to ensure proper device operation and performance.

Pin	External Connection or Component	Recommended Value
VDDD	Power supply filtering capacitor	C = 22 μF
VCPLDO	Power supply filtering capacitor	C = 22 μF
AAF0	Anti-aliasing filtering capacitor	C = 1 μF (for 160–320 Hz cut–off range)
AAF1	Anti-aliasing filtering capacitor	C = 1 $\mu$ F (for 160–320 Hz cut–off range)
VDBL	Power supply filtering capacitor	C = 10 μF
VBATA	Battery supply filtering capacitor	C = 22 μF
VBAT	Battery supply filtering capacitor	C = 22 μF
CP0, CP1	Charge pump capacitor between CP0, CP1	C = 1 μF
VDDIO0	I/O supply filtering capacitor	C = 22 μF
VDDIO1	I/O supply filtering capacitor	C = 22 μF
VDDUSB	Battery supply filtering capacitor	C = 10 μF
RTCXTAL0, RTCXTAL1	Crystal for real-time clock (No capacitors required)	f = 32768 Hz, C = 9 pF, ESR = 70 k $\Omega$
USBXTAL0, USBXTAL1	Crystal for USB (No capacitors required)	f = 48.0 MHz, C = 10 pF, ESR = 70 $\Omega$
VREF	Power supply filtering capacitor	C = 22 μF
IREF	Current reference resistor	R = 300 kΩ (± 1%,  TC  < 100 ppm/C)
VADC	Power supply filtering capacitor	C = 22 μF
VLCD	Power supply filtering capacitor	C = 1 μF
VLCD1	LCD driver voltage filtering capacitor	C = 1 nF
VLCD0	LCD driver voltage filtering capacitor	C = 1 nF
NMI	Test point recommended	
TEST	Test pin must be connected to VSS	
Thermal	Thermal must be connected to battery VSS	
USBDP, USBDN	ESD protection for USB bus	P/N = ON Semiconductor NUP2201MR6T1G

#### Table 3. REQUIRED AND RECOMMENDED EXTERNAL CONNECTIONS AND COMPONENTS

#### Table 4. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Input voltage on any digital pin		-0.3	3.6	V
Input voltage on any analog pin		-0.3	3.6	V
Input voltage on any supply pin		-0.3	3.6	V
Current on any digital pin			± 5	mA
Current on any analog pin			± 10	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### Table 5. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Units
Power supply applied to VBAT	VBAT	1.8	3.3	3.5	V
Power supply applied to VBATA	VBATA	2.2	3.3	3.5	V
Internal oscillator clock frequency		1		16	MHz
Externally supplied clock frequency				16	MHz
Ambient Operating temperature range	Та	0		50	°C
Junction temperature range	Tj	0		75	°C
Opamp differential mode voltage				± 5	mV

#### Table 6. ESD AND LATCH-UP CHARACTERISTICS

Parameter		Max	Units	
ESD – Human Body Model (Note 8)		VBAT pin	1250	V
	JEDEC JS-001-2010	SPST[0:3], MSW[0:2] pins	1500	
		all other pins	3000	
ESD – Charged Device Model (Note 8)	JESD2	750	V	
ESD – Machine Model (Note 8)	JESE2	250	V	
Latch-up (Note 8)	JEDEC	C STD-78, all pins	± 100	mA

8. Characteristics are obtained through device qualification and characterization and not tested in production

#### **ELECTRICAL CHARACTERISTICS**

#### **Test Conditions**

#### **Typical Values**

Unless otherwise noted, Typ values specify the typical values based on design and characterization data under normal operating conditions. Normal operating conditions include a supply voltage (VBAT and VBATA) of 3.3 V and an operating temperature of 25°C. For specific blocks the details of the normal operation conditions are described in their respective sections.

#### **Minimum and Maximum Values**

Unless otherwise noted, for range parameters, Min and Max values specify the designed range or measurement range and are guaranteed by design and/or characterization. Range parameters include the term "Range" in their name.

For non-range parameters, the Min and Max values specified may be based on factory production test limits, design, or characterization data. Production test limits are specified for typical temperature and supply voltage only.

#### **Temperature Range**

A • in the Conditions field for any parameter denotes characterized over the complete operating temperature range. The Typ values listed for those parameters are guaranteed by design and/or characterization over the complete range. If present, the Min and Max values for • parameters may be based on factory production test limits, design, or characterization data.

For more information related to the performance of the device across the operating temperature range refer to the Typical Operating Conditions plots.

#### **Normal Operating Conditions**

Unless otherwise noted, normal operating conditions indicate an ambient temperature Ta =  $25^{\circ}$ C and a supply voltage VBAT = VBATA = 3.3 V. VDDD, VADC, VREF, and the Internal Oscillator are calibrated to their preset factory calibration settings and correspond to their respective Typ values. VDDIO0 and VDDIO1 are powered externally from the VDDD Digital Supply Regulator. No external loads are applied to digital I/O or analog pins. The power supply for normal operating conditions is shown in Figure 3.



Figure 3. Normal Operating Condition Configuration

Symbol	Description	Value
C <sub>VREF</sub>	VREF filtering capacitor	22 μF
C <sub>VDDD</sub>	VDDD regulator filtering capacitor	22 μF
C <sub>VADC</sub>	VADC regulator filtering capacitor	10 μF
C <sub>VBAT</sub>	Supply filtering capacitor	22 μF
USB_XTAL	Crystal for USB	48 MHz
RTC_XTAL	Crystal for RTC	32.768 kHz
R <sub>IREF</sub>	Resistor for current reference	300 kΩ

#### Table 7. NORMAL OPERATION CONFIGURATION

**Table 8. SYSTEM** (Typical operating conditions (Ta =  $25^{\circ}$ C, VBAT = VBATA = 3.3 V, VDDIO0 = VDDIO1 = VDDD, 16-bit/32-bit mixed instructions, 66% execution from flash memory, data access from SRAM, sensor interface disabled, peripherals disabled) unless otherwise noted. • denotes characterized over complete temperature range. Current consumption for individual blocks may be found in their respective sections.)

Parameter	Symbol	Conditio	ons	Min	Тур	Max	Units
DC ELECTRICAL CHARACTERISTICS						-	
Main Supply Voltage Range (Note 9)	VBAT			1.8		3.6	V
Analog Supply Voltage Range (Note 10)	VBATA			2.2		3.6	V
USB Supply Voltage Range	VDDUSB			3.0		3.3	V
I/O Supply Voltage Range (Notes 11, 12)	VDDIO0, VDDIO1			1.8		3.6	V
LCD Supply Voltage Range (Note 13)	VLCD			1.8		3.6	V
Run Mode Current (Note 14)	IBAT	Typical application,	1 MHz		0.8		mA
	execution from flash, analog dis- abled	execution from flash, analog dis- abled	2 MHz		1.2		1
			4 MHz		2.1		1
			8 MHz		3.8		1
		16 MHz		7.0		1	
		Typical application,	1 MHz		0.7		1
		execution from SRAM	2 MHz		1.0		1
			4 MHz		1.7		1
			8 MHz		3.0		1
			16 MHz		5.6		1
Standby Mode Current		RTC enable	d		26		μΑ
Sleep Mode Current		RTC enable	d		0.75		μA
	RTC disabled		ed		0.15		1

9. VBAT powers the VDDD regulator (for the digital core, peripherals, internal oscillator), VCP regulator (for the charge-pump)

10. VBATA powers the VADC regulator, VREF, sensor interface, analog pins, and IF5 pins (wakeup)

11. VDDIO0 powers I<sup>2</sup>C (SCL, ŠDA), IF0, IF1, IF2, IF3, NMI, RSTB, EXTCLK, JTAG

12. VDDIO1 powers IF4

13. VLCD powers VLCD0, VLCD1, ILV

14. The current consumption in run mode depends on the complexity of the application (i.e. the number of memory accesses, type of instruction (16-bit or 32-bit), program and data storage in flash or SRAM).

 

 Table 9. DIGITAL I/O PINS (IF0, IF1, IF2, IF3, JTAG, EXTCLK, RSTB, NMI, SCL, SDA)

 (Typical operating conditions (Ta = 25°C, VDDIO0 = VDDD, Pull-up/Pull-down Enabled) unless otherwise noted. • denotes characterized

 over complete temperature range.)

Parameter	Symbol		Conditions			Тур	Max	Units
DC ELECTRICAL CHARACT	ERISTICS							
VDDIO0 Supply Voltage Range (Note 15)	VDDIO0				1.8		3.6	V
Output Low Level	V <sub>ol</sub>	ار	<sub>ol</sub> = 4 mA				0.2 x VDDIO0	V
Output High Level	V <sub>oh</sub>	$I_{ol} = -4 \text{ mA}$			0.8 x VDDIO0			V
Input Low Level	V <sub>il</sub>						0.2 x VDDIO0	V
Input High Level	V <sub>ih</sub>				0.8 x VDDIO0			V
Pull-up Resistance	R <sub>pu</sub>	Non-I <sup>2</sup> C	VDDIO0 = 1.8 V			102		kΩ
			VDDIO0 = 3.3 V		34	48	74	
		l <sup>2</sup> C	VDDIO0 = 1.8 V			1		
			VDDIO0 = 3.3 V			1		
Pull-down Resistance	R <sub>pd</sub>	VDD	IO0 = 1.8 V			102		kΩ
		VDD	IO0 = 3.3 V		34	55	75	
Pin Capacitance	Cp					5		pF
Maximum Output Current	I <sub>ol</sub> , I <sub>oh</sub>						± 4	mA
Input Leakage Current	lı						± 1	μA

15. Supply voltage may be lower during Standby Mode if VDDIO0 is connected to VDDD

 Table 10. LCD I/O PINS (IF4) (Typical operating conditions ( $T_a = 25^{\circ}C$ , VDDIO1 = VBAT, GPIO Mode, Pull-up / Pull-down Enabled) unless otherwise noted.
 • denotes characterized over complete temperature range.)

Parameter	Symbol	Conditions	Min	Тур	Max	Units
DC ELECTRICAL CHARACTERIS	TICS					
VDDIO1 Supply Voltage Range	VDDIO1	GPIO Mode	1.8		3.6	V
(Note 16)		LCD Mode	VLCD		3.6	
Output Low Level	V <sub>ol</sub>	I <sub>ol</sub> = 4 mA			0.2 x VDDIO1	V
Output High Level	V <sub>oh</sub>	I <sub>ol</sub> = -4 mA	0.8 x VDDIO1			V
Input Low Level	V <sub>il</sub>				0.2 x VDDIO1	V
Input High Level	V <sub>ih</sub>		0.8 x VDDIO1			V
Pull-down Resistance	R <sub>pd</sub>	VDDIO1 = 1.8 V		138		kΩ
		VDDIO1 = 3.3 V	34	54	75	
Pin Capacitance	Cp			5		pF
Maximum current					± 4	mA

16. Supply voltage may be lower during Standby Mode if VDDIO1 is connected to VDDD

Table 11. WAKEUP I/O PINS (IF5) (Typical operating conditions (Ta = 25°C, Pull-up / Pull-down Enabled, GPIO mode) unless
otherwise noted. • denotes characterized over complete temperature range.)

Parameter	Symbol	Conditions	Min	Тур	Max	Units
DC ELECTRICAL CHARACTERISTICS	S					
IF5 Supply Voltage Range (Note 17)	VBATA		1.8		3.6	V
Output Low Level	V <sub>ol</sub>	I <sub>ol</sub> = 4 mA			0.2 x VBATA	V
Output High Level	V <sub>oh</sub>	I <sub>ol</sub> = -4 mA	0.7 x VBATA			V
Input Low Level	V <sub>il</sub>				0.2 x VBATA	V
Input High Level	V <sub>ih</sub>		0.7 x VBATA			V
Wakeup Threshold (Note 18)		For IF5.0, IF5.1			0.2 x VBATA	V
		For IF5.2, IF5.3	0.2 x VBATA			
Pull-up Resistance	R <sub>pu</sub>	VBATA = 1.8 V		102		kΩ
		VBATA = 3.3 V		42		
Pull-down Resistance	R <sub>pd</sub>	VBATA = 1.8 V		140		kΩ
		VBATA = 3.3 V	34	54	75	
Pin Capacitance	Cp			5		pF
Maximum current					± 4	mA

17.IF5 Wakeup pins are powered from VBATA 18.Wakeup condition for IF5.0, IF5.1 is falling edge. Wakeup condition for IF5.2, IF5.3 is rising edge. Specified threshold indicates the maximum and minimum levels for the falling and rising edge final voltages, respectively

Table 12. USB I/O (USBD+, USBD-) (Typical operating conditions (Ta = 25°C, Full-speed Mode, VDDUSB = 3.3 V) unless otherwise noted. • denotes over complete temperature.)

Parameter	Symbol	Conditions	Min	Тур	Max	Units
DC & AC ELECTRICAL CHARAC	TERISTICS					
USB Supply Voltage	VDDUSB		3.0		3.6	V
Supply Current		Standby		0.5		μΑ
		Operating		450		
Output Low Level	V <sub>ol</sub>				0.3	V
Output High Level	V <sub>oh</sub>		2.8			V
Input Low Level	V <sub>il</sub>				0.8	V
Input High Level	V <sub>ih</sub>		2.0			V
External Pull-up Resistance (Note 19)			1.425		1.575	kΩ
Termination voltage for Pull-up			3.0		3.6	V
Slew Rate (Note 19)	T <sub>fr</sub>	Rise time, C <sub>I</sub> = 50 pF	4		20	ns
	T <sub>ff</sub>	Fall time, C <sub>l</sub> = 50 pF	4		20	
Slew Rate Matching	T <sub>frff</sub>	$T_{frff} = T_{fr}/T_{ff}$	90		111	%
Pin Capacitance	Cp				20	pF

19. External pull-up to 3.3 V is required on D+ to enumerate as a USB 2.0 Full-speed device

#### Table 13. FLASH MEMORY

(Typical operating conditions (Ta =  $25^{\circ}$ C) unless otherwise noted. All parameters in this section are obtained through qualification and characterization and are not tested in production • denotes characterized over complete temperature range.)

Parameter	Symbol	Conditions		Min	Тур	Max	Units
DC ELECTRICAL CHARACTERIS	DC ELECTRICAL CHARACTERISTICS						
Supply Voltage	VBAT			1.8		3.6	V
Write Endurance		On-chip ECC disabled		20000			cycles
Data Retention				100			years
Programming Time (per word)					20		μs
Erase Time		Single page		20			ms
		Entire array (Note 20)		20			

20. Erase time for the entire array is through the Mass Erase operation

#### Table 14. SPI

Parameter	Symbol	Conditions		Min	Тур	Max	Units
SPI clock frequency		Master mode/Slave mode				8.0	MHz
SPI clock rise and fall time					10		ns
Data input setup time		Master mode/Slave mode		5			ns
Data input hold time		Master mode/Slave mode		5			ns
Data output access time		Slave mode				50	ns
Data output disable time		Slave mode		10			ns
Data output valid time		Slave mode (after SPI_CLK edge)				20	ns
Data output valid time		Master mode (after SPI_CLK edge)				5	ns
Data output hold time		Slave mode (after SPI_CLK edge)		25			ns
Data output hold time		Master mode (after SPI_CLK edge)		10			ns

#### Table 15. I<sup>2</sup>C

Parameter	Symbol	Conditions	Min	Тур	Max	Units
SCL low time			5			μs
SCL high time			5			μs
SDA setup time			250			ns
SDA and SCL rise time					1000	ns
SDA and SCL fall time					300	ns
Start condition hold time			4			μs

#### Table 16. PCM

Parameter	Symbol	Conditions		Min	Тур	Max	Units
PCM_CLK						16	MHz
PCM_SI setup time		Before PCM_CLK edge		10			ns
PCM_SI hold time		After PCM_CLK edge		10			ns
PCM_SO data valid time		After PCM_CLK edge				50	ns

Table 17. LCD (IF4, VLCD1, VLCD0, ILV) (Typical operating conditions (Ta = 25°C, VBATA = 3.3 V, VLCD = VDDIO1 = 3.5 V).	
unless otherwise noted. • denotes characterized over complete temperature range.)	

Parameter	Symbol	Conditions	Min	Тур	Max	Units						
DC & AC ELECTRICAL CHARACTERISTICS												
Supply Voltage	VDDIO1, VLCD		1.8		3.6	V						
LCD Driving Voltage		LCD Driving Voltage 0	VSS			V						
		LCD Driving Voltage 1		0.33 x VLCD		1						
		LCD Driving Voltage 2		0.66 x VLCD		1						
		LCD Driving Voltage 3			VLCD							
LCD Driving Voltage Temperature Drift				< 6		ppm/°C						
LCD Backlight Current	Ι <sub>Ιν</sub>	Disabled		0.0	± 0.001	mA						
		Setting = 1 x I <sub>nom</sub>		1.1								
		Setting = 2 x I <sub>nom</sub>		2.2								
		Setting = 3 x I <sub>nom</sub>		3.3								
		Setting = 4 x I <sub>nom</sub>		4.4								
		Setting = 5 x I <sub>nom</sub>		5.4								
		Setting = 6 x I <sub>nom</sub>		6.4								
		Setting = 7 x I <sub>nom</sub>		7.4								
		Setting = 8 x I <sub>nom</sub>		8.4								
		Setting = 9 x I <sub>nom</sub>		9.4		]						
		Setting = 10 x I <sub>nom</sub>		10.3								

**Table 18. DACs (DAC0, DAC1, DAC2)** (Typical operating conditions (Ta = 25°C, VBATA = 3.3 V, DAC0 Mode 1, Code Range = 200 to 1023), unless otherwise noted. • denotes characterized over complete temperature range.)

Parameter	Symbol	Conditions		Min	Тур	Max	Units					
DC & AC ELECTRICAL CHARACTERISTICS												
Supply Voltage	VBATA			2.2		3.6	V					
Supply Current		Code = 200			150		μA					
		Code = 1023			105							
Reference Voltage		DAC0 Mode 0			VREF		V					
		DAC0 Mode 1, DAC1, DAC2			2 x VREF							
		DAC0 Mode 2			3 x VREF							
Resolution					10		bits					
Output Dynamic Range					58		dB					
Output Voltage Range (Note 21)		DAC0 Mode 0		0.15		0.9	V					
		DAC0 Mode 1		0.15		1.8						
		DAC0 Mode 2		0.15		2.7						
		DAC1		0.15		1.8						
		DAC2		0.15		1.8						

21. VBATA must be greater than the configured output voltage 22. Guaranteed monotonic from code 200 to 1023