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QN908x

Ultra low power Bluetooth 5 system-on-chip solution

Rev. 1.2 — 19 April 2018 Product data sheet

1. Introduction

QN908x is an ultra low power Bluetooth Low Energy wireless MCU with on-chip memory, USB 2.0 full-speed compliant device interface, and 16-bit ADC for Bluetooth Smart applications.

QN9080 integrates a 32-bit ARM Cortex-M4F core with Bluetooth Low Energy (v5.0) compliant radio, link controller, host stack and GATT profiles. The 32-bit ARM Cortex-M4F MCU and on-chip memory provides additional signal processing and scope to run applications for a true single-chip Bluetooth Low Energy (v5.0) solution.

The QN908x uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner. It optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

2. General description

The QN908x is a single chip, 10 mW peak power, high performance Bluetooth Low Energy SoC platform. It facilitates the development of end products such as wearables, health, and sport and fitness trackers. The end products also include retail beacons, connected smart home appliances, smart remote controls, HID devices, asset trackers, and home automation.

QN9080 provides single-chip solution for Bluetooth Smart applications by integrating a Bluetooth Low Energy (v5.0) compliant radio, link controller, host stack and GATT profiles. The integrated 32-bit ARM Cortex-M4F MCU with on-chip flash memory and a mix of analogue and digital peripherals provides the most efficient data fusion engine. The feature makes it a superior solution for applications requiring significant sensor fusion computation.

Additional system features include a fully integrated DC-to-DC converter, LDO, low-power sleep timer, battery monitor, high resolution ADC, and GPIO. These features reduce overall system cost and size.

The QN908x operates with a power supply range of 1.62 V to 3.6 V. The best in-class active current, with ultra-low power sleep modes, give excellent battery life allowing operation from a coin cell battery.

3. Features and benefits

- True single-chip Bluetooth Low Energy (v5.0) SoC solution
  - Integrated Bluetooth LE radio, protocol stack and application profiles
  - Supports central and peripherals roles
  - Supports master/slave concurrency
  - Supports 16 simultaneous links
  - Supports secure connections
  - Supports data packet length extension
  - Wifi/Bluetooth LE coexistence interface
  - 48-bit unique bluetooth device address
- RF
  - –95dBm RX sensitivity in 1Mbps mode, -92dBm RX sensitivity in 2Mbps mode (LDO mode)
  - –94dBm RX sensitivity in 1Mbps mode, -91.5dBm RX sensitivity in 2Mbps mode (DC-to-DC converter mode)
  - Fast and reliable RSSI in 1dB step
  - TX output power from –20 dBm to 2 dBm
  - Single-ended RF port with integrated balun
  - Generic FSK modulation with programmed data rate from 250Kbps to 2Mbps
  - Compatible with worldwide radio frequency regulations
- Very low power consumption
  - Single 1.62 V to 3.6 V power supply
  - Integrated DC-to-DC buck converter and LDO
  - 1.0 μA power-down 1 mode, to wake up by GPIO
  - 2.5 μA power-down 0 mode, to wake up by 32 kHz sleep timer, RTC and GPIO
  - 3.5 mA RX current with DC-to-DC convertor enabled at 3 V supply in 1Mbps mode
  - 5.0 mA RX current with DC-to-DC convertor enabled at 3 V supply in 2Mbps mode
  - 3.5 mA TX current @0 dBm TX power with DC-to-DC converter enabled at 3 V supply in both 1Mbps and 2Mbps mode
- ARM Cortex-M4 core (version r0p1)
  - ARM Cortex-M4 processor, running at a frequency of up to 32 MHz
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU)
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC)
  - Serial Wire Debug (SWD) with six instruction breakpoints, two literal comparators, and four watch points, including serial wire output for enhanced debug capabilities
  - System tick timer
- On-chip memory
  - 512 kB on-chip flash program memory and 2 kB page erase and write
  - 128 kB SRAM
  - 256 kB ROM
- ROM API support
  - Flash In-System Programming (ISP)
- Serial interfaces
  - Four Flexcomm serial peripherals

- USART protocol supported by Flexcomm0, USART and I2C by Flexcomm1, SPI and I2C by Flexcomm2, and SPI by Flexcomm3
- Each Flexcomm includes a FIFO
- I^2C-bus interfaces support fast mode and with multiple address recognition and monitor mode
- USB 2.0 (full speed) device interface
- Two quadrature decoders
- SPI Flash Interface (SPIFI) uses a SPI bus superset with four data lines to access off-chip quad SPI flash memory at a much higher rate than is possible using standard SPI or SSP interfaces
- Supports SPI memories with 1 or 4 data lines

- Digital peripherals
  - DMA controller with 20 channels, able to access memories and DMA capable peripherals
  - Up to 35 General Purpose Input Output (GPIO) pins, with configurable pull-up or pull-down resistors
  - GPIO registers are located on the AHB for fast access
  - 32 GPIOs can be selected as Pin INTerrupts (PINT), triggered by rising, or falling input edges
  - AES-128 security coprocessor
  - Random Number Generator (RNG)
  - CRC engine
  - Fusion Signal Processor (FSP) for data fusion and machine learning algorithms resulting in low power consumption compared to software processing
- Analog peripherals
  - 16-bit ADC with 8 external input channels, with sample rates of up to 32k sample per second, and with multiple internal and external trigger inputs
  - Integrated temperature sensor, connected to one internal dedicated ADC channel
  - Integrated battery monitor connected to one internal dedicated ADC channel
  - General-purpose 8-bit 1M sample per second DAC
  - Integrated capacitive sense up to 8 channels, able to wake up the MCU from low power states.
  - Two ultra low-power analog comparators, able to wake up the MCU from low power states.
- Timers
  - Four 32-bit general-purpose timers or counters, support capture inputs and compare outputs, PWM mode, and external count input
  - Sleep timer, which can work in power-down mode and wake up MCU
  - 32-bit Real Time Clock (RTC) with 1 second resolution running in the always-on power domain; can be used for wake-up from all low power modes including power-down
  - Watchdog Timer.
  - SC Timer or PWM.
- Clock generation
  - 32 MHz internal RC oscillator, which can be used as a system clock

  - 16 MHz or 32 MHz crystal oscillator, which can be used as a system and RF reference
  - 32 kHz on-chip RC oscillator
  - 32.768 kHz crystal oscillator
- Power control
  - Programmable Power Management Unit (PMU) to minimize power consumption
  - Reduced power modes: sleep, and power-down
  - Power-On Reset (POR)
  - Brown-Out Detection (BOD) with separate thresholds for interrupt and forced reset
- Single power supply 1.62 V to 3.6 V
- Operating temperature range −40 °C to +85 °C
- Available as 6 × 6 HVQFN48 and 3.28 × 3.20 mm WLCSP packages

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
QN9080	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 × 6 × 0.85 mm	SOT778-7
QN9083	WLCSP47	wafer level chip-scale package; 47 bumps; 3.28 × 3.20 × 0.365 mm, 0.40 mm pitch	SOT1882-1

4.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Silicon revision[1]	Flash (kB)	Total SRAM (kB)	Cortex-M4 with FPU	FSP	USB FS	GPIO
QN9080	QN9080CHN	C	512	128	1	1	1	35
	QN9080DHN	D	512	128	1	1	1	35
QN9083	QN9083CUK	C	512	128	1	1	1	28
	QN9083DUK	D	512	128	1	1	1	28

[1] For details of Silicon revision, please refer to Errata sheet.

5. Marking

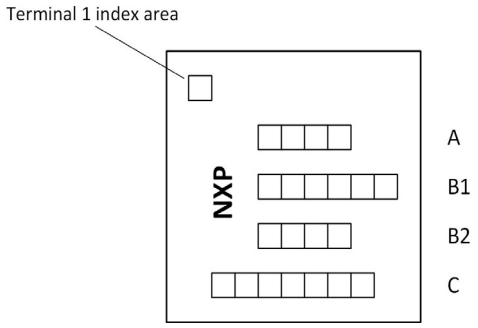


Fig 1. HVQFN48 package marking

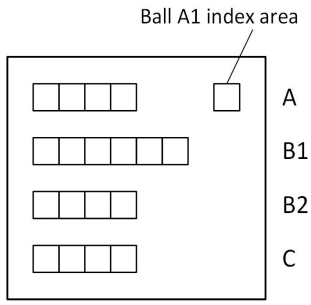


Fig 2. WLCSP47 package marking

The HVQFN package has the following top-side marking:

- Line A: “9080” for QN9080
- Line B1: xxxxxx
- Line B2: xxxx
- Line C: xxYYWW[R]
  - YY: year code, 17 for 2017
  - WW: week code
  - R = Chip revision

The WLCSP package has the following top-side marking:

- Line A: “9083”
- Line B1: xxxxxx
- Line B2: xxWW
  - WW: week code
- Line C: YY[R]x
  - YY: year code, 17 for 2017
  - R = Chip revision

Table 3. Device revision table

Revision identifier (R)	Revision description
‘D’	Current revision
‘C’	Second metal fix revision

6. Block diagram

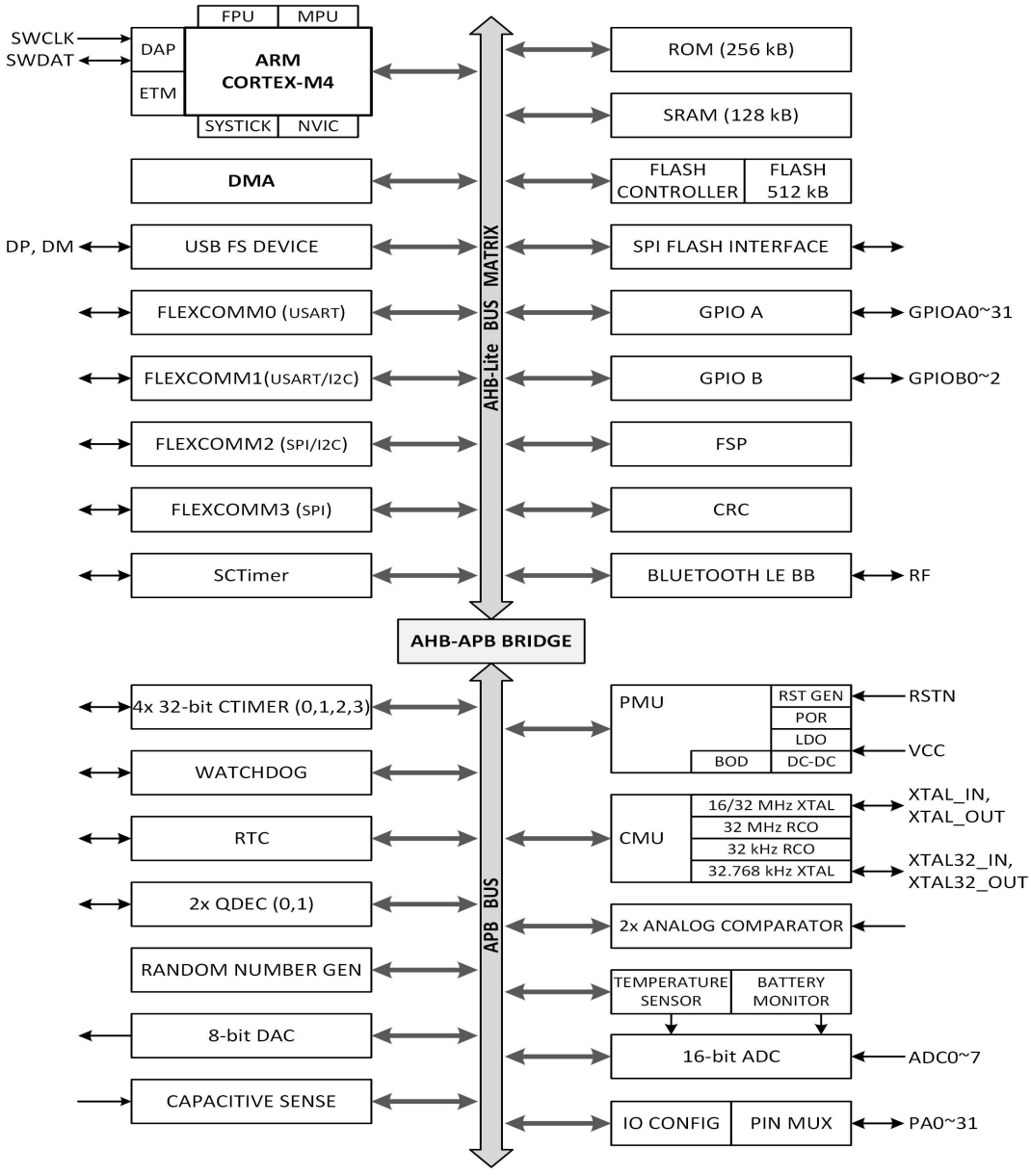


Fig 3. QN908x block diagram

7. Pinning information

7.1 Pinning

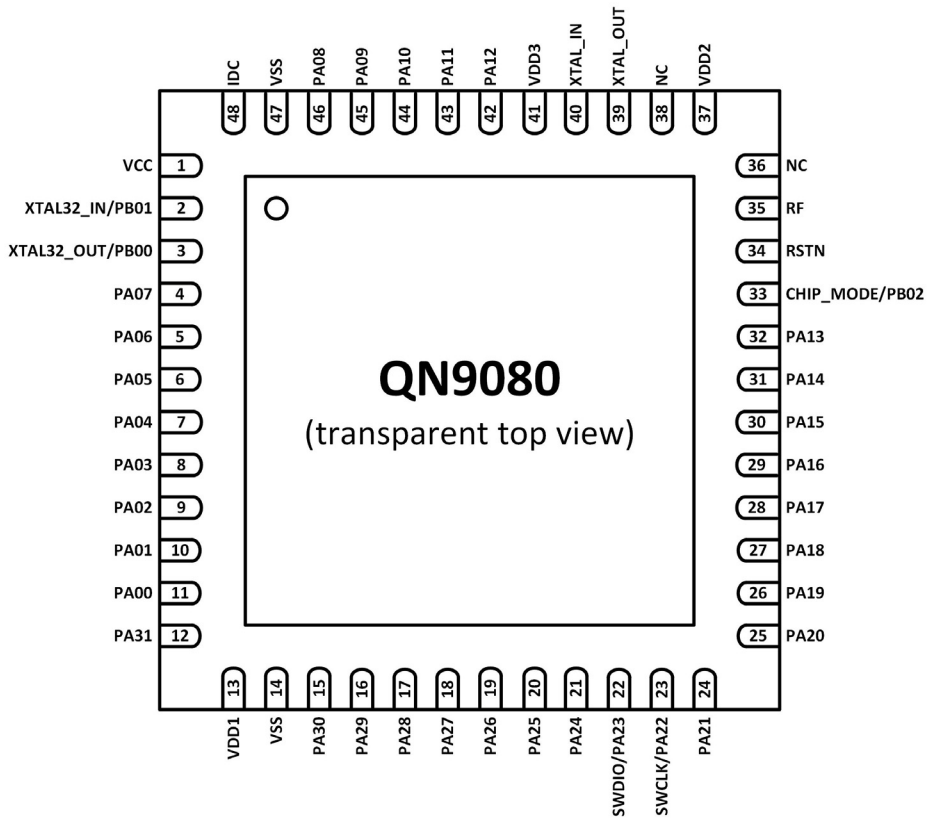


Fig 4. HVQFN48 pin configuration

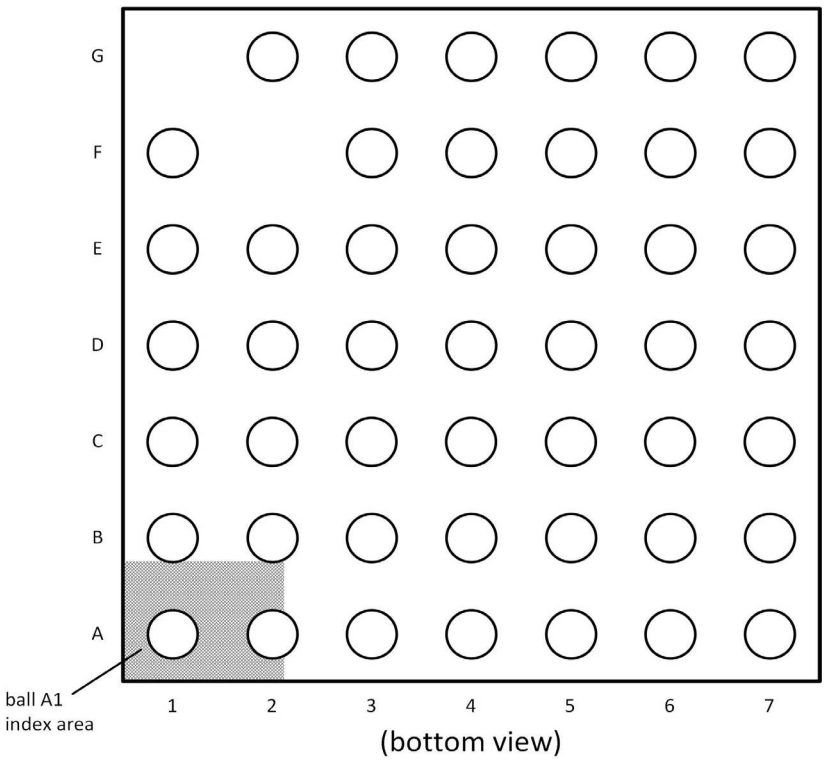


Fig 5. WLCSP pin configuration

7.2 Pin description

In QN908x, each pin can support up to eight different digital or analog functions, including General Purpose Input Output (GPIO).

Table 4. Pin description

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA00	11	6B	PU	GPIOA0	I/O	general-purpose digital input output pin
				ADC0	AI	ADC external input 0
				SCT0_OUT0	O	SCTimer output 0
				CTIMER0_CAP0	I	32-bit CTimer 0 capture input 0
				FC0_RTS	I/O	flexcomm 0: USART RTS
				FC2_SSEL3	I/O	flexcomm 2: SPI SSEL3
				WLAN_TX	I	WLAN active high TX active indicator for coexistence
PA01	10	6A	PU	GPIOA1	I/O	general-purpose digital input output pin
				ADC1	AI	ADC external input 1
				SCT0_OUT1	O	SCTimer output 1
				CTIMER0_CAP1	I	32-bit CTimer 0 capture input 1
				FC0_CTS	I/O	flexcomm 0: USART CTS
				FC2_SSEL2	I/O	flexcomm 2: SPI SSEL2
				WLAN_RX	I	WLAN active high RX active indicator for coexistence
PA02	9	-	PU	GPIOA2	I/O	general-purpose digital input output pin
				QDEC0_A	I	quadrature decoder 0 input channel A
				SCT0_OUT2	O	SCTimer output 2
				CTIMER0_MAT0	O	32-bit CTimer 0 match output 0
				R	I/O	reserved
				FC2_SCL_SSEL1	I/O	flexcomm 2: I2C SCL, SPI SSEL1
				RFE_RX_EN	O	RX enable for external RF front-end
PA03	8	-	PU	GPIOA3	I/O	general-purpose digital input output pin
				QDEC0_B	I	quadrature decoder 0 input channel B
				SCT0_OUT3	O	SCTimer output 3
				CTIMER0_MAT1	O	32-bit CTimer 0 match output 1
				R	O	reserved
				FC2_SDA_SSEL0	I/O	flexcomm 2: I2C SDA, SPI SSEL0
				RFE_TX_EN	O	TX enable for external RF front-end
PA04	7	5B	PU	GPIOA4	I/O	general-purpose digital input output pin
				ADC2	AI	ADC external input 2
				SCT0_OUT4	O	SCTimer output 4
				CTIMER0_MAT0	O	32-bit CTimer 0 match output 0
				FC0_TXD	I/O	flexcomm 0: USART TXD
				FC2_SDA_MOSI	I/O	flexcomm 2: I2C SDA, SPI MOSI
				SPIF_IO0	I/O	data bit 0 for the SPI flash interface

Table 4. Pin description *…continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA05	6	5A	PU	GPIOA5	I/O	general-purpose digital input output pin
				ADC3	AI	ADC external input 3
				SCT0_OUT5	O	SCTimer output 5
				CTIMER0_MAT1	O	32-bit CTimer 0 match output 1
				FC0_RXD	I/O	flexcomm 0: USART RXD
				FC2_SCL_MISO	I/O	flexcomm 2: SCL, SPI MISO
				SPIF_IO1	I/O	data bit 1 for the SPI flash interface
PA06	5	4B	PU	GPIOA6	I/O	general-purpose digital input output pin
				ADC_EX_CAP	A	connected with ADC external capacitor
				SCT0_OUT3	O	SCTimer output 3
				CTIMER0_MAT2	O	32-bit CTimer 0 match output 2
				FC1_RTS_SCL	I/O	flexcomm 1: USART RTS, I2C SCL
				BLE_PTI0	O	BLE packet traffic information bit 0
				SPIFI_CLK	O	clock output for the SPI flash interface
PA07	4	3B	PU	GPIOA7	I/O	general-purpose digital input output pin
				ADC_VREFI	AI	ADC external reference voltage input
				SCT0_OUT2	O	SCTimer output 2
				CTIMER1_CAP0	I	timer 1 input capture 0
				FC1_CTS_SDA	I/O	flexcomm 1: USART CTS, I2C SDA
				BLE_PTI1	O	BLE packet traffic information 1
				SPIFI_CSN	O	active low chip select output for the SPI flash interface
PA08	46	2B	PU	GPIOA8	I/O	general-purpose digital input output pin
				ADC4	AI	ADC external input 4
				SCT0_IN0	I	SCTimer input 0
				CTIMER1_CAP1	I	timer 1 input capture 1
				FC1_TXD_SCL	I/O	flexcomm 1: USART TXD, I2C SCL
				BLE_PTI2	O	BLE packet traffic information 2
				SPIFI_IO2	I/O	data bit 2 for the SPI flash interface
PA09	45	1B	PU	GPIOA9	I/O	general-purpose digital input output pin
				ADC5	AI	ADC external input 5
				SCT0_IN1	I	SCTimer input 1
				CTIMER1_MAT0	O	32-bit CTimer 1 match output 0
				FC1_RXD_SDA	I/O	flexcomm 1: USART RXD, I2C SDA
				BLE_PTI3	O	BLE packet traffic information bit 3
				SPIFI_IO3	I/O	data bit 3 for the SPI flash interface

Table 4. Pin description *…continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA10	44	2C	PU	GPIOA10	I/O	general-purpose digital input output pin
				ADC6	AI	ADC external input 6
				SCT0_IN2	I	SCTimer input 2
				CTIMER1_MAT1	O	32-bit CTimer 1 match output 1
				FC1_SCK	I/O	flexcomm 1: USART clock
				ACMP0_OUT	O	analog comparator 0 output
				BLE_TX	O	BLE transmit indicator for coexistence
PA11	43	2D	PU	GPIOA11	I/O	general-purpose digital input output pin
				ADC7	AI	ADC external input 7
				SCT0_IN3	I	SCTimer input 3
				CTIMER1_MAT2	O	32-bit CTimer 1 match output 2
				FC2_SSEL2	I/O	flexcomm 2: SPI SSEL2
				ACMP1_OUT	O	analog comparator 1 output
				BLE_RX	O	BLE reception indicator for coexistence
PA12	42	-	PU	GPIOA12	I/O	general-purpose digital input output pin
				R	O	reserved
				SCT0_OUT5	O	SCTimer output 5
				ACMP0_OUT	O	analog comparator 0 output
				FC1_TXD_SCL	I/O	flexcomm 1: USART TXD, I2C SCL
				SD_DAC	O	sigma-delta modulator DAC output
				ANT_SW	O	external antenna switch for diversity
PA13	32	-	PU	GPIOA13	I/O	general-purpose digital input output pin
				R	I/O	reserved
				SCT0_OUT4	O	SCTimer output 4
				ACMP1_OUT	O	analog comparator 1 output
				FC1_RXD_SDA	I/O	flexcomm 1: USART RXD, I2C SDA
				FC3_SSEL1	I/O	flexcomm 3: SPI SSEL1
				RFE_EN	O	enable for external RF front-end
PA14	31	5G	PU	GPIOA14	I/O	general-purpose digital input output pin
				CS0	AI	capacitive touch sense button input 0
				ANT_SW	O	external antenna switch for diversity
				CTIMER2_CAP0	I	timer 2 input capture 0
				FC0_RTS	I/O	flexcomm 0: USART RTS
				FC3_SSEL0	I/O	flexcomm 3: SPI SSEL0
				QDEC1_A	I	quadrature decoder 1 input channel A

Table 4. Pin description *…continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA15	30	4G	PU	GPIOA15	I/O	general-purpose digital input output pin
				CS1	AI	capacitive touch sense button input 1
				SCT0_OUT0	O	SCTimer output 0, PWM output 0
				CTIMER2_CAP1	I	timer 2 input capture 1
				FC0_CTS	I/O	flexcomm 0: USART CTS
				FC3_SCK	I/O	flexcomm 3: SPI clock
				QDEC1_B	I	quadrature decoder 1 input channel B
PA16	29	4F	PU	GPIOA16	I/O	general-purpose digital input output pin
				CS2	AI	capacitive touch sense button input 2
				SCT0_OUT1	O	SCTimer output 1, PWM output 1
				CTIMER2_MAT0	O	32-bit CTimer 2 match output 0
				FC0_TXD	I/O	flexcomm 0: USART TXD
				FC3_MOSI	I/O	flexcomm 3: SPI MOSI
				QDEC0_A	I	quadrature decoder 0 input channel A
PA17	28	6G	PU	GPIOA17	I/O	general-purpose digital input output pin
				CS3	AI	capacitive touch sense button input 3
				SD_DAC	O	sigma-delta modulator DAC output
				CTIMER2_MAT1	O	32-bit CTimer 2 match output 1
				FC0_RXD	I/O	flexcomm 0: USART RXD
				FC3_MISO	I/O	flexcomm 3: SPI MISO
				QDEC0_B	I	quadrature decoder 0 input channel B
PA18	27	5F	PU	GPIOA18	I/O	general-purpose digital input output pin
				CS4	AI	capacitive touch sense button input 4
				SCT0_OUT3	O	SCTimer output 3, PWM output 3
				CTIMER2_MAT2	O	32-bit CTimer 2 match output 2
				FC0_SCK	I/O	flexcomm 0: USART clock
				FC3_SSEL2	I/O	flexcomm 3: SPI SSEL2
				BLE_SYNC	O	BLE sync pulse
PA19	26	7G	PU	GPIOA19	I/O	general-purpose digital input output pin
				CS5	AI	capacitive touch sense button input 5
				SCT0_OUT2	O	SCTimer output 2, PWM output 2
				RFE_EN	O	enable for external RF front-end
				FC0_SCK	I/O	flexcomm 0: USART clock
				FC3_SSEL3	I/O	flexcomm 3: SPI SSEL3
				BLE_IN_PROC	O	BLE event in process indicator for coexistence

Table 4. Pin description *...continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA20	25	-	PU	GPIOA20	I/O	general-purpose digital input output pin
				QDEC1_A	I	quadrature decoder 1 input channel A
				SCT0_OUT1	O	SCTimer output 1, PWM output 1
				CTIMER2_MAT0	O	32-bit CTimer 2 match output 0
				SWO	I/O	serial wire trace output
				FC1_RTS_SCL	I/O	flexcomm 1: USART RTS, I2C SCL
				SPIFI_CLK	O	clock output for the SPI flash interface
PA21	24	-	PU	GPIOA21	I/O	general-purpose digital input output pin
				QDEC1_B	I	quadrature decoder 1 input channel B
				SCT0_OUT0	O	SCTimer output 0, PWM output 0
				CTIMER2_MAT1	O	32-bit CTimer 2 match output 1
				FC2_SSEL3	I/O	flexcomm 2: SPI SSEL3
				FC1_CTS_SDA	I/O	flexcomm 1: USART CTS, I2C SDA
				SPIFI_CSN	O	active low chip select output for the SPI flash interface
SWCLK /PA22	23	7F	PU	SWCLK	I/O	serial wire clock; it is the default function after reset
				GPIOA22	I/O	general-purpose digital input output pin
				SCT0_IN2	I	SCTimer input 2
				CTIMER3_MAT0	O	32-bit CTimer 3 match output 0
				FC2_SDA_SSEL0	I/O	flexcomm 2: I2C SDA, SPI SSEL0
				FC3_SSEL3	I/O	flexcomm 3: SPI SSEL3
				QDEC1_A	I	quadrature decoder 1 input channel A
SWDIO/ PA23	22	6F	PU	SWDIO	I/O	serial wire debug I/O; it is the default function after booting
				GPIOA23	I/O	general-purpose digital input output pin
				SCT0_IN3	I	SCTimer input 3
				CTIMER3_MAT1	O	32-bit CTimer 3 match output 1
				FC2_SCL_SSEL1	I/O	flexcomm 2: I2C SCL, SPI SSEL1
				FC3_SSEL2	I/O	flexcomm 3: SPI SSEL2
				QDEC1_B	I	quadrature decoder 1 input channel B
PA24	21	6E	PU	GPIOA24	I/O	general-purpose digital input output pin
				ACMP0N/CS6	AI	analog comparator 0 negative input, or capacitive touch sense button input 6
				ETM_TRACEDAT0	O	ETM trace data output bit 0
				CTIMER3_CAP0	I	timer 3 input capture 0
				RFE_RX_EN	O	RX enable for external RF front-end
				FC3_SSEL1	I/O	flexcomm 3: SPI SSEL1
				SPIFI_IO0	I/O	data bit 0 for the SPI flash interface

Table 4. Pin description *…continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA25	20	7E	PU	GPIOA25	I/O	general-purpose digital input output pin
				ACMP0P/CS7	AI	analog comparator 0 positive input, or capacitive touch sense button input 7
				ETM_TRACEDAT1	O	ETM trace data output bit 1
				CTIMER3_CAP1	I	timer 3 input capture 1
				RFE_TX_EN	O	TX enable for external RF front-end
				FC3_SSEL0	I/O	flexcomm 3: SPI SSEL0
				SPIFI_IO1	I/O	data bit 1 for the SPI flash interface
PA26	19	6D	PU	GPIOA26	I/O	general-purpose digital input output pin
				USB_DP	I/O	USB0 bidirectional D+ line
				SCT0_IN0	I	SCTimer input 0
				CTIMER1_MAT0	O	32-bit CTimer 1 match output 0
				FC2_SDA_MOSI	I/O	flexcomm 2: I2C SDA, SPI MOSI
				QDEC0_A	I	quadrature decoder 0 input channel A
				BLE_SYNC	O	BLE sync pulse
PA27	18	7D	PU	GPIOA27	I/O	general-purpose digital input output pin
				USB_DM	I/O	USB0 bidirectional D- line
				SCT0_IN1	I	SCTimer input 1
				CTIMER1_MAT2	O	32-bit CTimer 1 match output 2
				FC2_SCL_MISO	I/O	flexcomm 2: I2C SCL, SPI MISO
				QDEC0_B	I	quadrature decoder 0 input channel B
				BLE_IN_PROC	O	BLE event in process indicator for coexistence
PA28	17	-	PU	GPIOA28	I/O	general-purpose digital input output pin
				CLK_AHB	O	AHB clock output
				ETM_TRACECLK	O	ETM trace clock output
				RTC_CAP	I	RTC capture input
				FC1_SCK	I/O	flexcomm 1: USART clock
				SD_DAC	O	sigma-delta modulator DAC output
				SPIFI_CSN	O	active low chip select output for the SPI flash interface
PA29	16	6C	PU	GPIOA29	I/O	general-purpose digital input output pin
				ACMP1N	AI	analog comparator 1 negative input
				ETM_TRACEDAT2	O	ETM trace data output bit 2
				CTIMER3_MAT0	O	timer 3 match output 0
				FC2_SCK	I/O	flexcomm 2: SPI clock
				FC3_MISO	I/O	flexcomm 3: SPI MISO
				SPIFI_IO2	I/O	data bit 2 for the SPI flash interface

Table 4. Pin description *…continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA30	15	7C	PU	GPIOA30	I/O	general-purpose digital input output pin
				ACMP1P	AI	analog comparator 1 positive input
				ETM_TRACEDAT3	O	ETM trace data output bit 3
				CTIMER3_MAT1	O	timer 3 match output 1
				FC2_SCK	I/O	flexcomm 2: SPI clock
				FC3_MOSI	I/O	flexcomm 3: SPI MOSI
				SPIFI_IO3	I/O	data bit 3 for the SPI flash interface
PA31	12	7B	PU	GPIOA31	I/O	general-purpose digital input output pin
				DAC	AO	DAC analog output
				RTC_CAP	I	RTC capture input
				CTIMER3_MAT2	O	Timer 3 match output 2
				SWO	I/O	serial wire trace output
				FC3_SCK	I/O	flexcomm 3: SPI clock
				SPIFI_CLK	O	clock output for the SPI flash interface
XTAL32_OUT/PB00	3	4A	-	XTAL32_OUT	AO	32.768 kHz crystal oscillator output **Remark:** leave it unconnected or used as GPIO when the LFXO is not used.
				GPIOB00	I/O	general-purpose digital input output pin
XTAL32_IN/PB01	2	3A	-	XTAL32_IN	AI	32.768 kHz crystal oscillator input **Remark:** external input clock can be injected when the LFXO is not used.
				GPIOB01	I/O	general-purpose digital input output pin
CHIP_MODE/PB02	33	3C	PU	CHIP_MODE	I	boot selection with pull-up by default; it should be pulled low to go through the normal ISP process for firmware programming, otherwise the ISP process is escaped to jump to flash
				GPIOB02	I/O	general-purpose digital input output pin
				ANT_SW	O	external antenna switch for diversity
RSTN	34	4E	PU	-	I	active low reset input
XTAL_OUT	39	1D	-	-	AO	16/32 MHz crystal oscillator output **Remark:** leave it unconnected if not used for crystal oscillator
XTAL_IN	40	1C	-	-	AI	16/32 MHz crystal oscillator input **Remark:** this can be used as external clock input, without using internal crystal oscillator
RF	35	2G	-	-	RF	RF input output port with Tx or Rx switch integrated on chip
VCC	1	2A	-	-	-	power supply (1.62 V to 3.6 V)
VDD1	13	7A	-	-	-	digital power supply
VDD2	37	1E	-	-	-	RF power supply
VDD3	41	2E	-	-	-	analog power supply

Table 4. Pin description *…continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
VSS	14,47	1F,3D,3E,3F,3G,4C,4D,5C,5D,5E	-	-	-	ground
IDC	48	1A	-	-	AO	DC-to-DC converter output; refer to reference design circuit when DC-to-DC is used; leave it open when DC-to-DC is not used
NC	36,38	-	-	-	-	not connected

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{CC}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, AO = analog output, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 7.2.2. For termination on unused pins, see Section 7.2.1.

7.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function can be left unconnected and are configured as input with their internal pull-up or pull-down enabled. Enabling pull-down is preferred.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as inputs, with their internal pull-up or pull-down enabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
PAnm	I; PU	unconnected if driven LOW and configured as GPIO output with pull-up disabled by software
XTAL32_IN	-	unconnected
XTAL32_OUT	-	unconnected

[1] I = Input, PU = Pull-up enabled

7.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Power-down
PAnm pins	As configured in the SYSCON[1]. Default: input with internal pull-up enabled		
RSTN	Reset function enabled. Default: input, internal pull-up enabled		

[1] Default and programmed pin states are retained in sleep and power down mode

8. Functional description

8.1 Architectural overview

The ARM Cortex-M4 includes one AHB-Lite bus, one system bus, and I-code and D-code buses. Separate buses are dedicated for instruction fetch (I-code) and data access (D-code).

The QN908x uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner. It optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

8.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general-purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, and interruptable or continuable multiple load and store instructions. It also provides automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is executed, its successor is decoded, and a third instruction is fetched from memory.

8.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE standard 754-2008. The IEEE standard for binary floating-point arithmetic is referred as the IEEE 754 standard.

8.4 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data. Access to memory regions can be disabled and also be defined as read-only. It detects unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions, each of which is divided into eight sub-regions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will trigger memory management fault exception.

8.5 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

The NVIC supports 52 external interrupt input sources, each with eight levels of priority. The processor supports both level and edge interrupts. External interrupt signals are connected to the NVIC, and the NVIC prioritizes the interrupts. Software is used to set the priority of each interrupt. The NVIC and the Cortex-M4F processor core are closely coupled, providing low-latency interrupt processing and efficient processing of late arriving interrupts.

The Wake-up Interrupt Controller (WIC) supports ultra-low power sleep mode. It enables the processor and NVIC to be put into a very low-power sleep mode leaving the WIC to identify and prioritize the interrupts. The processor implements the Wait-For-Interrupt (WFI), Wait-For-Event (WFE) and the Send EVent (SEV) instructions. In addition, the processor also supports use of SLEEPONEXIT, which causes the processor core to enter sleep mode when it returns from an exception handler to thread mode.

8.5.1 Features

- Controls system exceptions and peripheral interrupts
- 52 external interrupt input sources
- Eight programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table using Vector Table Offset Register (VTOR)
- Software interrupt generation

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. There are 52 interrupt sources in total.

8.6 System Tick timer (SysTick)

The ARM Cortex-M4 core includes a System Tick timer (SysTick) that generates a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

8.7 On-chip static RAM

QN908x supports 128 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

The 128 kB SRAM is divided into ten memory blocks, each with separate power control, to refine the power consumption according to application requirements.

Table 7. SRAM memory blocks

SRAM block	SIze	Start address offset
9	4k × 32 bit	0x0001 C000
8	4k × 32 bit	0x0001 8000
7	4k × 32 bit	0x0001 4000
6	4k × 32 bit	0x0001 0000

Table 7. SRAM memory blocks

SRAM block	SIze	Start address offset
5	4k × 32 bit	0x0000 C000
4	4k × 32 bit	0x0000 8000
3	4k × 32 bit	0x0000 4000
2	2k × 32 bit	0x0000 2000
1	1k × 32 bit	0x0000 1000
0	1k × 32 bit	0x0000 0000

8.8 On-chip flash

The QN908x supports 512 kB of on-chip flash memory, to store code and data. The MCU accesses the flash via flash controller.

- 256 equal pages with 2 kB each; any page can be erased individually
- Greater than 10 years of data retention at 85°C
- Endurance: minimum 10,000 cycles

8.9 On-chip ROM

The 256 kB on-chip ROM contains boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) support for flash programming

8.10 Memory mapping

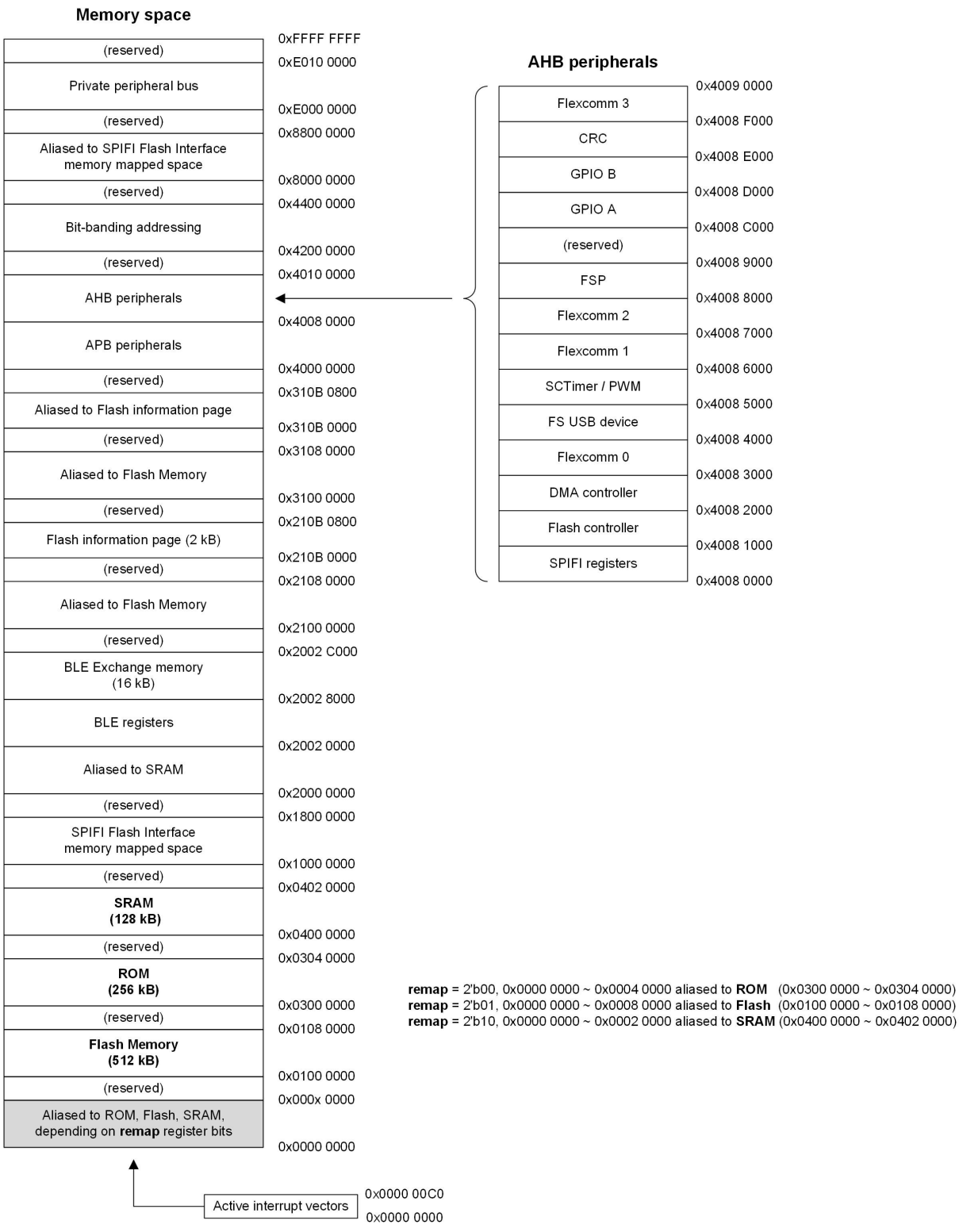
QN908x incorporates several distinct memory regions. The APB peripheral area is 64 kB in size and is divided to allow for multiple peripherals. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

QN908x integrates four types of memories: embedded flash, ROM, SRAM, and external SPIFI memory interface. To provide enough flexibility, the flash, ROM and RAM can be mapped to different regions of the memory map, depending on the register bits remap. The remap is 0 after reset and ROM is remapped to the address 0x0000 0000.

Table 8. Memory map options

Memory	Primary space	Alias	Memory remap option
ROM (256 kB)	0x0300 0000 to 0x0304 0000	N/A	0x0000 0000 to 0x0004 0000 (remap=0)
flash (512 kB)	0x0100 0000 to 0x0108 0000	0x2100 0000 to 0x2108 0000; 0x3100 0000 to 0x3108 0000	0x0000 0000 to 0x0008 0000 (remap=1)
SRAM (128 kB)	0x0400 0000 to 0x0402 0000	0x2000 0000 to 0x2002 0000	0x0000 0000 to 0x0002 0000 (remap=2)
SPIFI flash memory	0x1000 0000 to 0x1800 0000	0x8000 0000 to 0x8800 0000	N/A

Figure 6 shows the overall map of the entire address space from the user program viewpoint.



The private peripheral bus includes CPU peripherals such as the NVIC, SysTick, and the core control registers.

Fig 6. QN908x memory mapping

Fig 7. QN908x APB memory map

8.11 Power management

To minimize system power consumption, the QN908x supports a variety of power modes and power management features.

8.11.1 Power supply

QN908x integrates both LDO and DC-to-DC converter. When the device is powered at a higher supply voltage like 3 V, DC-to-DC converter can be used to reduce current consumption.

When in the LDO mode without using DC-to-DC converter, users should make sure the VDD1, VDD2 and VDD3 never ramp-up before VCC. A simple way is to connect them together. Refer to the reference schematic for more information.

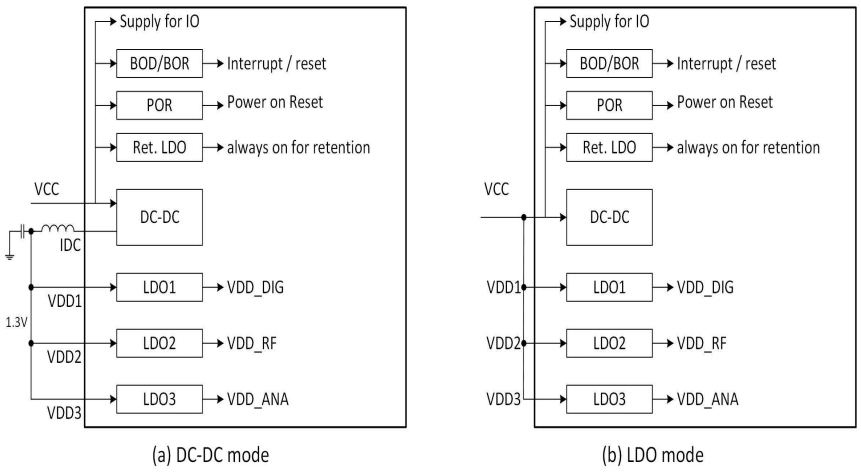


Fig 8. QN908x power supply

8.11.2 Power modes

A variety of power modes are supported for the optimization of power consumption, including active, sleep, power-down 0 and power-down 1 mode. Upon power-up or reset, the device enters active mode. After processing is complete, the software puts the chip into sleep mode or power-down mode, to save power consumption. The device is woken up either by a reset or an interrupt trigger like a GPIO interrupt, timer timeout, or other wake-up sources.

8.11.2.1 Sleep mode

In sleep mode, the system clock to the CPU is stopped and execution of instructions is suspended until either a reset or an interrupt occurs. Peripheral functions, if selected to be clocked, can continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

8.11.2.2 Power-down 0 mode

In power-down 0 mode, power is shut off to the entire chip except for the always-on PMU domain, 32.768 kHz crystal oscillator, 32k RC oscillator, sleep timer, RTC, and the RSTN pin. All peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock running. In addition, all analog blocks and flash are shut down. In power down mode, the application can keep the analog comparator circuit running to monitor external voltage input, which wakes up the device if external voltage is higher than the reference voltage.

The QN908x wakes up from power-down 0 mode via a reset, digital pins selected as inputs to the pin interrupt block, sleep timer timeout interrupt, RTC interrupt, BOD forced reset, analog comparator interrupt, or cap sense interrupt.