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Cortina Systems® LXT9785 and LXT9785E Advanced 8-Port 10/100 Mbps PHY Transceivers

Datasheet

The Cortina Systems® LXT9785 and LXT9785E are 8-port Fast Ethernet PHY Transceivers supporting IEEE 802.3 physical layer applications at 10 Mbps and 100 Mbps. These devices provide Serial/Source Synchronous Serial Media Independent Interfaces (SMII/SS-SMII) and Reduced Media Independent Interface (RMII) for switching and other independent port applications. The LXT9785 and LXT9785E are identical except for the IP telephony features included in the LXT9785E transceiver. The LXT9785E is an enhanced version of the LXT9785 that detects Data Terminal Equipment (DTE) requiring power from the switch over a CAT5 cable. The system uses the information collected by the LXT9785E to apply power if the DTE at the far end requires power over the cable, such as an IP telephone.

Each network port can provide a twisted-pair (TP) or Low-Voltage Positive Emitter Coupled Logic (LVPECL) interface. The twisted-pair interface supports 10 Mbps and 100 Mbps (10BASE-T and 100BASE-TX) Ethernet over twisted-pair. The LVPECL interface supports 100 Mbps (100BASE-FX) Ethernet over fiber-optic media.

The LXT9785/LXT9785E provides three discrete LED driver outputs for each port. The devices support both half-duplex and full-duplex operation at 10 Mbps and 100 Mbps and require only a single 2.5 V power supply.

Applications

- Enterprise switches
- IP telephony switches
- Storage Area Networks
- Multi-port Network Interface Cards (NICs)

Product Features

- Eight IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters.
- 100BASE-FX fiber-optic capability on all ports.
- 2.5 V operation.
- Low power consumption; 250 mW per port typical.
- Multiple RMII or SMII/SS-SMII ports for independent PHY port operation.
- Auto MDI/MDIX crossover capability.
- Proprietary Optimal Signal Processing™ architecture improves SNR by 3 dB over ideal analog filters.
- Optimized for dual-high stacked RJ-45 applications.
- MDIO sectionalization into 2x4 or 1x8 configurations.
- Supports both auto-negotiation systems and legacy systems without auto-negotiation capability.
- Robust baseline wander correction.
- Configurable through the MDIO port or external control pins.
- JTAG boundary scan.
- 208-pin PQFP: LXT9785HC, LXT9785EHC, LXT9785HE.
- 241-ball BGA: LXT9785BC, LXT9785EBC.
- 196-ball BGA: LXT9785MBC (includes DTE detection similar to the LXT9785E)
- DTE detection for remote powering applications (LXT9785E and LXT9785MBC only).
- Extended temperature operation of -40 °C to +85 °C (LXT9785E only).

Contents

Figures

Tables

Revision History

Revision 11.0 Revision Date: 16 April 2007
First release of this document from Cortina Systems, Inc.

Revision Number: 010 Revision Date: 30-Mar-2006	
Page	**Description**
page 48	Modified signal description text for VCCPECL in Table 15, *Power Supply Signal Descriptions – PQFP*.
page 93	Modified signal description text for VCCPECL in Table 34, *Power Supply Signal Descriptions – BGA23*.
page 123	Added note under Section 4.4.2.5, *RxCLK Signal (SS-SMII Only)*.
page 126	Modified CFG (1,2,3) settings for Register bit 0.8 when set to “1” in Table 42, *Global Hardware Configuration Settings*.
page 192	Added table note 6 to Register bit 0.14 (Loopback) in Table 84, *Control Register (Address 0)* .
page 195	Modified table note 6 (for Register bit 4.13) in Table 88, *Auto-Negotiation Advertisement Register (Address 4)*.
page 200	Modified note in Register bit 17.11 (Collision Status) in Table 94, *Quick Status Register (Address 17, Hex 11)*.
page 217	Added Section 8.1, *Top Label Markings*.
page 219	Modified Section 9.0, *Ordering Information* (Table 105, *Product Information* and Figure 72, *Ordering Information - Sample*.

Revision Number: 009 Revision Date: April 30, 2004	
Page	**Description**
1	Modified 196-Ball BGA and DTE Detection bullets under Product Features.
43	Added table note 3 (regarding LINKHOLD) to Table 13, *Miscellaneous Signal Descriptions – PQFP*, on page 43.
88	Added table note 3 (regarding LINKHOLD) to Table 32, *Miscellaneous Signal Descriptions – BGA23*, on page 88.
53	Modified Table 18 “RMII BGA23 Ball List in Alphanumeric Order by Signal Name” through Table 23 “SS-SMII BGA23 Ball List in Alphanumeric Order by Ball Location” for ball, type, and reference page corrections.
229	Modified Table 104 “Product Information” [added new packaging information].
230	Modified Figure 69 “Ordering Information - Sample” [changed Internal Package Designator for B and E, and added the GD and definition under Package Designator).

Revision Number: 008 Revision Date: April 15, 2004	
Page	**Description**
All	Globally added LEDn_3 to BGA15.
229	Added Figure 68 “Cortina Systems® LXT9785MBC 196-Ball BGA15 Package – Bottom View”.

Revision Number: 007 Revision Date: August 28, 2003	
Page	**Description**
21	Modified Figure 2 “Cortina Systems® LXT9785 and Cortina Systems® LXT9785E RMII 208-Pin PQFP Assignments”.
22	Modified Table 2 “Cortina Systems® LXT9785/LXT9785E RMII PQFP Pin List”.
26	Modified Figure 3 “Cortina Systems® LXT9785/LXT9785E SMII 208-Pin PQFP Assignments”.
27	Modified Table 3 “Cortina Systems® LXT9785/LXT9785E SMII PQFP Pin List”.
31	Modified Figure 4 “Cortina Systems® LXT9785/LXT9785E SS-SMII 208-Pin PQFP Assignments”.
32	Modified Table 4 “Cortina Systems® LXT9785/LXT9785 SS-SMII PQFP Pin List”.
36	Modified Table 5 “Cortina Systems® LXT9785/LXT9785E RMII Signal Descriptions – PQFP”.
40	Modified Table 8 “Cortina Systems® LXT9785/LXT9785E SS-SMII Specific Signal Descriptions – PQFP”.
43	Modified Table 13 “Cortina Systems® LXT9785/LXT9785E Miscellaneous Signal Descriptions – PQFP”.
50	Modified Table 16 “Cortina Systems® LXT9785/LXT9785E Unused/Reserved Pins – PQFP”.
51	Replaced old Figures 5, 6, and 7 with Figure 5 “Cortina Systems® LXT9785/LXT9785E 241-Ball BGA23 Assignments (Top View)”.
52	Modified Table 18 “Cortina Systems® LXT9785/LXT9785E RMII BGA23 Ball List in Alphanumeric Order by Signal Name”.
57	Modified Table 19 “Cortina Systems® LXT9785/LXT9785E RMII BGA23 Ball List in Alphanumeric Order by Ball Location”.
62	Modified Table 20 “Cortina Systems® LXT9785/LXT9785E SMII BGA23 Ball List in Alphanumeric Order by Signal Name”.
67	Modified Table 21 “Cortina Systems® LXT9785/LXT9785E SMII BGA23 Ball List in Alphanumeric Order by Ball Location”
72	Modified Table 22 “Cortina Systems® LXT9785/LXT9785E SS-SMII BGA23 Ball List in Alphanumeric Order by Signal Name”.
77	Modified Table 23 “Cortina Systems® LXT9785/LXT9785E SS-SMII BGA23 Ball List in Alphanumeric Order by Ball Location”.
82	Modified Table 23 “Cortina Systems® LXT9785/LXT9785E SS-SMII BGA23 Ball List in Alphanumeric Order by Ball Location”.
86	Modified Table 27 “Cortina Systems® LXT9785/LXT9785E SS-SMII Specific Signal Descriptions – BGA23”.
90	Modified Table 32 “Cortina Systems® LXT9785/LXT9785E Miscellaneous Signal Descriptions – BGA23”.
97	Modified Table 35 “Cortina Systems® LXT9785/LXT9785E Unused/Reserved Pins – BGA23”.
98	Added Section 3.5, “BGA15 Ball Assignments” (including Figure 6 “Cortina Systems® LXT9785MBC 196-Ball BGA15 Assignments (Top View)”, Table 37 “Cortina Systems® LXT9785MBC BGA15 Ball List in Alphanumeric Order by Signal Name” through Table 39 “Cortina Systems® LXT9785 BGA15 Signal Descriptions”.
116	Added second paragraph under Section 4.1, “Introduction”.
117	Added note under Section 4.1.2.1, “Sectionalization”.
119	Added note under Table 40 “Cortina Systems® LXT9785/LXT9785E MDIX Selection”.
119	Added note under Section 4.3, “Media Independent Interface (MII) Interfaces”.
120	Added note to Table 41 “Cortina Systems® LXT9785/LXT9785E MII Mode Select”.
120	Modified/added text under Section 4.3.2, “Internal Loopback”.
121	Modified text under Section 4.3.6, “MII Isolate”.

Revision Number: 007 Revision Date: August 28, 2003	
Page	**Description**
121	Section 4.3.7, “MDIO Management Interface”: Added note under second paragraph. Added last paragraph.
123	Added note under Section 4.3.8, “MII Sectionalization”.
124	Added new Section 4.3.11, “FIFO Initial Fill Values”
125	Modified paragraph three under Section 4.4.1, “Power Requirements”.
127	Added notes under second and last paragraphs under Section 4.5.3, “Power-Down Mode”.
128	Modified last bullet under Section 4.5.3.1, “Global (Hardware) Power Down”.
128	Added last paragraph to Section 4.5.4, “Reset”.
129	Modified Table 42 “Cortina Systems® LXT9785/LXT9785E Global Hardware Configuration Settings”.
130	Change heading and modified last line under Section 4.6.1.2, “Manual Next Page Exchange”.
130	Section 4.6.1.4, “Link Criteria”: Changed scrambler to descrambler in first line. Modified second paragraph. Added two new paragraphs.
131	Added second paragraph under Section 4.6.1.5, “Parallel Detection”.
131	Modified paragraphs under Section 4.6.1.6, “Reliable Link Establishment While Auto MDI/MDIX is Enabled in Forced Speed Mode”.
136	Changed “1110” to “0101” under Section 4.7.4.3, “Receive Error”.
141	Added note under first paragraph of Section 4.8, “RMII Operation”
148	Changed “asynchronously” to “synchronously” in second paragraph under Section 4.9.3.3, “Carrier Sense/Data Valid (RMII)”.
148	Modified last sentence in first paragraph under Section 4.9.3.4, “Carrier Sense (SMII)”.
149	Modified paragraph under Section 4.9.3.6.3, “Polarity Correction”.
149	Added note under Section 4.9.3.7, “Fiber PMD Sublayer”.
149	Added second paragraph under Section 4.9.3.7.1, “Far End Fault Indications”.
150	Modified/added text under Section 4.10.1, “Preamble Handling”.
151	Modified text under Section 4.10.4, “Jabber”.
152	Modified first paragraph under Section 4.11, “DTE Discovery Process”.
153	Modified Item 1 of Section 4.11.2, “Interaction between Processor, MAC, and PHY”.
154	Modified second paragraph under Section 4.11.4, “DTE Discovery Process Flow”.
155	Added Section 4.11.5, “DTE Discovery Behavior”
157	Added BGA15 information into first paragraph under Section 4.12.2, “Per-Port LED Driver Functions”.
158	Added last sentence to first paragraph and note under first paragraph under Section 4.12.3, “Out-of-Band Signaling”.
160	Added Section 4.13, “Cable Diagnostics Overview”.
161	Modified/added text under Section 4.13.3, “Implementation Considerations”.
162	Added Section 4.14, “Link Hold-Off Overview”.
173	Modified Table 52 “Cortina Systems® LXT9785/LXT9785E Operating Conditions”
176	Modified Table 58 “Cortina Systems® LXT9785/LXT9785E 100BASE-FX Transceiver Characteristics”

Revision Number: 007 Revision Date: August 28, 2003	
Page	**Description**
178-195	Added note to Table 60 “Cortina Systems® LXT9785/LXT9785E SMII - 100BASE-TX Receive Timing Parameters” through Table 77 “Cortina Systems® LXT9785/LXT9785E RMII - 10BASE-T Transmit Timing Parameters”.
178	Added table note to Table 60 “Cortina Systems® LXT9785/LXT9785E SMII - 100BASE-TX Receive Timing Parameters”.
184	Added table note to Table 66 “Cortina Systems® LXT9785/LXT9785E SS-SMII - 100BASE-TX Receive Timing Parameters”.
190	Added table note to Table 72 “Cortina Systems® LXT9785/LXT9785E RMII - 100BASE-TX Receive Timing Parameters”
198	Added software power-down and note to Table 80 “Cortina Systems® LXT9785/LXT9785E Power-Up Timing Parameters”.
199	Modified paragraphs and added last paragraph under Section 7.0, “Register Definitions”.
199	Modified Table 82 “Cortina Systems® LXT9785/LXT9785E Register Set”.
200	Modified Table 83 “Control Register (Address 0)”.
201	Modified Table 84 “Status Register (Address 1)”.
203	Modified Table 85 “PHY Identification Register 1 (Address 2)”.
203	Modified Table 86 “PHY Identification Register 2 (Address 3)”
204	Modified Table 87 “Auto-Negotiation Advertisement Register (Address 4)”
205	Modified Table 88 “Auto-Negotiation Link Partner Base Page Ability Register (Address 5)”.
206	Modified Table 89 “Auto-Negotiation Expansion Register (Address 6)”.
206	Modified Table 90 “Auto-Negotiation Next Page Transmit Register (Address 7)”.
206	Modified Table 91 “Auto-Negotiation Link Partner Next Page Receive Register (Address 8)”.
207	Modified Table 92 “Port Configuration Register (Address 16, Hex 10)”. (Register bits 16.6, 16.4:3)
209	Modified Table 93 “Quick Status Register (Address 17, Hex 11)”. (Register bit 17.8)
211	Modified Table 94 “Interrupt Enable Register (Address 18, Hex 12)”
212	Modified Table 95 “Interrupt Status Register (Address 19, Hex 13)”
213	Modified Table 96 “LED Configuration Register (Address 20, Hex 14)”
214	Modified Table 97 “Receive Error Count Register (Address 21, Hex 15)”.
215	Modified Table 98 “RMII Out-of-Band Signaling Register (Address 25, Hex 19)”.
216	Modified Table 99 “Trim Enable Register (Address 27, Hex 1B)”. (Register bit 27.6)
217	Added Table 100 “Cable Diagnostics Register (Address 29, Hex 1D)”.
219	Modified Table 101 “Cortina Systems® LXT9785/LXT9785E Register Bit Map”.
226	Added Figure 102 “Cortina Systems® LXT9785MBC 196-Ball BGA15 Package Dimensions”
227	Modified table and figure under Section 9.0, “Ordering Information”.

Revision Number: 006 (INTERNAL RELEASE) Revision Date: June 10, 2003	
Page	**Description**
1	Changed "pseudo-ECL (PECL)" to "Low Voltage Positive Emitter Coupled Logic (LVPECL)" in the second paragraph, front page.
36	Modified Table 5 “Cortina Systems® LXT9785/LXT9785E RMII Signal Descriptions – PQFP”. Added last sentence to RXER0 through RXER7 signal description.
42	Modified Table 10 “Cortina Systems® LXT9785/LXT9785E Signal Detect – PQFP”.
42	Modified Table 11 “Cortina Systems® LXT9785/LXT9785E Network Interface Signal Descriptions – PQFP”,
43	Modified Table 13 “Cortina Systems® LXT9785/LXT9785E Miscellaneous Signal Descriptions – PQFP”. Added note to PREASEL signal description.
116	Modified Section 4.1, “Introduction”. Changed "Pseudo-ECL (PECL)" to "Low Voltage PECL (LVPECL)" in the first paragraph, second sentence.
119	Replace text under Section 4.2.1.3, “Fiber Interface”.
120	Modified Section 4.3.2, “Internal Loopback”.
130	Modified last sentence under Section 4.6.1.4, “Link Criteria”.
131	Modified text under Section 4.6.1.5, “Parallel Detection”. Added second paragraph.
136	Modified text under Section 4.7.4.3, “Receive Error”.
145	Changed "PECL" to "LVPECL in third paragraph, first sentence under Section 4.9.1, “100BASE-X Network Operations”.
146	Modified Figure 28 “Cortina Systems® LXT9785/LXT9785E Protocol Sublayers”.
148	Modified Section 4.9.3.3, “Carrier Sense/Data Valid (RMII)”. Changed “asynchronously to “synchronously.”
148	Modified text under Section 4.9.3.4, “Carrier Sense (SMII)”. Revised last sentence in first paragraph.
149	Modified paragraph under Section 4.9.3.6.3, “Polarity Correction”.
149	Replaced text under Section 4.9.3.7, “Fiber PMD Sublayer”.
150	Modified Section 4.10.1, “Preamble Handling”. Added text to last paragraph.
151	Modified first sentence under Section 4.10.4, “Jabber”.
152	Modified first paragraph of Section 4.11, “DTE Discovery Process”.
153	Modified Item 1 of Section 4.11.2, “Interaction between Processor, MAC, and PHY”.
158	Modified Section 4.12.3, “Out-of-Band Signaling”. Added sentence to end of first paragraph.
166	Replaced text under Section 5.2.5, “The Fiber Interface”.
170	Replaced Figure 36 “Recommended Cortina Systems® LXT9785/LXT9785E-to-3.3 V Fiber Transceiver Interface Circuitry”.
171	Replaced Figure 37 “Recommended Cortina Systems® LXT9785/LXT9785E-to-5 V Fiber Transceiver Interface Circuitry”.
173	Modified Table 52 “Cortina Systems® LXT9785/LXT9785E Operating Conditions”.
174	Modified Table 53 “Cortina Systems® LXT9785/LXT9785E Digital I/O DC Electrical Characteristics (VCCIO = 2.5 V +/- 5%)”.
175	Modified Table 54 “Cortina Systems® LXT9785/LXT9785E Digital I/O DC Electrical Characteristics (VCCIO = 3.3 V +/- 5%)”.
175	Added Table 55 “Cortina Systems® LXT9785/LXT9785E Digital I/O DC Electrical Characteristics – SD Pins”.
176	Modified Table 58 “Cortina Systems® LXT9785/LXT9785E 100BASE-FX Transceiver Characteristics”.

Revision Number: 006 (INTERNAL RELEASE) Revision Date: June 10, 2003	
Page	**Description**
200	Modified Table 83 “Control Register (Address 0)”.
201	Modified Table 84 “Status Register (Address 1)”.
204	Modified Table 87 “Auto-Negotiation Advertisement Register (Address 4)”.
205	Modified Table 88 “Auto-Negotiation Link Partner Base Page Ability Register (Address 5)”.
207	Modified Table 91 “Auto-Negotiation Link Partner Next Page Receive Register (Address 8)”.
207	Modified Table 92 “Port Configuration Register (Address 16, Hex 10)”.
209	Modified Table 93 “Quick Status Register (Address 17, Hex 11)”.
211	Modified Table 94 “Interrupt Enable Register (Address 18, Hex 12)”
212	Modified Table 95 “Interrupt Status Register (Address 19, Hex 13)”. Changed all references of RO/SC to R/LH.
214	Modified Table 97 “Receive Error Count Register (Address 21, Hex 15)”.
215	Modified Table 98 “RMII Out-of-Band Signaling Register (Address 25, Hex 19)”. Added note to Register bit 25.0.
216	Modified Table 99 “Trim Enable Register (Address 27, Hex 1B)”.
227	Modified Table 103 “Product Information”.

Revision Number: 005 Revision Date: January 2002	
Page	**Description**
1	Added bullet to Product Features
49	Modified Table 12 “Cortina Systems® LXT9785/LXT9785E Miscellaneous Signal Descriptions” (Added FIFOSEL1 and FIFOSEL0)
70	Added Section 2.6.1.6, “Reliable Link Establishment While Auto MDI/MDIX is Enabled in Forced Speed Mode”
109	Modified Figure 38 “Recommended Cortina Systems® LXT9785/LXT9785E-to-3.3 V Fiber Transceiver Interface Circuitry”
110	Added Figure 39 “Recommended Cortina Systems® LXT9785/LXT9785E-to-5 V Fiber Transceiver Interface Circuitry”
111	Added Figure 40 “ON Semiconductor Triple PECL-to-LVPECL Translator”
112	Modified Table 28 “Absolute Maximum Ratings”
112	Modified Table 29 “Operating Conditions”
114	Modified Table 31 “Digital I/O DC Electrical Characteristics (VCCIO = 3.3 V +/- 5%)”(Output low voltage SD pins - Max)
129	Modified Figure 53 “RMII - 100BASE-TX Receive Timing” and Table 49 “RMII - 100BASE-TX Receive Timing Parameters”
131	Modified Figure 55 “RMII - 100BASE-FX Receive Timing” and Table 51 “RMII - 100BASE-FX Receive Timing Parameters”
133	Modified Figure 57 “RMII - 10BASE-T Receive Timing” and Table 53 “RMII - 10BASE-T Receive Timing Parameters”

Revision Number: 005 Revision Date: January 2002	
Page	**Description**
146	Modified Table 69 “Port Configuration Register (Address 16, Hex 10)” (Bits 16.5 and 16.6)
148	Modified Table 71 “Interrupt Enable Register (Address 18, Hex 12)”
168	Added product ordering table and diagram.

Revision Number: 003 Revision Date: April 2001	
Page	**Description**
1	Modified and added new language to front page.
61	Reset: Modified language in first paragraph.
85	Added new section on DTE discovery.
93	Supported JTAG Instructions table: replaced long hit streams with hex.
97	LED Circuit: Modified paragraph language.
97	LED Circuit diagram: Modified diagram.
99	Replaced Typical Fiber Interface diagram.
102	Required Clock Characteristics table: Replaced SMII Input frequency and RMII Input frequency symbol with “f”.
122	Auto-Negotiation and Fast Link Pulse Timing Parameters: FLP burst width under Typ = 2.
126	Control Register table: Modified table and table notes.
128	PHY Identification Register 2 (Address 3): Modified table.
128	PHY Identifier Bit Mapping: Modified diagram.
131	Auto-Negotiation Expansion: Modified table and table notes.
133	Port Configuration Register table: Modified table and table notes.
140	Trim Enable Register: Modified table (DTE Discovery).
141	Modified Register Bit Map table.

1.0 Introduction

This document contains information on the Cortina Systems® LXT9785 and LXT9785E Advanced 8-Port 10/100 Mbps PHY Transceivers.

1.1 What You Will Find in This Document

This document contains the following sections:

- Section 2.0, *Block Diagram*, on page 19
- Section 3.0, *Pin/Ball Assignments and Signal Descriptions*, on page 20
  This section contains pin/ball assignments and signal descriptions for the following:
  - Section 3.1, *PQFP Pin Assignments*, on page 20
  - Section 3.2, *PQFP Signal Descriptions*, on page 36
  - Section 3.3, *BGA23 Ball Assignments*, on page 51
  - Section 3.4, *BGA23 Signal Descriptions*, on page 79
  - Section 3.5, *BGA15 Ball Assignments*, on page 97
  - Section 3.6, *BGA15 Signal Descriptions*, on page 106
- Section 4.0, *Functional Description*, on page 113
- Section 5.0, *Application Information*, on page 161
- Section 6.0, *Test Specifications*, on page 170
- Section 7.0, *Register Definitions*, on page 191
- Section 8.0, *Package Specifications*, on page 212
- Section 9.0, *Ordering Information*, on page 219

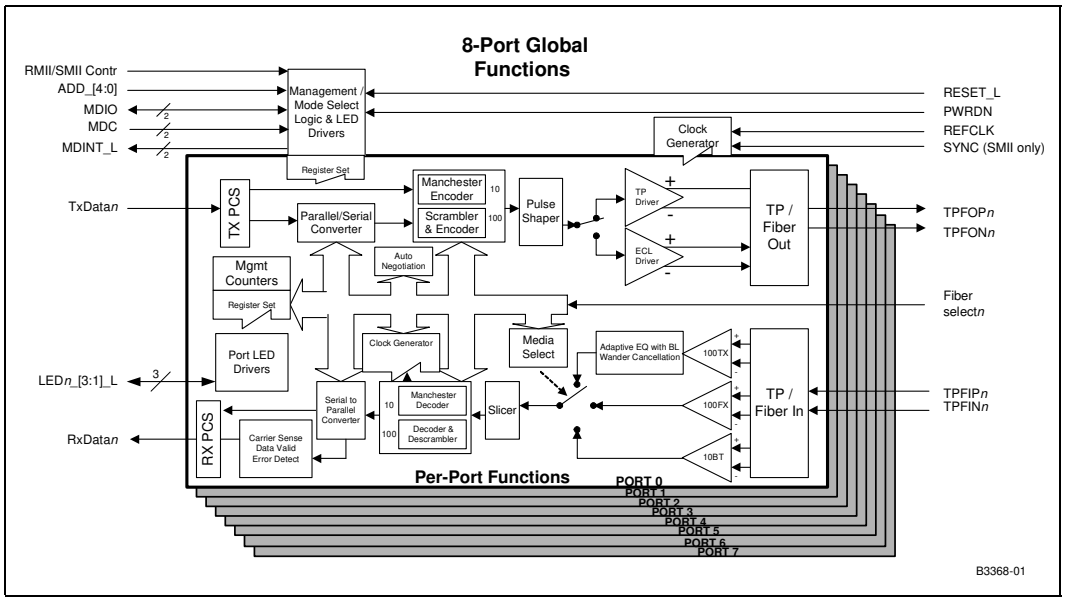
1.2 Related Documents

Document	Document Number
Cortina Systems® LXT9785/LXT9785E Design and Layout Guide	249509
Cortina Systems® LXT9785/LXT9785E Specification Update	249357
Cortina Systems® LXT9785/LXT9785E 100BASE-FX Fiber Optic Transceivers: Connecting a PECL/LVPECL Interface	250781
IP Telephony and DTE Discovery Using Cortina Systems® Ethernet PHYs	249611

2.0 Block Diagram

Figure 1 provides the LXT9785/LXT9785E block diagram.

Figure 1 Block Diagram



3.0 Pin/ Ball Assignments and Signal Descriptions

3.1 PQFP Pin Assignments

The following sections show PQFP pin assignments and signal descriptions:

- Section 3.1.1, *PQFP Pin Assignments – RMII Configuration*, on page 20
- Section 3.1.2, *PQFP Pin Assignments – SMII Configuration*, on page 26
- Section 3.1.3, *PQFP Pin Assignments – SS-SMII Configuration*, on page 31

Table 1 lists the acronyms and descriptions for signal types.

Table 1 Signal Type Descriptions

Acronym	Description
AI	Analog Input
AO	Analog Output
I	Input
O	Output
OD	Open Drain Output
ST	Schmitt Triggered Input
TS	Three-State-able Output
SL	Slew-rate Limited Output
IP	Weak Internal Pull-Up
ID	Weak Internal Pull-Down

3.1.1 PQFP Pin Assignments – RMII Configuration

Figure 2 and Table 2, *RMII PQFP Pin List*, on page 22 provide LXT9785/LXT9785E RMII PQFP pin assignments.

Figure 2 RMII 208-Pin PQFP Assignments

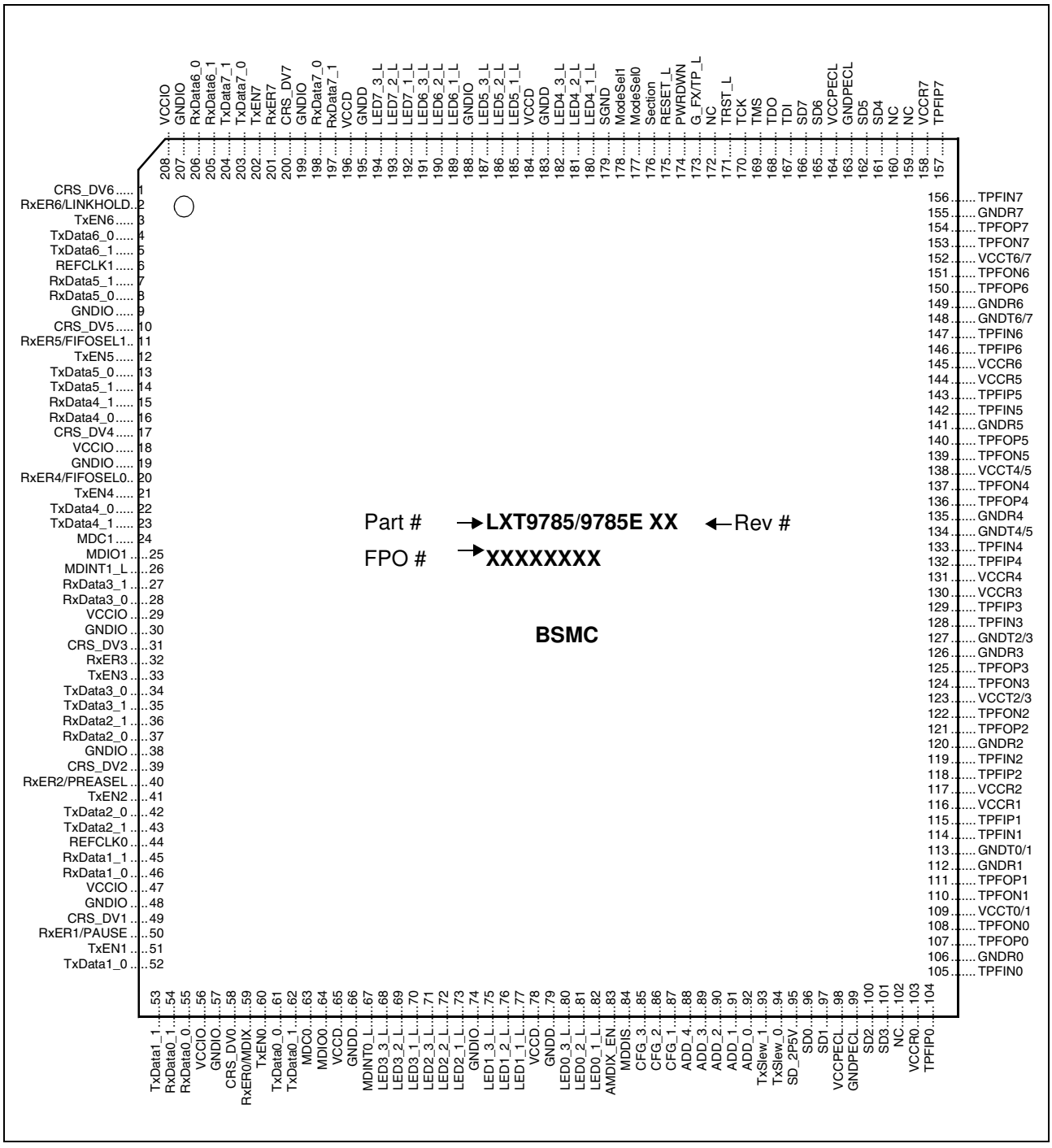


Table 2 RMII PQFP Pin List

Pin	Symbol	Type	Reference for Full Description
1	CRS_DV6	O, TS, SL	Table 5
2	RxER6/ LINKHOLD	O, TS, SL, ID, I, ST	Table 5 Table 13
3	TxEN6	I, ID	Table 5
4	TxData6_0	I, ID	Table 5
5	TxData6_1	I, ID	Table 5
6	REFCLK1	I	Table 5
7	RxData5_1	O, TS, ID	Table 5
8	RxData5_0	O, TS	Table 5
9	GNDIO	–	Table 15
10	CRS_DV5	O, TS, SL	Table 5
11	RxER5 / FIFOSEL1	O, TS, SL, ID, I, ST	Table 5 Table 13
12	TxEN5	I, ID	Table 5
13	TxData5_0	I, ID	Table 5
14	TxData5_1	I, ID	Table 5
15	RxData4_1	O, TS,ID	Table 5
16	RxData4_0	O, TS	Table 5
17	CRS_DV4	O, TS, SL	Table 5
18	VCCIO	–	Table 15
19	GNDIO	–	Table 15
20	RxER4 / FIFOSEL0	O, TS, SL, ID, I, ST	Table 5 Table 13
21	TxEN4	I, ID	Table 5
22	TxData4_0	I, ID	Table 5
23	TxData4_1	I, ID	Table 5
24	MDC1	I, ST, ID	Table 8
25	MDIO1	I/O, TS, SL, IP	Table 8
26	MDINT1_L	OD, TS, SL, IP	Table 8
27	RxData3_1	O, TS, ID	Table 5
28	RxData3_0	O, TS	Table 5
29	VCCIO	–	Table 15
30	GNDIO	–	Table 15
31	CRS_DV3	O, TS, SL	Table 5
32	RxER3	O, TS, SL, ID	Table 5
33	TxEN3	I, ID	Table 5
34	TxData3_0	I, ID	Table 5
35	TxData3_1	I, ID	Table 5
36	RxData2_1	O, TS, ID	Table 5
37	RxData2_0	O, TS	Table 5
38	GNDIO	–	Table 15
39	CRS_DV2	O, TS, SL	Table 5
40	RxER2 (PREASEL)	O, TS, SL, ID, I, ST	Table 5 Table 13
41	TxEN2	I, ID	Table 5
42	TxData2_0	I, ID	Table 5
43	TxData2_1	I, ID	Table 5
44	REFCLK0	I	Table 5
45	RxData1_1	O, TS, ID	Table 5
46	RxData1_0	O, TS	Table 5
47	VCCIO	–	Table 15
48	GNDIO	–	Table 15
49	CRS_DV1	O, TS, SL	Table 5
50	RxER1/ PAUSE	O, TS, SL, ID, I, ST	Table 5
51	TxEN1	I, ID	Table 5
52	TxData1_0	I, ID	Table 5
53	TxData1_1	I, ID	Table 5
54	RxData0_1	O, TS, ID	Table 5
55	RxData0_0	O, TS	Table 5
56	VCCIO	–	Table 15
57	GNDIO	–	Table 15
58	CRS_DV0	O, TS, SL	Table 5

Pin	Symbol	Type	Reference for Full Description
59	RxER0/ MDIX	O, TS, SL, ID, I, ST	Table 5
60	TxEN0	I, ID	Table 5
61	TxData0_0	I, ID	Table 5
62	TxData0_1	I, ID	Table 5
63	MDC0	I, ST, ID	Table 8
64	MDIO0	I/O, TS, SL, IP	Table 8
65	VCCD	–	Table 15
66	GNDD	–	Table 15
67	MDINT0_L	OD, TS, SL, IP	Table 8
68	LED3_3_L	OD, TS, SO, IP	Table 14
69	LED3_2_L	OD, TS, SL, IP	Table 14
70	LED3_1_L	OD, TS, SL, IP	Table 14
71	LED2_3_L	OD, TS, SL, IP	Table 14
72	LED2_2_L	OD, TS, SL, IP	Table 14
73	LED2_1_L	OD, TS, SL, IP	Table 14
74	GNDIO	–	Table 15
75	LED1_3_L	OD, TS, SL, IP	Table 14
76	LED1_2_L	OD, TS, SL, IP	Table 14
77	LED1_1_L	OD, TS, SL, IP	Table 14
78	VCCD	–	Table 15
79	GNDD	–	Table 15
80	LED0_3_L	OD, TS, SL, IP	Table 14
81	LED0_2_L	OD, TS, SL, IP	Table 14
82	LED0_1_L	OD, TS, SL, IP	Table 14
83	AMDIX_EN	I, ST, IP	Table 13
84	MDDIS	I, ST, ID	Table 9
85	CFG_3	I, ST, ID	Table 13
86	CFG_2	I, ST, ID	Table 13
87	CFG_1	I, ST, ID	Table 13
88	ADD_4	I, ST, ID	Table 13
89	ADD_3	I, ST, ID	Table 13
90	ADD_2	I, ST, ID	Table 13
91	ADD_1	I, ST, ID	Table 13
92	ADD_0	I, ST, ID	Table 13
93	TxSLEW_1	I, ST, ID	Table 13
94	TxSLEW_0	I, ST, ID	Table 13
95	SD_2P5V	I, ST, ID	Table 10
96	SD0	I	Table 10
97	SD1	I	Table 10
98	VCCPECL	–	Table 15
99	GNDPECL	–	Table 15
100	SD2	I	Table 10
101	SD3	I	Table 10
102	NC	–	Table 17
103	VCCR0	–	Table 15
104	TPFIP0	AO/AI	Table 11
105	TPFIN0	AO/AI	Table 11
106	GNDR0	–	Table 15
107	TPFOP0	AO/AI	Table 11
108	TPFON0	AO/AI	Table 11
109	VCCT0/1	–	Table 15
110	TPFON1	AO/AI	Table 11
111	TPFOP1	AO/AI	Table 11
112	GNDR1	–	Table 15
113	GNDT0/1	–	Table 15
114	TPFIN1	AO/AI	Table 11
115	TPFIP1	AO/AI	Table 11
116	VCCR1	–	Table 15
117	VCCR2	–	Table 15
118	TPFIP2	AO/AI	Table 11
119	TPFIN2	AO/AI	Table 11
120	GNDR2	–	Table 15
121	TPFOP2	AO/AI	Table 11
122	TPFON2	AO/AI	Table 11
123	VCCT2/3	–	Table 15
124	TPFON3	AO/AI	Table 11

Pin	Symbol	Type	Reference for Full Description
125	TPFOP3	AO/AI	Table 11
126	GNDR3	–	Table 15
127	GNDT2/3	–	Table 15
128	TPFIN3	AO/AI	Table 11
129	TPFIP3	AO/AI	Table 11
130	VCCR3	–	Table 15
131	VCCR4	–	Table 15
132	TPFIP4	AO/AI	Table 11
133	TPFIN4	AO/AI	Table 11
134	GNDT4/5	–	Table 15
135	GNDR4	–	Table 15
136	TPFOP4	AO/AI	Table 11
137	TPFON4	AO/AI	Table 11
138	VCCT4/5	–	Table 15
139	TPFON5	AO/AI	Table 11
140	TPFOP5	AO/AI	Table 11
141	GNDR5	–	Table 15
142	TPFIN5	AO/AI	Table 11
143	TPFIP5	AO/AI	Table 11
144	VCCR5	–	Table 15
145	VCCR6	–	Table 15
146	TPFIP6	AO/AI	Table 11
147	TPFIN6	AO/AI	Table 11
148	GNDT6/7	–	Table 15
149	GNDR6	–	Table 15
150	TPFOP6	AO/AI	Table 11
151	TPFON6	AO/AI	Table 11
152	VCCT6/7	–	Table 15
153	TPFON7	AO/AI	Table 11
154	TPFOP7	AO/AI	Table 11
155	GNDR7	–	Table 15
156	TPFIN7	AO/AI	Table 11
157	TPFIP7	AO/AI	Table 11
158	VCCR7	–	Table 15
159	NC	–	Table 17
160	NC	–	Table 17
161	SD4	I	Table 10
162	SD5	I	Table 10

Pin	Symbol	Type	Reference for Full Description
163	GNDPECL	–	Table 15
164	VCCPECL	–	Table 15
165	SD6	I	Table 10
166	SD7	I	Table 10
167	TDI	I, ST, IP	Table 12
168	TDO	O, TS	Table 12
169	TMS	I, ST, IP	Table 12
170	TCK	I, ST, ID	Table 12
171	TRST_L	I, ST, IP	Table 12
172	NC	–	Table 17
173	G_FX/TP_L	I, ST, ID	Table 13
174	PWRDWN	I, ST, ID	Table 13
175	RESET_L	I, ST, IP	Table 13
176	SECTION	I, ST, ID	Table 13
177	ModeSel0	I, ST, ID	Table 13
178	ModeSel1	I, ST, ID	Table 13
179	SGND	–	Table 15
180	LED4_1_L	OD, TS, SL, IP	Table 14
181	LED4_2_L	OD, TS, SL, IP	Table 14
182	LED4_3_L	OD, TS, SL, IP	Table 14
183	GNDD	–	Table 15
184	VCCD	–	Table 15
185	LED5_1_L	OD, TS, SL, IP	Table 14
186	LED5_2_L	OD, TS, SL, IP	Table 14
187	LED5_3_L	OD, TS, SL, IP	Table 14
188	GNDIO	–	Table 15
189	LED6_1_L	OD, TS, SL, IP	Table 14
190	LED6_2_L	OD, TS, SL, IP	Table 14
191	LED6_3_L	OD, TS, SL, IP	Table 14
192	LED7_1_L	OD, TS, SL, IP	Table 14
193	LED7_2_L	OD, TS, SL, IP	Table 14

Pin	Symbol	Type	Reference for Full Description
194	LED7_3_L	OD, TS, SL, IP	Table 5
195	GNDD	–	Table 15
196	VCCD	–	Table 15
197	RxData7_1	O, TS, ID	Table 5
198	RxData7_0	O, TS	Table 5
199	GNDIO	–	Table 15
200	CRS_DV7	O, TS, SL	Table 5
201	RxER7	O, TS, SL, ID	Table 5
202	TxEN7	I, ID	Table 5
203	TxData7_0	I, ID	Table 5
204	TxData7_1	I, ID	Table 5
205	RxData6_1	O, TS, ID	Table 5
206	RxData6_0	O, TS	Table 5
207	GNDIO	–	Table 15
208	VCCIO	–	Table 15