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RL78/L12

R01DS0157EJ0210

RENESAS MCU

Rev.2.10

Sep 30, 2016

Integrated LCD controller/driver, True Low Power Platform (as low as 62.5 $\mu\text{A}/\text{MHz}$, and 0.64 μA for RTC + LVD), 1.6 V to 5.5 V operation, 8 to 32 Kbyte Flash, 31 DMIPS at 24 MHz, for All LCD Based Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology

- 1.6 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 μA , (LVD enabled): 0.31 μA
- Halt (RTC + LVD): 0.64 μA
- Supports snooze
- Operating: 62.5 $\mu\text{A}/\text{MHz}$
- LCD operating current (Capacitor split method): 0.12 μA
- LCD operating current (Internal voltage boost method): 0.63 μA ($V_{\text{DD}} = 3.0 \text{ V}$)

16-bit RL78 CPU Core

- Delivers 31 DMIPS at maximum operating frequency of 24 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory

- Density: 8 KB to 32 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with flash shield window function

Data Flash Memory

- Data flash with background operation
- Data flash size: 2 KB size
- Erase cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 5.5 V

RAM

- 1 KB and 1.5 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator

- 24 MHz with +/- 1% accuracy over voltage (1.8 V to 5.5 V) and temperature (-20°C to 85°C)
- Pre-configured settings: 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz & 1 MHz

Reset and Supply Management

- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 14 setting options (Interrupt and/or reset function)

LCD Controller/Driver

- Up to 35 seg x 8 com or 39 seg x 4 com
- Supports capacitor split method, internal voltage boost method and resistance division method
- Supports waveform types A and B
- Supports LCD contrast adjustment (16 steps)
- Supports LCD blinking

Direct Memory Access (DMA) Controller

- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces

- Up to 1 x I²C multi-master
- Up to 2 x CSI/SPI (7-, 8-bit)
- Up to 1 x UART (7-, 8-, 9-bit)
- Up to 1 x LIN

Extended-Function Timers

- Multi-function 16-bit timers: Up to 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog

- ADC: Up to 10 channels, 10-bit resolution, 2.1 μs conversion time
- Supports 1.6 V
- Internal reference voltage (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)

- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock frequency detection
- ADC self-test

General Purpose I/O

- 5V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature

- T_A: -40 °C to +85 °C (A: Consumer applications)
- T_A: -40 °C to +105 °C (G: Industrial applications)

Package Type and Pin Count

From 7mm x 7mm to 12mm x 12mm
QFP: 32, 44, 48, 52, 64

○ ROM, RAM capacities

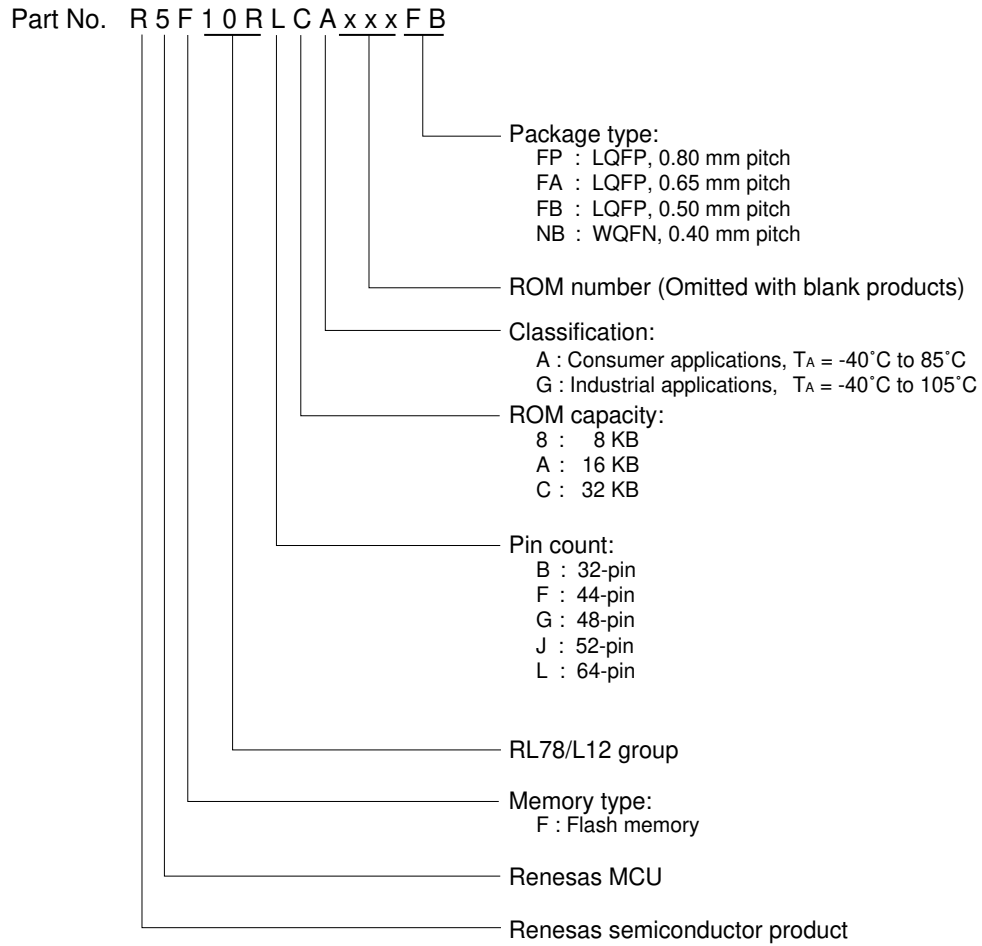
Flash ROM	Data flash	RAM	RL78/L12				
			32 pins	44 pins	48 pins	52 pins	64 pins
32 KB	2 KB	1.5 KB ^{Note}	R5F10RBC	R5F10RFC	R5F10RGC	R5F10RJC	R5F10RLC
16 KB	2 KB	1 KB ^{Note}	R5F10RBA	R5F10RFA	R5F10RGA	R5F10RJA	R5F10RLA
8KB	2 KB	1 KB ^{Note}	R5F10RB8	R5F10RF8	R5F10RG8	R5F10RJ8	–

Note In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Numbers

Figure 1-1 Part Number, Memory Size, and Package of RL78/L12



Pin count	Package	Fields of Application ^{Note}	Part Number
32 pins	32-pin plastic LQFP (7 × 7)	A G	R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP R5F10RB8GFP, R5F10RBAGFP, R5F10RBCGFP
44 pins	44-pin plastic LQFP (10 × 10)	A G	R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP R5F10RF8GFP, R5F10RFAGFP, R5F10RFCGFP
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	A G	R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB R5F10RG8GFB, R5F10RGAGFB, R5F10RGCGB
52 pins	52-pin plastic LQFP (10 × 10)	A G	R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA R5F10RJ8GFA, R5F10RJAGFA, R5F10RJCGFA
64 pins	64-pin plastic WQFN (8 × 8)	A G	R5F10RLAANB, R5F10RLCANB R5F10RLAGNB, R5F10RLCGNB
	64-pin plastic LQFP (fine pitch) (10 × 10)	A G	R5F10RLAAFB, R5F10RLCAFB R5F10RLAGFB, R5F10RLCGFB
	64-pin plastic LQFP (12 × 12)	A G	R5F10RLAAFA, R5F10RLCAFA R5F10RLAGFA, R5F10RLCGFA

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/L12**.

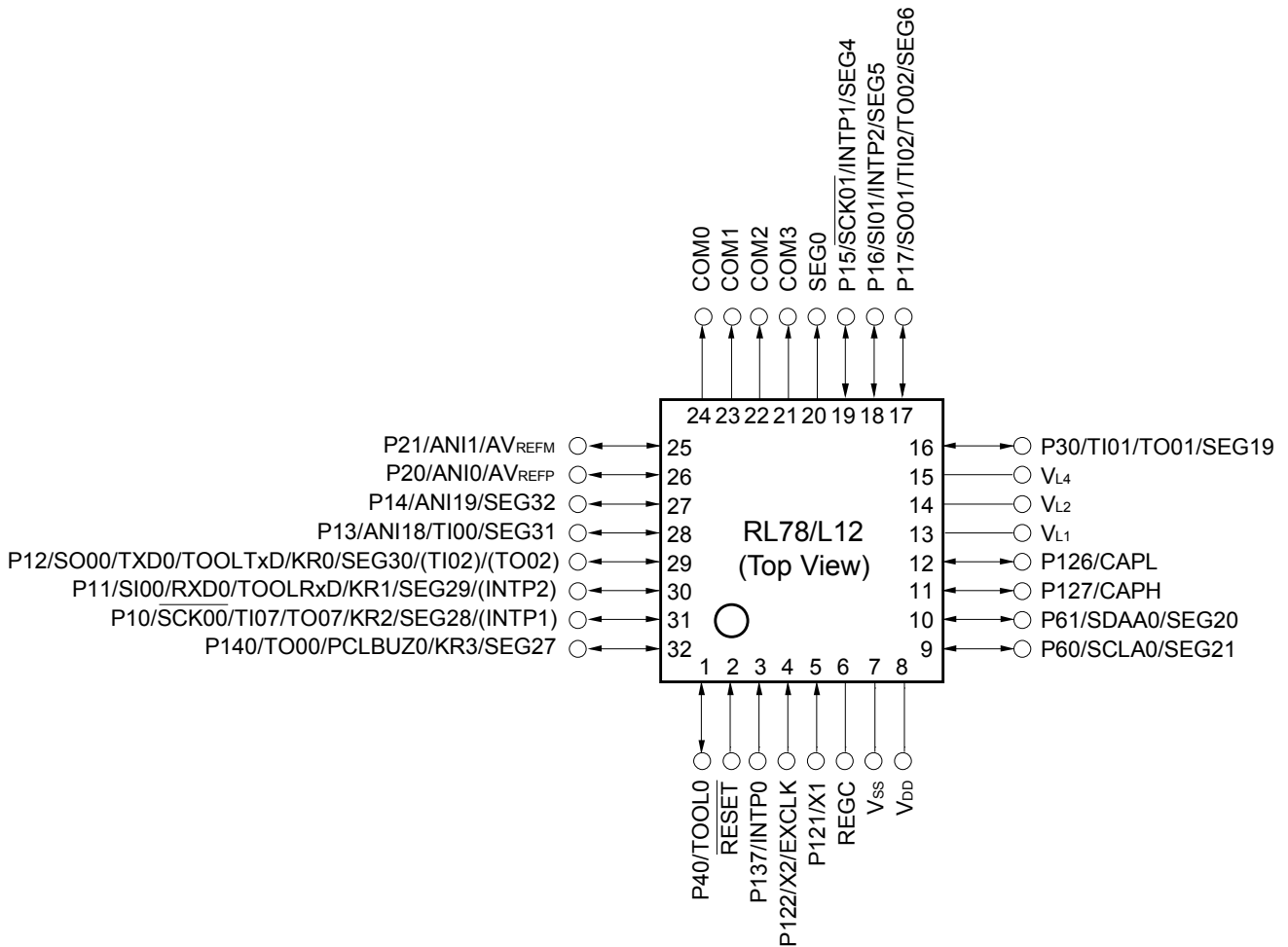
Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 32-pin products

- 32-pin plastic LQFP (7 × 7)

<R>



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

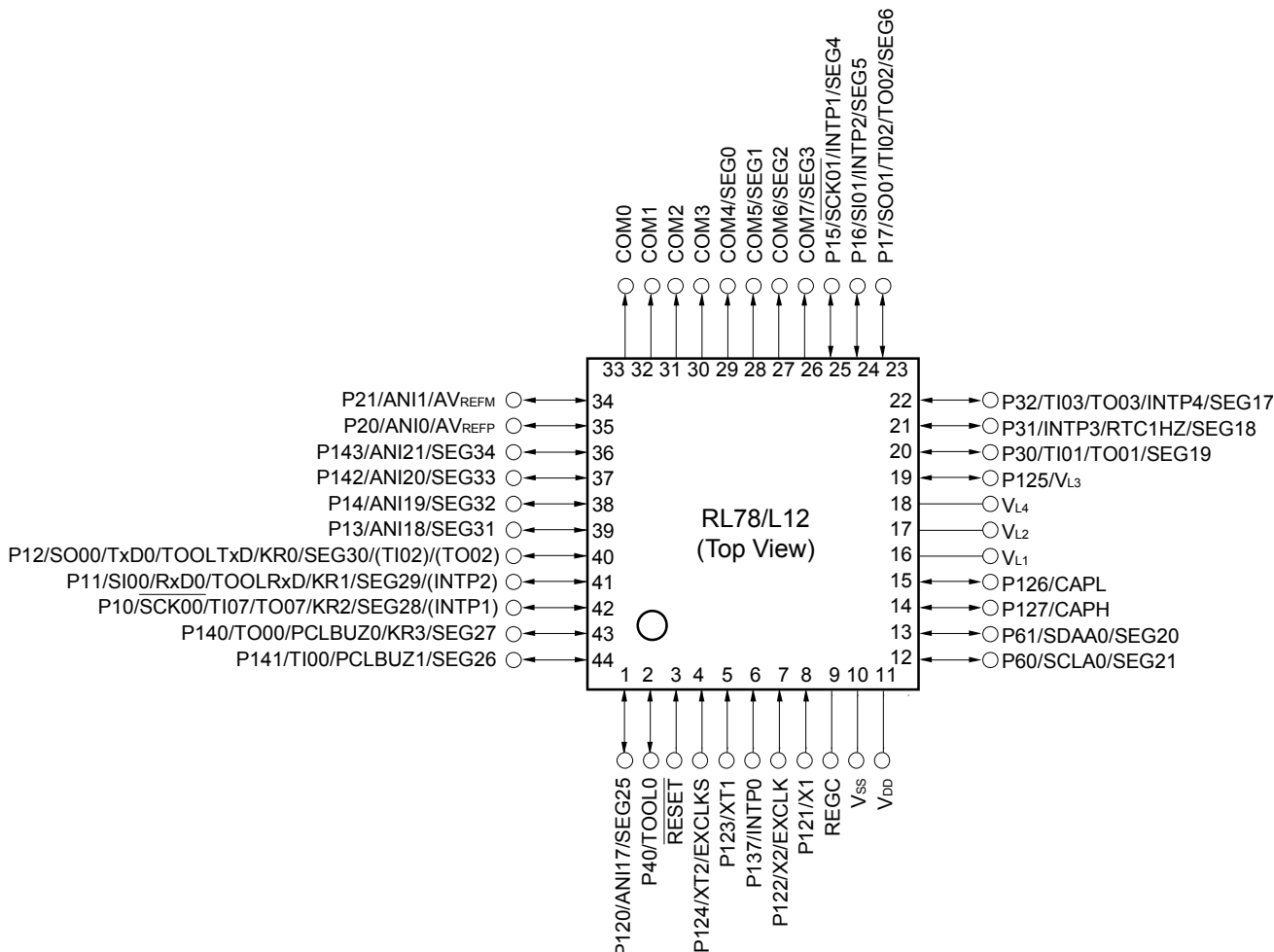
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 44-pin products

- 44-pin plastic LQFP (10 × 10)

<R>



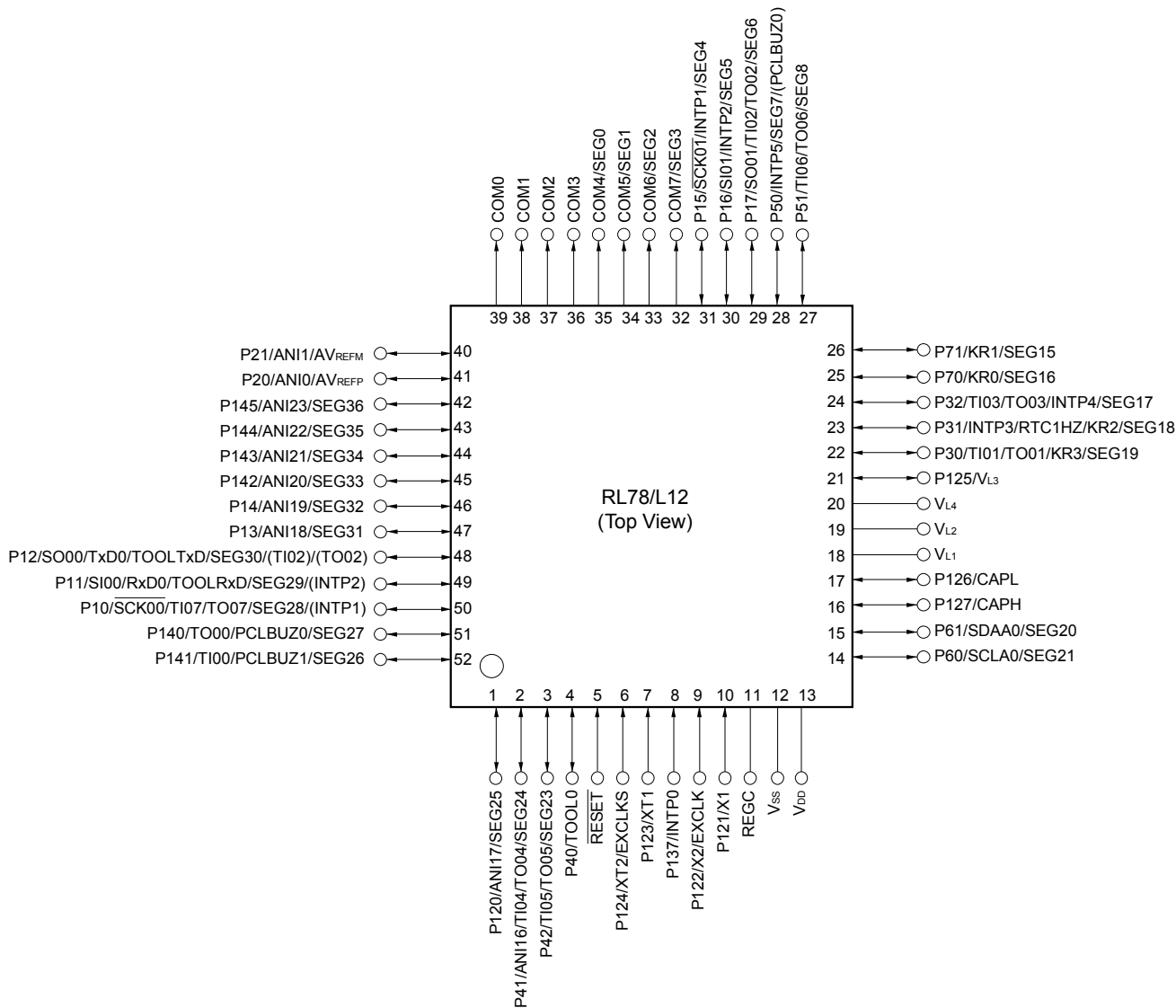
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.4 52-pin products

- 52-pin plastic LQFP (10 × 10)

<R>



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

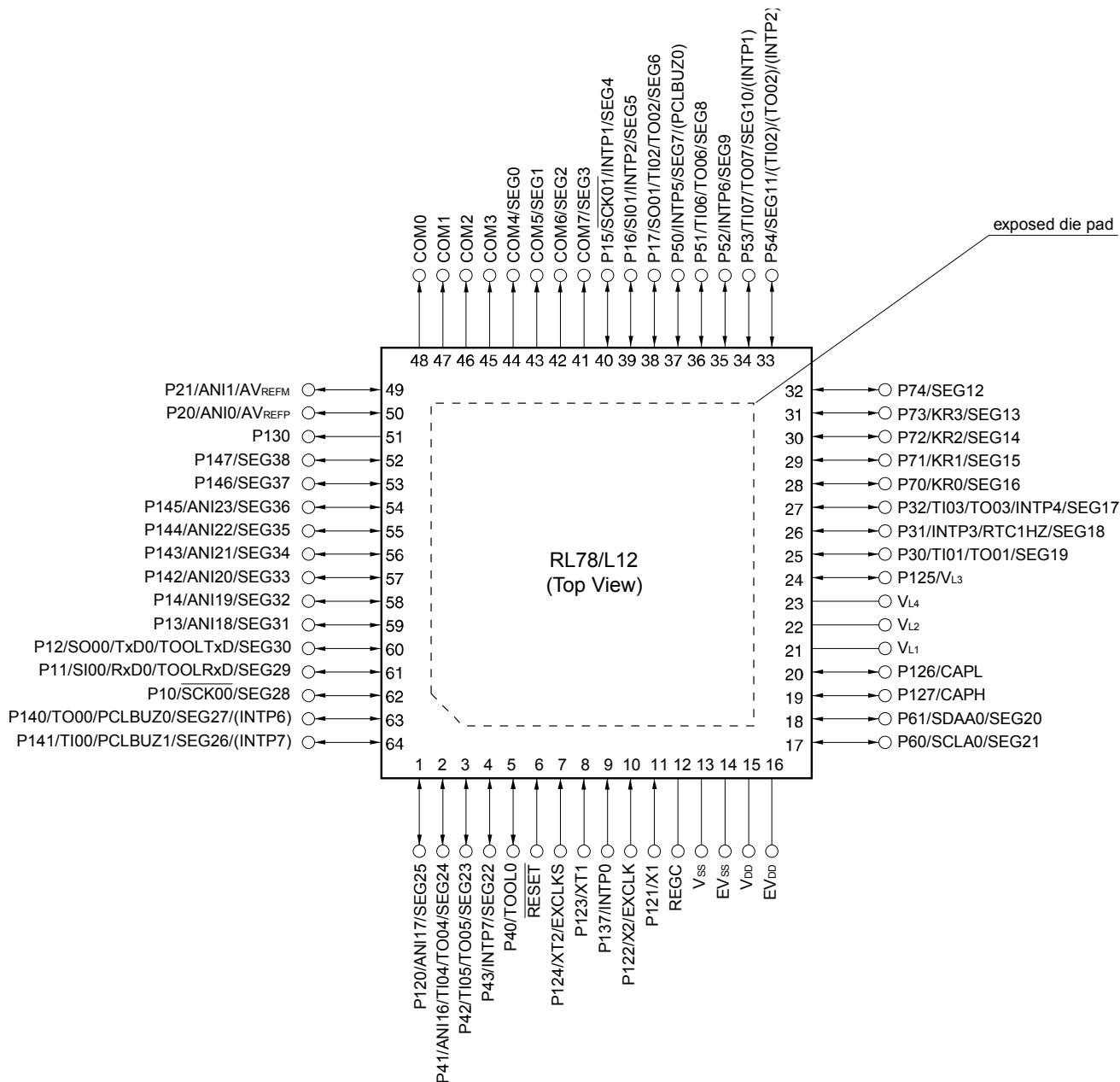
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.5 64-pin products

- 64-pin plastic WQFN (8 × 8)

<R>

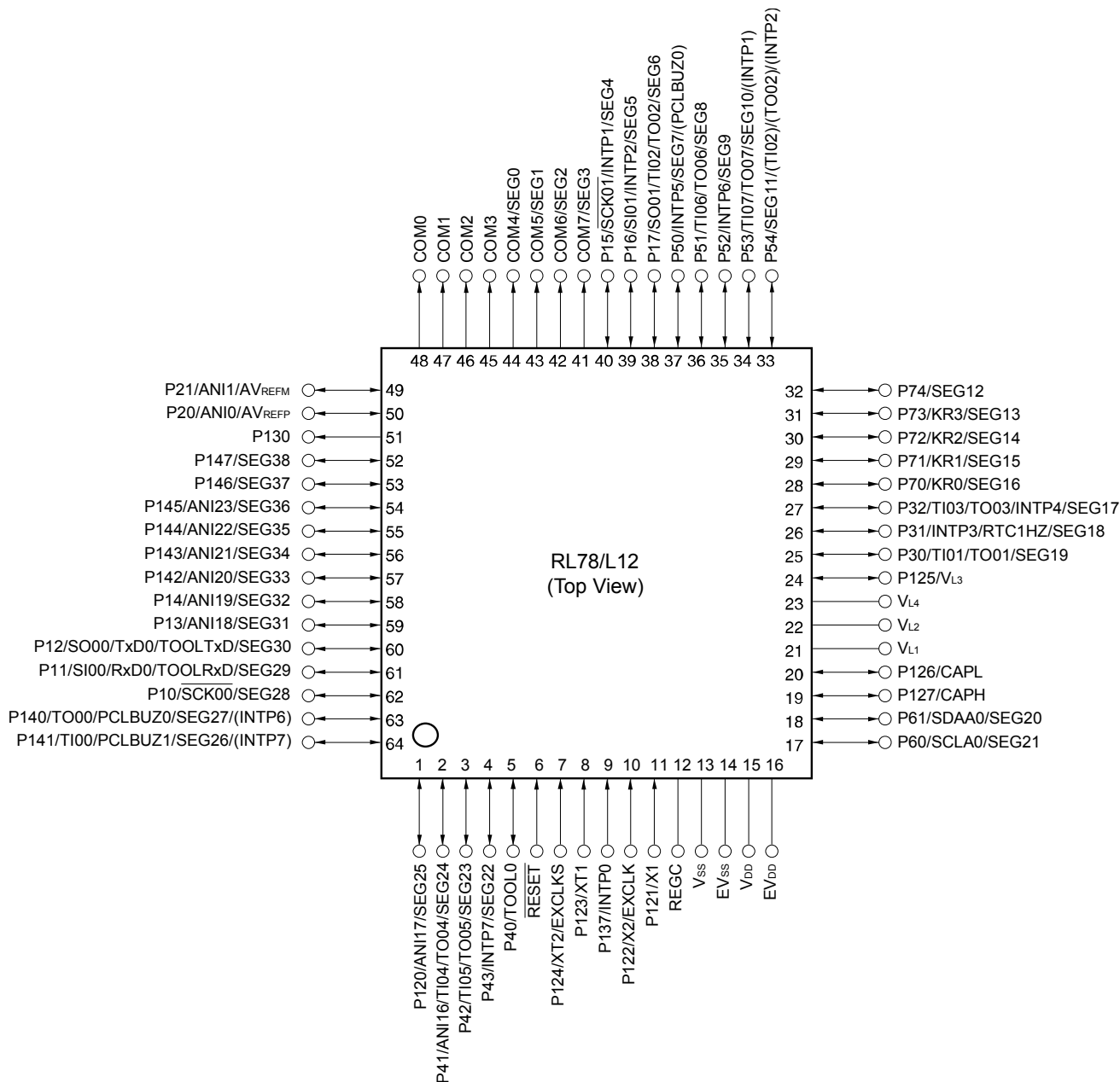


- Cautions**
1. Make EV_{SS} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the same potential as EV_{DD} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)

<R>



- Cautions**
1. Make EV_{SS} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the same potential as EV_{DD} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

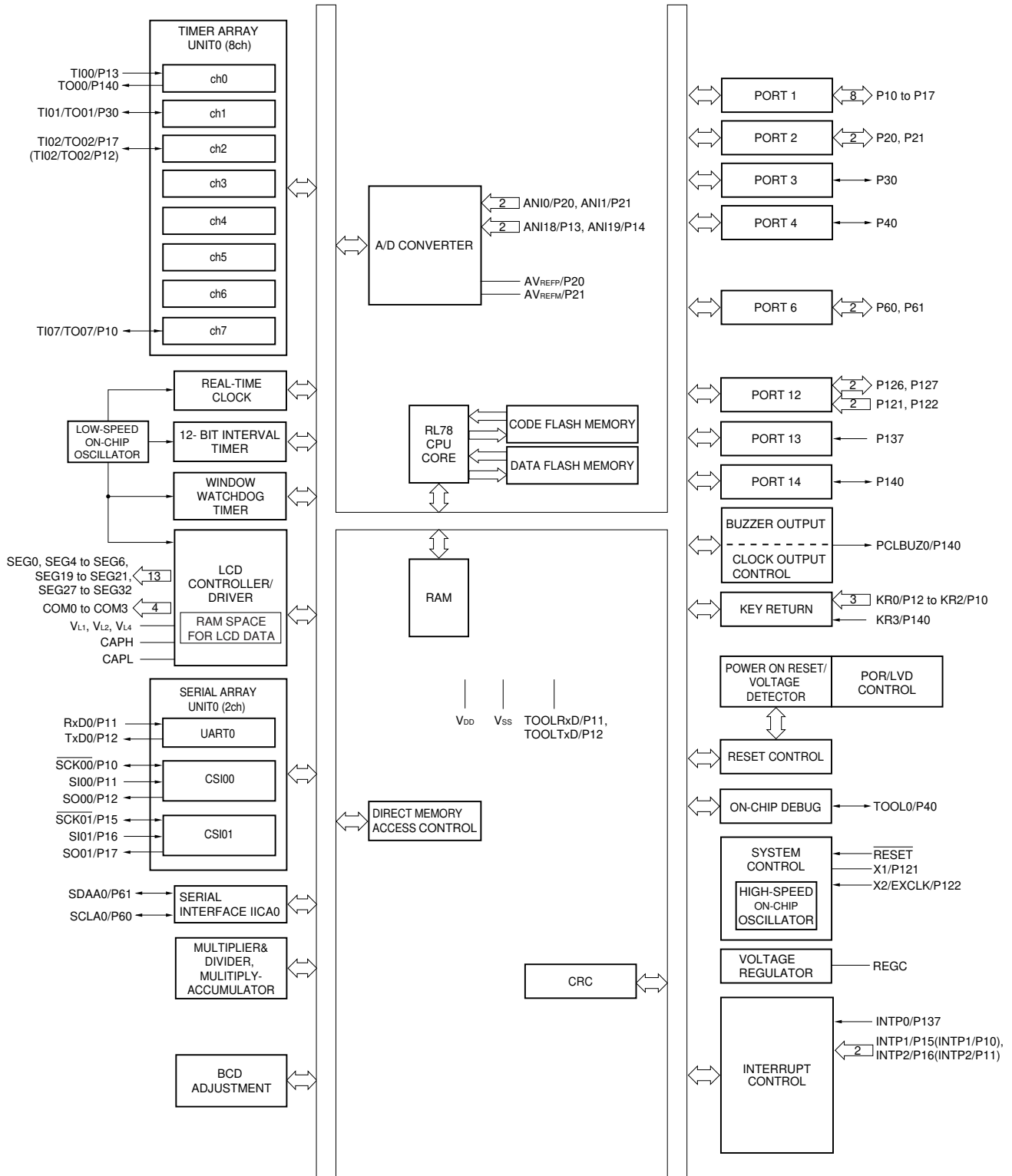
- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

ANI0, ANI1,		P130, P137:	Port 13
ANI16 to ANI23:	Analog Input	P140 to P147:	Port 14
AVREFM:	Analog Reference Voltage Minus	PCLBUZ0, PCLBUZ1:	Programmable Clock Output/Buzzer Output
AVREFP:	Analog Reference Voltage Plus	REGC:	Regulator Capacitance
CAPH, CAPL:	Capacitor for LCD	<u>RESET</u> :	Reset
COM0 to COM7,		RTC1HZ:	Real-time Clock Correction Clock (1 Hz) Output
EVDD:	Power Supply for Port	RxD0:	Receive Data
EVSS:	Ground for Port	<u>SCK00</u> , <u>SCK01</u> :	Serial Clock Input/Output
EXCLK:	External Clock Input (Main System Clock)	SCLA0:	Serial Clock Input/Output
		SDAA0:	Serial Data Input/Output
EXCLKS:	External Clock Input (Subsystem Clock)	SEG0 to SEG38:	LCD Segment Output
		SI00, SI01:	Serial Data Input
INTP0 to INTP7:	Interrupt Request From Peripheral	SO00, SO01:	Serial Data Output
		TI00 to TI07:	Timer Input
KR0 to KR3:	Key Return	TO00 to TO07:	Timer Output
P10 to P17:	Port 1	TOOL0:	Data Input/Output for Tool
P20, P21:	Port 2	TOOLRxD, TOOLTxD:	Data Input/Output for External Device
P30 to P32:	Port 3	TxD0:	Transmit Data
P40 to P43:	Port 4	V _{DD} :	Power Supply
P50 to P54:	Port 5	V _{L1} to V _{L4} :	LCD Power Supply
P60, P61:	Port 6	V _{SS} :	Ground
P70 to P74:	Port 7	X1, X2:	Crystal Oscillator (Main System Clock)
P120 to P127:	Port 12	XT1, XT2:	Crystal Oscillator (Subsystem Clock)

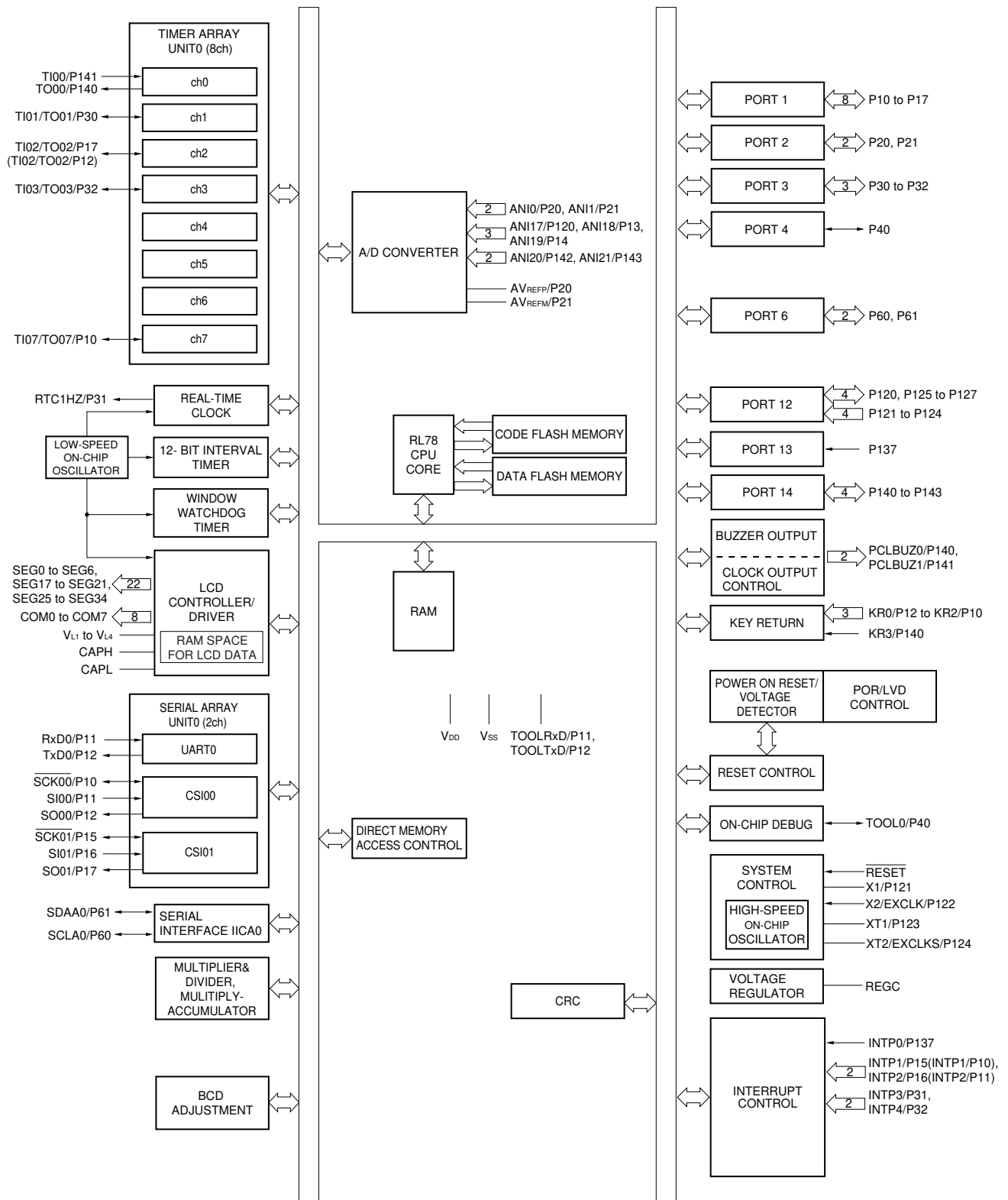
1.5 Block Diagram

1.5.1 32-pin products



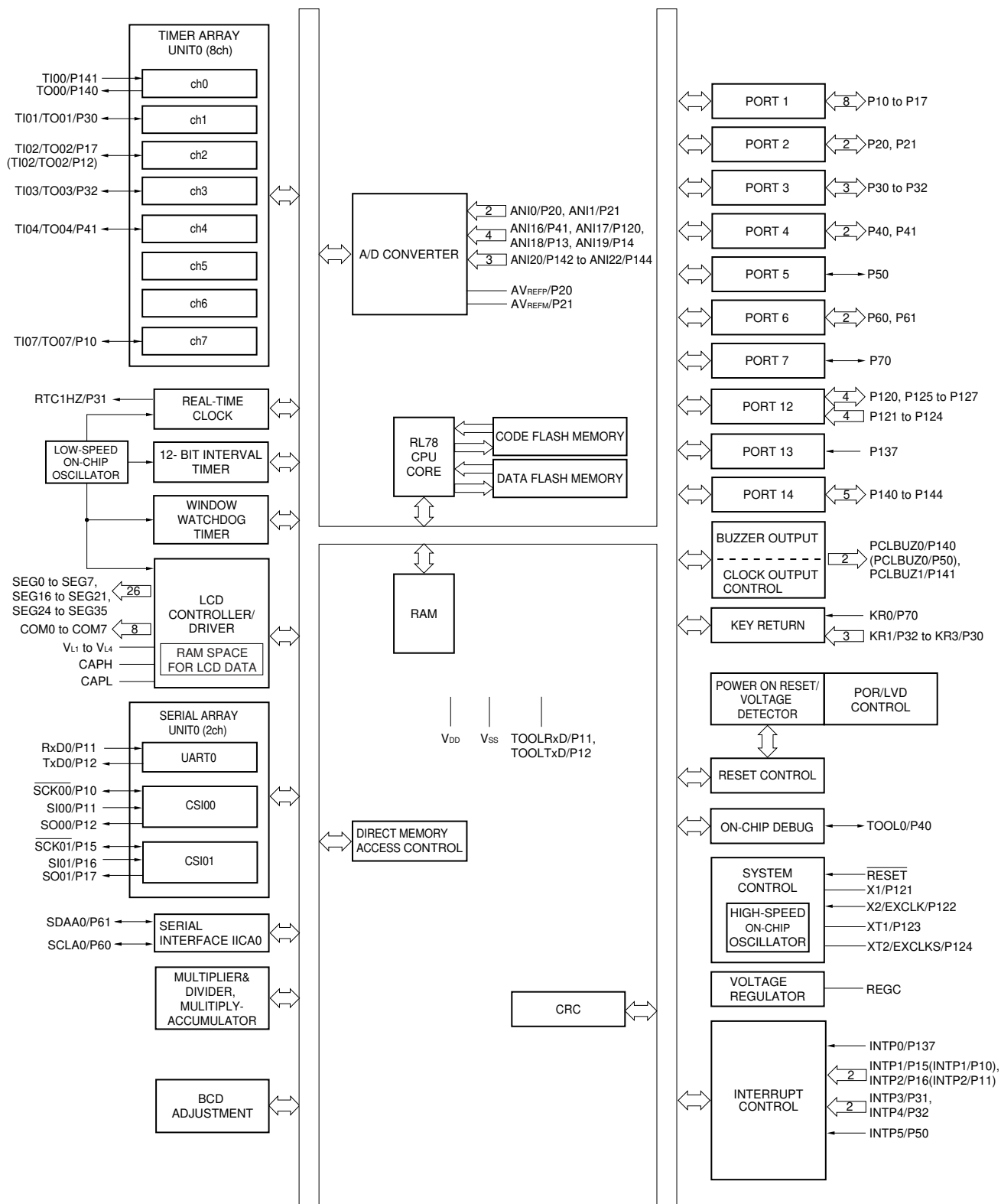
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.2 44-pin products



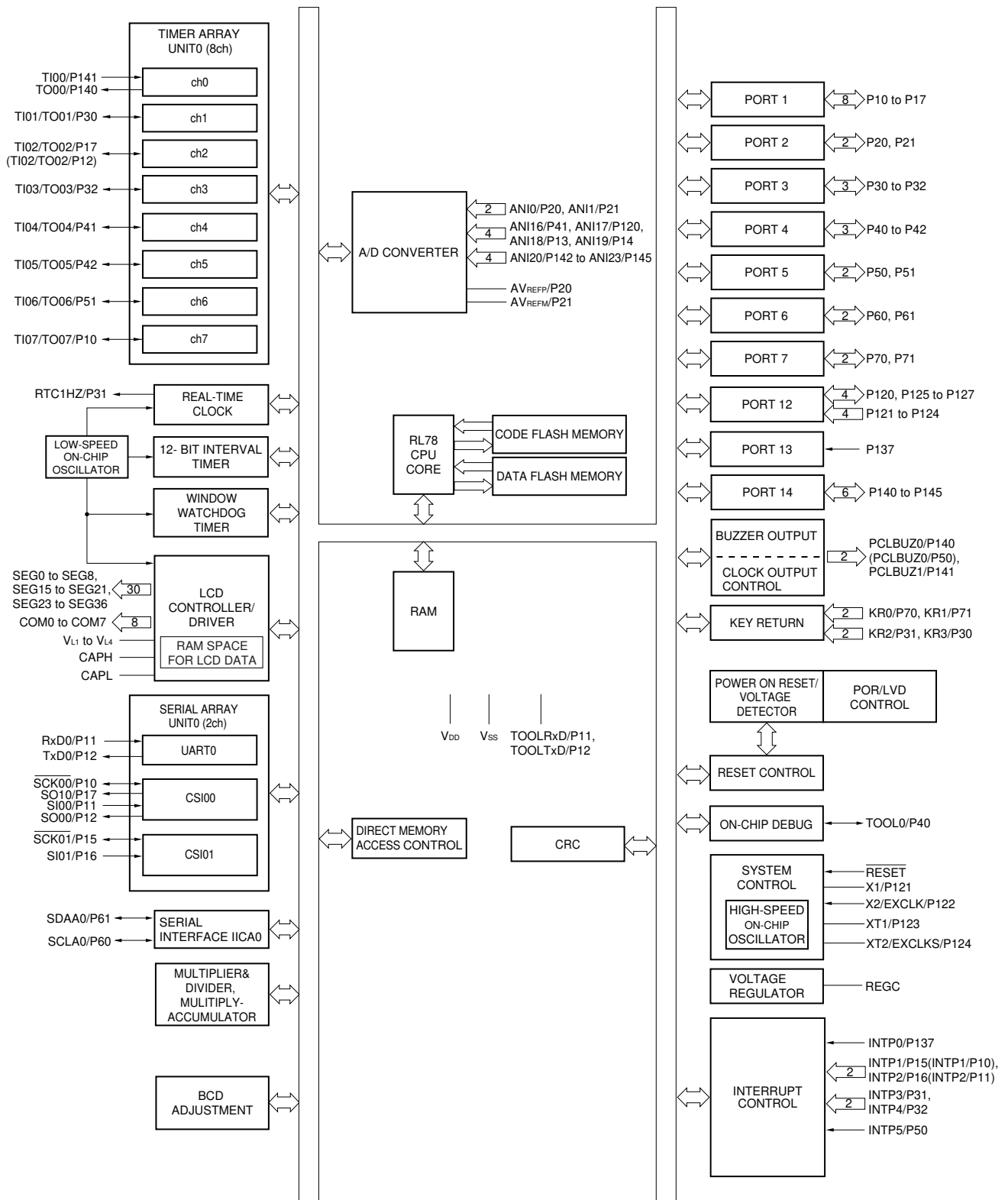
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.3 48-pin products



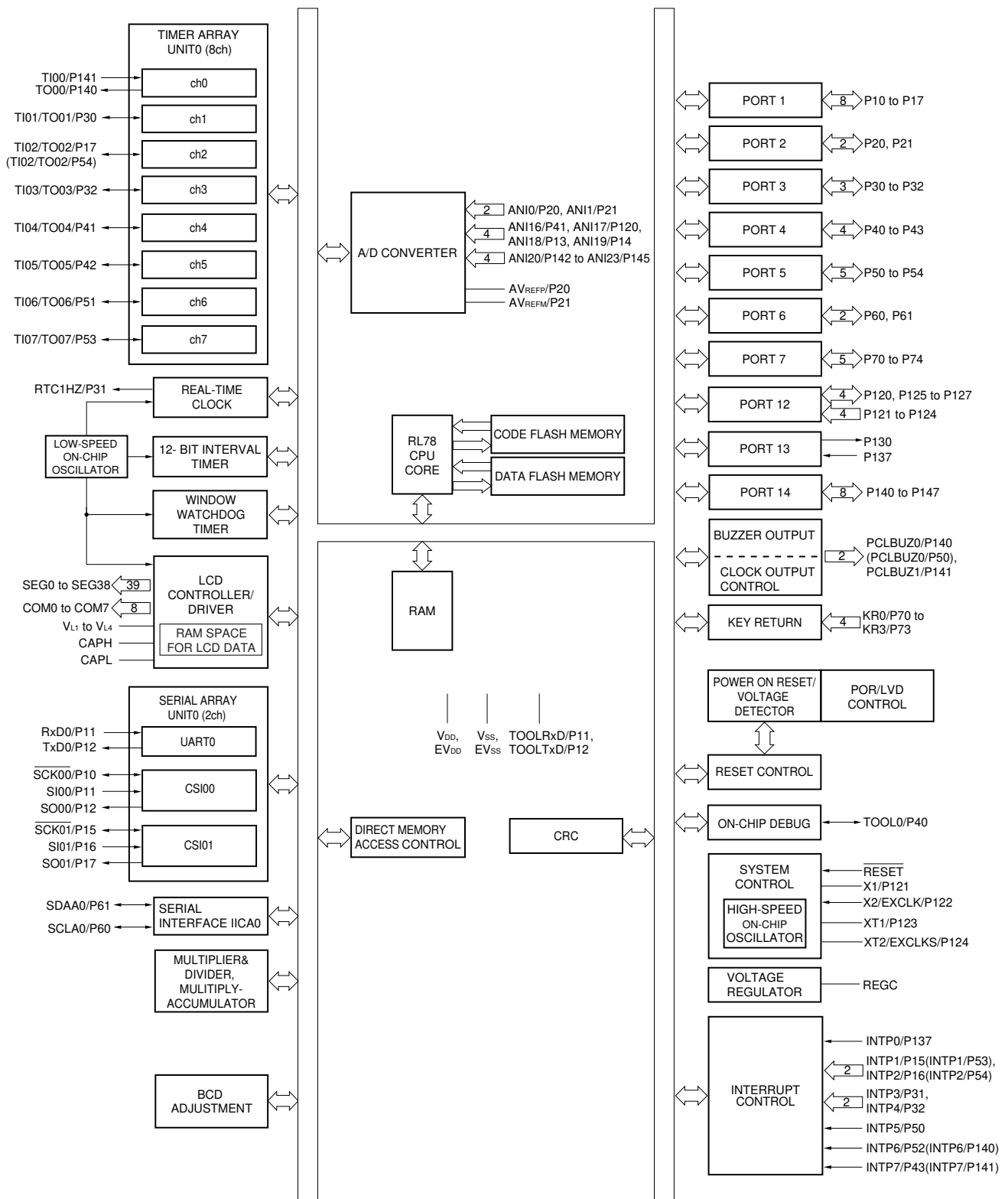
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.4 52-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.5 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		32-pin	44-pin	48-pin	52-pin	64-pin
		R5F10RBx	R5F10RFx	R5F10RGx	R5F10RJx	R5F10RLx
Code flash memory (KB)		8 to 32	8 to 32	8 to 32	8 to 32	16, 32
Data flash memory (KB)		2	2	2	2	2
RAM (KB)		1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}
Memory space		1 MB				
<R> Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) operation: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) operation: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) operation: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) operation: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)				
	High-speed on-chip oscillator clock	HS (high-speed main) operation: 1 to 24 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) operation: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) operation: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) operation: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)				
Subsystem clock		–	XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V			
Low-speed on-chip oscillator clock		Internal oscillation 15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.04167 μ s (High-speed on-chip oscillator clock: $f_{IH} = 24$ MHz operation)				
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)				
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)				
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 				
Total number of I/O port pins and pins dedicated to drive an LCD		28	40	44	48	58
I/O port	Total	20	29	33	37	47
	CMOS I/O	15	22	26	30	39
	CMOS input	3	5	5	5	5
	CMOS output	–	–	–	–	1
	N-ch open-drain I/O (E_{VDD} tolerance)	2	2	2	2	2
Pins dedicated to drive an LCD		8	11	11	11	11
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.				
Segment signal output		13	22 (18) ^{Note 2}	26 (22) ^{Note 2}	30 (26) ^{Note 2}	39 (35) ^{Note 2}
Common signal output		4	4 (8) ^{Note 2}			

Notes 1. In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used.

2. The values in parentheses are the number of signal outputs when 8 com is used.

(2/2)

Item		32-pin	44-pin	48-pin	52-pin	64-pin
		R5F10RBx	R5F10RFx	R5F10RGx	R5F10RJx	R5F10RLx
Timer	16-bit timer	8 channels	8 channels (with 1 channel remote control output function)			
	Watchdog timer	1 channel				
	Real-time clock (RTC)	1 channel				
	12-bit interval timer (IT)	1 channel				
	Timer output	4 channels (PWM outputs: 3 ^{Note 1})	5 channels (PWM outputs: 4 ^{Note 1})	6 channels (PWM outputs: 5 ^{Note 1})	8 channels (PWM outputs: 7 ^{Note 1})	
	RTC output	–	1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz or)			
Clock output/buzzer output		1	2 • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
8/10-bit resolution A/D converter		4 channels	7 channels	9 channels	10 channels	10 channels
Serial interface		• CSI: 2 channel/UART (LIN-bus supported): 1 channel				
	I ² C bus	1 channel	1 channel	1 channel	1 channel	1 channel
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)				
DMA controller		2 channels				
Vectored interrupt sources	Internal	23	23	23	23	23
	External	4	6	7	7	9
Key interrupt		4				
Reset		• Reset by \overline{RESET} pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note 2} • Internal reset by RAM parity error • Internal reset by illegal-memory access				
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V • Power-down-reset: 1.50 ±0.04 V				
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)				
On-chip debug function		Provided				
Power supply voltage		$V_{DD} = 1.6$ to 5.5 V				
Operating ambient temperature		$T_A = -40$ to +85 °C				

Notes 1. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves).

2. The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (A, G: $T_A = -40$ to $+85^\circ\text{C}$)

This chapter describes the electrical specifications for the products "A: Consumer applications ($T_A = -40$ to $+85^\circ\text{C}$)" and "G: Industrial applications (with $T_A = -40$ to $+85^\circ\text{C}$)".

- Cautions**
- 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**
 - 2. With products not provided with an EV_{DD} , or EV_{SS} pin, replace EV_{DD} with V_{DD} , or replace EV_{SS} with V_{SS} .**

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

(1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{SS}		-0.5 to +0.3	V
REGC pin input voltage	V _{REGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 ^{Note 1}	V
Input voltage	V _{I1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I2}	P60, P61 (N-ch open-drain)	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I3}	P20, P21, P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Output voltage	V _{O1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{O2}	P20, P21	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI16 to ANI23	-0.3 to EV _{DD} + 0.3 and -0.3 to AV _{REF(+)} + 0.3 Notes 2, 3	V
	V _{AI2}	ANI0, ANI1	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF(+)} + 0.3 Notes 2, 3	V

- Notes**
1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
 2. Must be 6.5 V or lower.
 3. Do not exceed AV_{REF(+)} + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks**
1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
 2. AV_{REF(+)} : + side reference voltage of the A/D converter.
 3. V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C)**(2/3)**

Parameter	Symbols	Conditions	Ratings	Unit
LCD voltage	V _{L1}	V _{L1} voltage ^{Note 1}	-0.3 to +2.8 and -0.3 to V _{L4} + 0.3	V
	V _{L2}	V _{L2} voltage ^{Note 1}	-0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{L3}	V _{L3} voltage ^{Note 1}	-0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{L4}	V _{L4} voltage ^{Note 1}	-0.3 to +6.5	V
	V _{LCAP}	CAPL, CAPH voltage ^{Note 1}	-0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{LOUT}	COM0 to COM7, SEG0 to SEG38, output voltage	External resistance division method	-0.3 to V _{DD} + 0.3 ^{Note 2}
	Capacitor split method		-0.3 to V _{DD} + 0.3 ^{Note 2}	
	Internal voltage boosting method		-0.3 to V _{L4} + 0.3 ^{Note 2}	

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C)**(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	-70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	-100	mA
	I _{OH2}	Per pin	P20, P21	-0.5	mA
		Total of all pins		-1	mA
	Output current, low	I _{OL1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40
Total of all pins 170 mA			P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
I _{OL2}		Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature		T _A	In normal operation mode		-40 to +85
	In flash memory programming mode				
Storage temperature	T _{stg}			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f _X) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ V _{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V _{DD} ≤ 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.7 V	1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f _{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _H			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1		+1	%
			1.6 V ≤ V _{DD} < 1.8 V	-5		+5	%
		-40 to -20°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.5		+1.5	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _L				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **2.4 AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high ^{Note 1}	I _{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147			-10.0 Note 2	mA	
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-40.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			-8.0	mA
			1.8 V ≤ EV _{DD} < 2.7 V			-4.0	mA
			1.6 V ≤ EV _{DD} < 1.8 V			-2.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-60.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			-15.0	mA
			1.8 V ≤ EV _{DD} < 2.7 V			-8.0	mA
			1.6 V ≤ EV _{DD} < 1.8 V			-4.0	mA
		Total of all pins (When duty = 70% ^{Note 3})					-100.0
I _{OH2}	P20, P21	Per pin			-0.1	mA	
		Total of all pins	1.6 V ≤ V _{DD} ≤ 5.5 V			-0.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -40.0 mA

$$\text{Total output current of pins} = (-40.0 \times 0.7)/(80 \times 0.01) \cong -35.0 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, I _{OL} ^{Note 1}	I _{OL1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				20.0 Note 2	mA
		Per pin for P60, P61				15.0 ^{Note 2}	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			15.0	mA
			1.8 V ≤ EV _{DD} < 2.7 V			9.0	mA
			1.6 V ≤ EV _{DD} < 1.8 V			4.5	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			35.0	mA
			1.8 V ≤ EV _{DD} < 2.7 V			20.0	mA
			1.6 V ≤ EV _{DD} < 1.8 V			10.0	mA
	Total of all pins (When duty = 70% ^{Note 3})						150.0
I _{OL2}	P20, P21	Per pin				0.4	mA
		Total of all pins		1.6 V ≤ V _{DD} ≤ 5.5 V			0.8

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 70.0 mA

$$\text{Total output current of pins} = (70.0 \times 0.7) / (80 \times 0.01) \cong 61.25 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.