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RX630 Group
Renesas MCUs

R01DS0060EJ0160
Rev.1.60
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# 100-MHz 32-bit RX MCU, on-chip FPU, 165 DMIPS, up to 2-MB flash memory, USB 2.0 full-speed function interface, CAN, 10- & 12-bit A/D converter, RTC, up to 22 comms interfaces

## Features

### ■ 32-bit RX CPU core
- Max. operating frequency: 100 MHz
  Capable of 165 DMIPS in operation at 100 MHz
- Single precision 32-bit IEEE-754 floating point
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- Two types of debugging interfaces: JTAG and FINE (two-line)

### ■ Low-power design and architecture
- Operation from a single 2.7- to 3.6-V supply
- Low power consumption: A product that supports all peripheral functions draws only 500 µA/MHz.
- RTC is capable of operation from a dedicated power supply (min. operating voltage: 2.3 V).
- Four low-power modes

### ■ On-chip main flash memory, no wait states
- 100-MHz operation, 10-ns read cycle (no wait states)
- 384-Kbyte to 2-Mbyte capacities
- User code is programmable by on-board or off-board programming.

### ■ On-chip data flash memory
- Max. 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

### ■ On-chip SRAM, no wait states
- 32- to 128-Kbyte capacities
- For instructions and operands
- Can provide backup on deep software standby

### ■ DMA
- DMAC: Incorporates four channels
- DTC

### ■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

### ■ Clock functions
- External crystal oscillator or internal PLL for operation at 4 to 16 MHz
- Internal 125-kHz LOCO and 50-MHz HOCO
- 125-kHz clock for the IWDT
- Frequency of the oscillator for sub-clock generation: 32 kHz

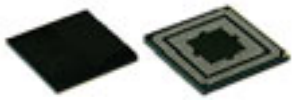
### ■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Time capture function
  (for capturing times in response to event-signal input on external pins)

### ■ Independent watchdog timer
- 125-kHz LOCO clock operation

### ■ Useful functions for IEC60730 compliance
- Oscillation-stop detection, frequency measurement, CRC, IWDT, self-diagnostic function for the A/D converter, etc.

PLQP0176KB-A 24 × 24 mm, 0.5-mm pitch
PLQP0144KA-A 20 × 20 mm, 0.5-mm pitch
PLQP0100KB-A 14 × 14 mm, 0.5-mm pitch
PLQP0080KB-A 12 × 12 mm, 0.5-mm pitch

PTLG0177JB-A 8 × 8 mm, 0.5-mm pitch
PTLG0145KA-A 7 × 7 mm, 0.5-mm pitch
PTLG0100KA-A 5.5 × 5.5 mm, 0.5-mm pitch



PLBG0176GA-A 13 × 13 mm, 0.8-mm pitch

### ■ Up to 22 communications interfaces
- USB 2.0 full-speed function interface (1 channel)
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (up to 3 channels)
- SCI with multiple functionalities (up to 13 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simple SPI, simple $I^2C$, and extended serial mode.
- $I^2C$ bus interface for transfer at up to 1 Mbps (up to 4 channels)
- RSPI for high-speed transfer (up to 3 channels)

### ■ External address space
- 8 CS areas (8 × 16 Mbytes)
- Multiplexed address data or separate address lines are selectable per area.
- 8-, 16-, or 32-bit bus space is selectable per area

### ■ Up to 20 extended-function timers
- 16-bit MTU2: input capture, output capture, complementary PWM output, phase-counting mode (6 channels)
- 16-bit TPU: input capture, output capture, phase-counting mode (12 channels)
- 8-bit TMR (4 channels)
- 16-bit compare-match timers (4 channels)

### ■ A/D converter for 1-MHz operation
- Up to 21 12-bit channels, and incorporating 1 sample-and-hold circuit
- Up to 8 10-bit channels, and incorporating 1 sample-and-hold circuit
- Addition of results of A/D conversion (in the 12-bit A/D converter)
- self-diagnosis (for the 10-bit A/D converter)

### ■ 10-bit D/A converter: 2 channels

### ■ Temperature sensor for measuring temperature within the chip

### ■ Register write protection function can protect values in important registers against overwriting.

### ■ Up to 148 general I/O port pins for GPIO
- 5-V tolerance, open drain, input pull-up, switchable driving ability

### ■ Unique ID
- 16-byte ID code is provided for each chip (only for the G version)

### ■ Operating temp. range
- D version: -40 to +85°C
- G version: -40 to +105°C

# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.
Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the ROM capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

**Table 1.1 Outline of Specifications (1/5)**

| Classification | Module/Function | Description |
|---|---|---|
| CPU | CPU | • Maximum operating frequency: 100 MHz<br>• 32-bit RX CPU<br>• Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>• Address space: 4-Gbyte linear<br>• Register set of the CPU<br>General purpose: Sixteen 32-bit registers<br>Control: Nine 32-bit registers<br>Accumulator: One 64-bit register<br>• Basic instructions: 73<br>• Floating-point operation instructions: 8<br>• DSP instructions: 9<br>• Addressing modes: 10<br>• Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>• On-chip 32-bit multiplier: 32 × 32 → 64 bits<br>• On-chip divider: 32 / 32 → 32 bits<br>• Barrel shifter: 32 bits<br>• Memory protection unit (MPU) |
| | FPU | • Single precision floating point (32 bits)<br>• Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | ROM | • Capacity: 384 Kbytes, 512 Kbytes, 768 Kbytes, 1 Mbyte, 1.5 Mbytes, 2 Mbytes<br>• 100 MHz, no-wait access<br>• On-board programming: Four types<br>• Off-board programming (parallel programmer mode) |
| | RAM | • Capacity: 64 Kbytes, 96 Kbytes, 128 Kbytes<br>• 100 MHz, no-wait access |
| | $E^2$ data flash | • Capacity: 32 Kbytes<br>• Programming/erasing: 100,000 times |
| MCU operating modes | | Single-chip mode, on-chip ROM enabled extended mode, and on-chip ROM disabled extended mode (software switching) |
| Clock | Clock generation circuit | • Main clock oscillator, sub-clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and dedicated on-chip oscillator for the IWDT<br>• Main-clock oscillation stop detection<br>• Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), FlashIF clock (FCLK) and external bus clock (BCLK)<br>The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz<br>Peripheral modules run in synchronization with the peripheral module clock (PCLK): Up to 50 MHz<br>Flash IF run in synchronization with the FlashIF clock (FCLK): Up to 50 MHz<br>Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz |
| Reset | | RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset |
| Voltage detection circuit | | When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated. |

**Table 1.1 Outline of Specifications (2/5)**

| Classification | Module/Function | Description |
|---|---|---|
| Low power consumption | Low power consumption facilities | • Module stop function<br>• Four low power consumption modes<br>Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode<br>• Battery backup function |
| Interrupt | Interrupt controller (ICUb) | • Peripheral function interrupts: 180 sources<br>• External interrupts: 16 (pins IRQ0 to IRQ15)<br>• Software interrupts: One source<br>• Non-maskable interrupts: 6 sources<br>• Sixteen levels specifiable for the order of priority |
| External bus extension | | • The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings.<br>Capacity of each area: 16 Mbytes (CS0 to CS7)<br>A chip-select signal (CS0# to CS7#) can be output for each area.<br>Each area is specifiable as an 8-, 16- or 32-bit bus space<br>The data arrangement in each area is selectable as little or big endian (only for data).<br>• Bus format: Separate bus, multiplex bus<br>• Wait control<br>• Write buffer facility |
| DMA | DMA controller (DMACA) | • 4 channels<br>• Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| | Data transfer controller (DTCa) | • Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: External interrupts and interrupt requests from peripheral functions |
| I/O ports | General I/O port pins | • 177-pin TFLGA (in planning), 176-pin LFBGA (in planning), 176-pin LQFP<br>I/O pins: 148<br>Input pin: 1<br>Pull-up resistors: 148<br>Open-drain outputs: 148<br>5-V tolerance: 54<br>• 145-pin TFLGA (in planning), 144-pin LQFP<br>I/O pins: 117<br>Input pin: 1<br>Pull-up resistors: 117<br>Open-drain outputs: 117<br>5-V tolerance: 53<br>• 100-pin TFLGA (in planning), 100-pin LQFP<br>I/O pins: 78<br>Input pin: 1<br>Pull-up resistors: 78<br>Open-drain outputs: 78<br>5-V tolerance: 44<br>• 80-pin LQFP (in planning)<br>I/O pins: 58<br>Input pin: 1<br>Pull-up resistors: 58<br>Open-drain outputs: 58<br>5-V tolerance: 34 |

**Table 1.1 Outline of Specifications (3/5)**

| Classification | Module/Function | Description |
|---|---|---|
| Timers | 16-bit timer pulse unit (TPUa) | • (16 bits × 6 channels) × 2 units<br>• Maximum of 16 pulse-input/output possible<br>• Select from among seven or eight counter-input clock signals for each channel<br>• Supports the input capture/output compare function<br>• Output of PWM waveforms in up to 15 phases in PWM mode<br>• Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel.<br>• PPG output trigger can be generated<br>• Capable of generating conversion start triggers for the A/D converters<br>• Signals from the input capture pins are input via a digital filter<br>• Clock frequency measuring method |
| | Multi-function timer pulse unit 2 (MTU2a) | • (16 bits × 6 channels) × 1 unit<br>• Time bases for the 6 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines<br>• Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available.<br>• Input capture function<br>• 21 output compare/input capture registers<br>• Complementary PWM output mode<br>• Reset synchronous PWM mode<br>• Phase-counting mode<br>• Generation of triggers for A/D converter conversion<br>• Digital filter<br>• Signals from the input capture pins are input via a digital filter<br>• PPG output trigger can be generated<br>• Clock frequency measuring function |
| | Frequency measurement function (MCK) | The MTU or unit 0 TPU module can be used to monitor the main clock, sub-clock, HOCO clock, LOCO clock, and PLL clock for abnormal frequencies. |
| | Port output enable 2 (POE2a) | Controls the high-impedance state of the MTU's waveform output pins |
| | Programmable pulse generator (PPG) | • (4 bits × 4 groups) × 2 units<br>• Pulse output with the MTU or TPU output as a trigger<br>• Maximum of 32 pulse-output possible |
| | 8-bit timers (TMR) | • (8 bits × 2 channels) × 2 units<br>• Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal<br>• Capable of output of pulse trains with desired duty cycles or of PWM signals<br>• The 2 channels of each unit can be cascaded to create a 16-bit timer<br>• Generation of triggers for A/D converter conversion<br>• Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 |
| | Compare match timer (CMT) | • (16 bits × 2 channels) × 2 units<br>• Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Realtime clock (RTCa) | • Clock sources: Main clock, sub-clock<br>• Clock and calendar functions<br>Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt<br>• Battery backup operation<br>• Time-capture facility for three values |
| | Watchdog timer (WDTA) | • 14 bits × 1 channel<br>• Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192) |
| | Independent watchdog timer (IWDTA) | • 14 bits × 1 channel<br>• Counter-input clock: Dedicated on-chip oscillator for the IWDT<br>• Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 |

**Table 1.1 Outline of Specifications (4/5)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication function | USB 2.0 function module (USBa) | • Includes a UDC (USB Device Controller) and transceiver for USB 2.0<br>• Single port<br>• Compliance with the USB 2.0 specification<br>• Transfer rate: Full speed (12 Mbps)<br>• Self-power mode and bus power are selectable<br>• Incorporates 2 Kbytes of RAM as a transfer buffer |
| | Serial communications interfaces (SCIc, SCId) | • 13 channels (SCIc: 12 channels + SCId: 1 channel)<br>• SCIc<br>Serial communications modes: Asynchronous, clock synchronous, and smart-card interface<br>Multi-processor function<br>On-chip baud rate generator allows selection of the desired bit rate<br>Choice of LSB-first or MSB-first transfer<br>Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12<br>Simple $I^2C$<br>Simple SPI<br>• SCId (The following functions are added to SCIc)<br>Supports the serial communications protocol, which contains the start frame and information frame<br>Supports the LIN format |
| | $I^2C$ bus interfaces (RIIC) | • 4 channels (one of them is FM+)<br>Communication formats<br>$I^2C$ bus format/SMBus format<br>Supports the multi-master<br>Max. transfer rate: 1 Mbps (channel 0) |
| | IEBus (IEB) | • 1 channel<br>• Supports protocol control for the IEBus<br>Half-duplex asynchronous transfer<br>Multi-master operation<br>Broadcast communications function<br>Two selectable modes, differentiated by transfer rate |
| | CAN module (CAN) | • 3 channels<br>• Compliance with the ISO11898-1 specification (standard frame and extended frame)<br>• 32 mailboxes per channel |
| | Serial peripheral interfaces (RSPI) | • 3 channels<br>• RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>• Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Buffered structure<br>Double buffers for both transmission and reception |
| 12-bit A/D converter (S12ADa) | | • 1 unit (1 unit × 21 channels)<br>• 12-bit resolution<br>• Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz)<br>• Operating mode<br>Scan mode (single scan mode or continuous scan mode)<br>• Sample-and-hold function<br>• Reference voltage generation<br>• Three ways to start A/D conversion<br>Conversion can be started by a software trigger, a trigger from a timer (MTU, TPU, or TMR), or an external trigger signal<br>• A/D conversion of the temperature sensor output |

**Table 1.1 Outline of Specifications (5/5)**

| Classification | Module/Function | Description |
|---|---|---|
| 10-bit A/D converter (ADb) | | • 1 unit (1 unit × 8 channels)<br>• 10-bit resolution<br>• Conversion time: 1.0 µs per channel (in operation with PCLK at 50 MHz)<br>• Operating mode<br>Scan mode (single scan mode or continuous scan mode)<br>External amplifier connection mode<br>• Sample-and-hold function<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal. |
| D/A converter (DAa) | | • 2 channels<br>• 10-bit resolution<br>• Output voltage: 0 V to VREFH |
| Temperature sensor | | • 1 channel<br>• Precision: ± 1 ºC<br>• The voltage of the temperature is converted into a digital value by the 12-bit A/D converter. |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$.<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable |
| Unique ID | | A 16-byte device-specific ID (only for the G version) |
| Operating frequency | | Up to 100 MHz |
| Power supply voltage | | VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, Vbatt = 2.3 to 3.6 V |
| Operating temperature | | D version: -40 to +85°C,<br>G version: -40 to +105°C*1 |
| Package | | 177-pin TFLGA (PTLG0177KA-A) (in planning)<br>176-pin LFBGA (PLBG0176GA-A) (in planning)<br>176-pin LQFP (PLQP0176KB-A)<br>145-pin TFLGA (PTLG0145KA-A) (in planning)<br>144-pin LQFP (PLQP0144KA-A)<br>100-pin TFLGA (PTLG0100KA-A) (in planning)<br>100-pin LQFP (PLQP0100KB-A)<br>80-pin LQFP (PLQP0080KB-A) (in planning) |
| On-chip debugging system | | • E1 emulator (JTAG and FINE interfaces)<br>• E20 emulator (JTAG interface) |

Note 1. Please contact us if you are using a G version.

**Table 1.2 Comparison of Functions for Different Packages**

| Functions | | RX630 Group | | | |
|---|---|---|---|---|---|
| **Package** | | **177 Pins, 176 Pins** | **145 Pins, 144 Pins** | **100 Pins** | **80 Pins** |
| External bus | External bus width | 32 bits | 16 bits | | Not supported |
| DMA | DMA controller | Ch. 0 to 3 | | | |
| | Data transfer controller | Supported | | | |
| Timers | 16-bit timer pulse unit | Ch. 0 to 11 | | Ch. 0 to 5 | |
| | Multi-function timer pulse unit 2 | Ch. 0 to 5 | | | |
| | Port output enable 2 | Supported | | | |
| | Programmable pulse generator | Ch. 0 and 1 | | | |
| | 8-bit timers | Ch. 0 to 3 | | | |
| | Compare match timer | Ch. 0 to 3 | | | |
| | Realtime clock | Supported | | | |
| | Watchdog timer | Supported | | | |
| | Independent watchdog timer | Supported | | | |
| Communication function | USB 2.0 function module | Ch. 0 | | | |
| | Serial communications interfaces (SCIc) | Ch. 0 to 11 | | Ch. 0 to 3, 5, 6, 8, 9 | Ch. 1, 5, 6, 8, 9 |
| | Serial communications interfaces (SCId) | Ch. 12 | | | |
| | $I^2C$ bus interfaces | Ch. 0 to 3 | | Ch. 0, 2 | |
| | IEBus | Supported | | | |
| | Serial peripheral interfaces | Ch. 0 to 2 | | Ch. 0, 1 | |
| | CAN module | For 1 M or less: Ch. 0, 1<br>For 1.5 M or more: Ch. 0 to 2 | | For 512 K or less: Ch. 1<br>For 768 K or more: Ch. 0, 1 | Ch. 1 |
| 12-bit A/D converter | | AN000 to 020 | | AN000 to 013 | AN000 to 010 |
| 10-bit A/D converter | | AN0 to 7 | | | AN0 to 3 |
| D/A converter | | Ch. 0, 1 | | Ch. 1 | |
| Temperature sensor | | Supported | | | |
| CRC calculator | | Supported | | | |
| Unique ID | | Available (only for the G version) | | | |

## 1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

**Table 1.3 List of Products (1/2)**

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|---|---|---|---|---|---|---|---|
| RX630 (D version) | R5F56307CDFN | PLQP0080KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56307DDFN | PLQP0080KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56307CDFP | PLQP0100KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56307DDFP | PLQP0100KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56307CDLA | PTLG0100KA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56307DDLA | PTLG0100KA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56308CDFN | PLQP0080KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56308DDFN | PLQP0080KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56308CDFP | PLQP0100KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56308DDFP | PLQP0100KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56308CDLA | PTLG0100KA-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56308DDLA | PTLG0100KA-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ACDFP*1 | PLQP0100KB-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ADDFP*1 | PLQP0100KB-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ACDFB*1 | PLQP0144KA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ADDFB*1 | PLQP0144KA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ACDLK*1 | PTLG0145KA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ADDLK*1 | PTLG0145KA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ACDFC | PLQP0176KB-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ADDFC | PLQP0176KB-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ACDBG | PLBG0176GA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ADDBG | PLBG0176GA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ACDLC | PTLG0177KA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ADDLC | PTLG0177KA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BCDFP*1 | PLQP0100KB-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BDDFP*1 | PLQP0100KB-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BCDFB*1 | PLQP0144KA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BDDFB*1 | PLQP0144KA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BCDLK*1 | PTLG0145KA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BDDLK*1 | PTLG0145KA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BCDFC | PLQP0176KB-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BDDFC | PLQP0176KB-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BCDBG | PLBG0176GA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BDDBG | PLBG0176GA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BCDLC | PTLG0177KA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630BDDLC | PTLG0177KA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DCDFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DDDFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DCDFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DDDFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DCDLK | PTLG0145KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |

**Table 1.3 List of Products (2/2)**

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|---|---|---|---|---|---|---|---|
| RX630 (D version) | R5F5630DDDLK | PTLG0145KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DCDFC | PLQP0176KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DDDFC | PLQP0176KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DCDBG | PLBG0176GA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DDDBG | PLBG0176GA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DCDLC | PTLG0177KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630DDDLC | PTLG0177KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ECDFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630EDDFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ECDFB | PLQP0144KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630EDDFB | PLQP0144KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ECDLK | PTLG0145KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630EDDLK | PTLG0145KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ECDFC | PLQP0176KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630EDDFC | PLQP0176KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ECDBG | PLBG0176GA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630EDDBG | PLBG0176GA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630ECDLC | PTLG0177KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5630EDDLC | PTLG0177KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| RX630 (G version) *2 | R5F5630BDGFB | PLQP0144KA-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100MHz | -40 to +105°C |
| | R5F5630ADGFB | PLQP0144KA-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100MHz | -40 to +105°C |
| | R5F5630BDGFP | PLQP0100KB-A | 1 Mbyte | 96 Kbytes | 32 Kbytes | 100MHz | -40 to +105°C |
| | R5F5630ADGFP | PLQP0100KB-A | 768 Kbytes | 96 Kbytes | 32 Kbytes | 100MHz | -40 to +105°C |
| | R5F56308DGFP | PLQP0100KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100MHz | -40 to +105°C |
| | R5F56307DGFP | PLQP0100KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100MHz | -40 to +105°C |
| | R5F56308DGFN | PLQP0080KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100MHz | -40 to +105°C |
| | R5F56307DGFN | PLQP0080KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100MHz | -40 to +105°C |

Note 1. The sub-clock oscillator, real-time clock, and boundary scan have different specifications. For details, see section 11.2.8, Sub-Clock Oscillator Wait Control Register (SOSCWTCR), section 28.2.19, RTC Control Register 3 (RCR3), and section 44.2.4, Boundary Scan Register (JTBSR) in the User's manual: Hardware.

Note 2. The specifications of the temperature sensor calibration and unique ID for G-version products differ from those for other products. For details, see section 41.2.2, Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL), section 41.3, Using the Temperature Sensor, and section 43.2.22, Unique ID Registers n (UIDRn) (n = 0 to 15) in the User's manual: Hardware.

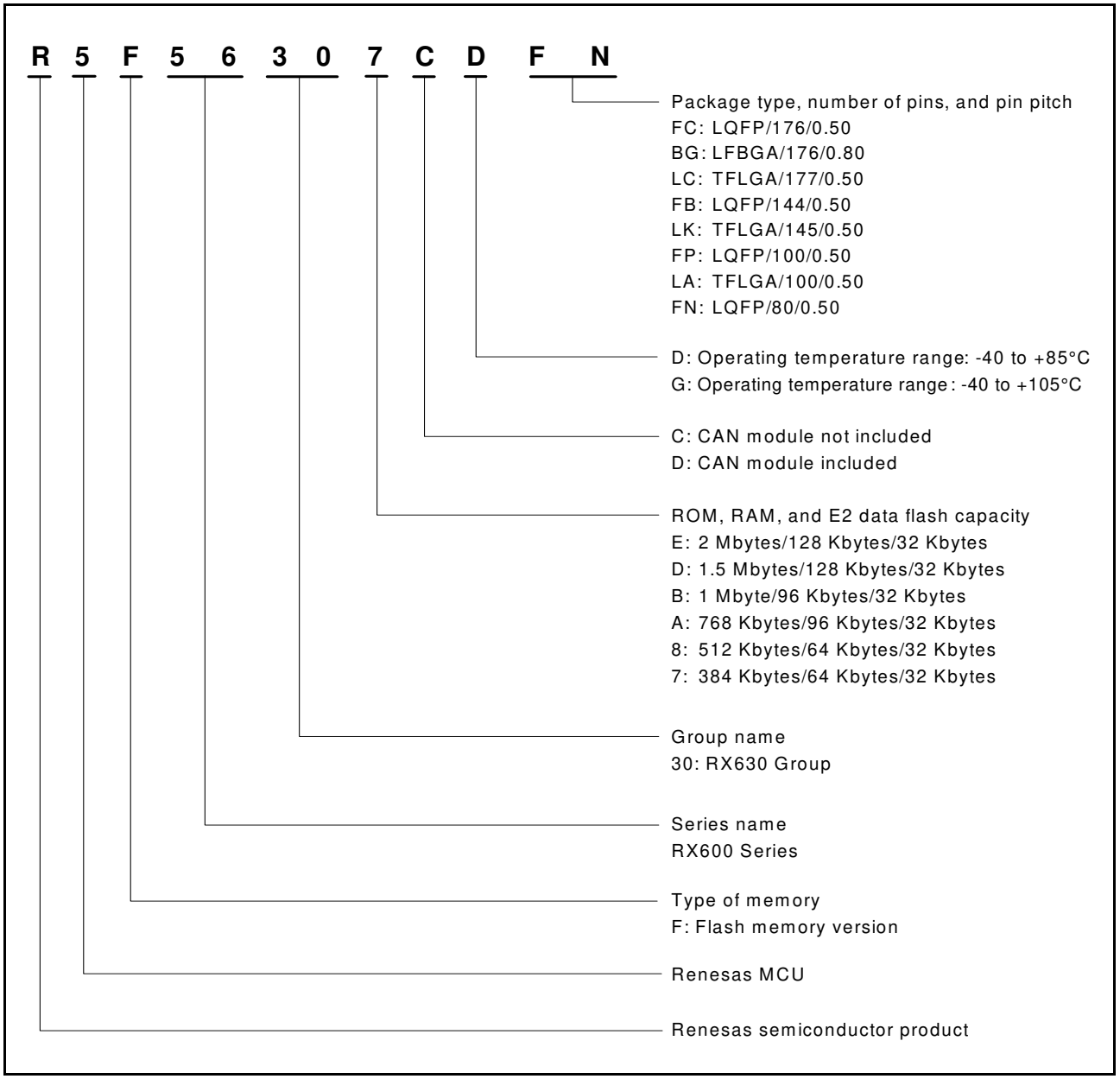
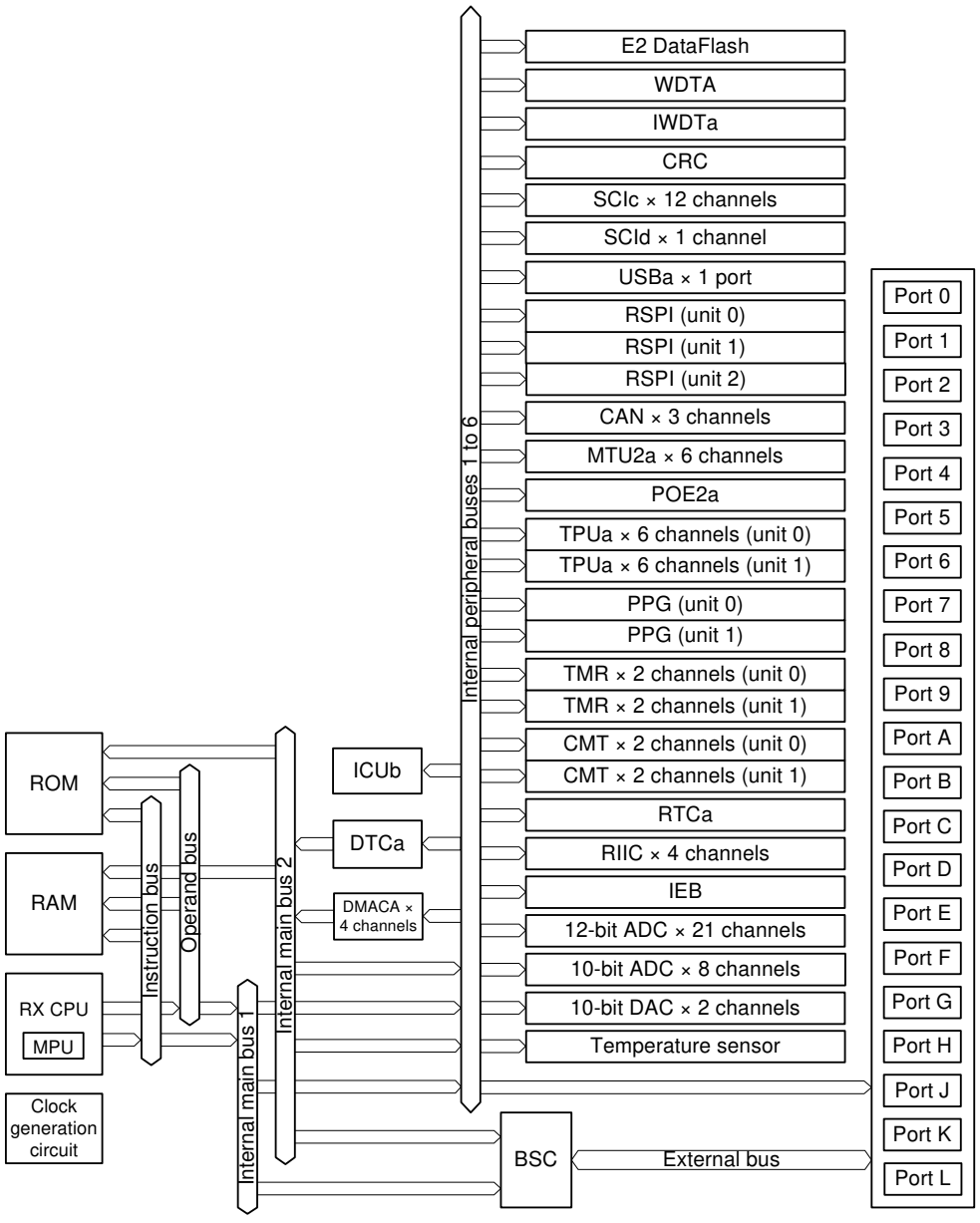



**Figure 1.1 How to Read the Product Part Number**

## 1.3 Block Diagram

Figure 1.2 shows a block diagram.




| | | | |
|---|---|---|---|
| ICUb: | Interrupt controller | CAN: | CAN module |
| DTCa: | Data transfer controller | MTU2a: | Multi-function timer pulse unit 2 |
| DMACA: | DMA controller | POE2a: | Port output enable 2 |
| BSC: | Bus controller | TPUa: | 16-bit timer pulse unit |
| WDTA: | Watchdog timer | PPG: | Programmable pulse generator |
| IWDTa: | Independent watchdog timer | TMR: | 8-bit timer |
| CRC: | CRC (cyclic redundancy check) calculator | CMT: | Compare match timer |
| SCIc, SCId: | Serial communications interface | RTCa: | Realtime clock |
| USBa: | USB 2.0 function module | RIIC: | $I^2C$ bus interface |
| RSPI: | Serial peripheral interface | IEB: | IEBus controller |
| MPU: | Memory protection unit | | |

**Figure 1.2 Block Diagram**

## 1.4 Pin Functions

Table 1.4 lists the pin functions.

**Table 1.4 Pin Functions (1/5)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin |
| | VCL | Input | Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V) |
| | VBATT | Input | Backup power pin. When the battery backup function is not to be used, connect it to the VCC pin. |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices |
| | XCOUT | Output | Input/output pins for the sub-clock oscillator circuit. Connect a crystal resonator between XCOUT and XCIN |
| | XCIN | Input | |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal levels on these pins must not be changed during operation |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low |
| | BSCANP | Input | Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low |
| On-chip emulator | FINEC | Input | Fine interface clock pin |
| | FINED | I/O | Fine interface pin |
| | TRST# | Input | On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data |
| | TRSYNC | Output | This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid |
| | TRDATA0 to TRDATA3 | Output | These pins output the trace information |
| Address bus | A0 to A23 | Output | Output pins for the address |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus |
| Multiplexed bus | A0/D0 to A15/D15 | I/O | Address/data multiplexed bus |

**Table 1.4 Pin Functions (2/5)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Bus control | RD# | Output | Strobe signal which indicates that reading from the external bus interface space is in progress |
| | WR# | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode |
| | WR0# to WR3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode |
| | BC0# to BC3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected |
| | WAIT# | Input | Input pin for wait request signals in access to the external space |
| | CS0# to CS7# | Output | Select signals for CS areas |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ15 | Input | Maskable interrupt request pin |
| Multi-function timer pulse unit 2 | MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins |
| | MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins |
| | MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins |
| | MTIC5U, MTIC5V MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins |
| | MTCLKA, MTCLKB MTCLKC, MTCLKD | Input | Input pins for external clock |
| Port output enable 2 | POE0# to POE3# POE8# | Input | Input pins for request signals to place the MTU large-current pins in the high impedance state |

**Table 1.4 Pin Functions (3/5)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| 16-bit timer pulse unit | TIOCA0, TIOCB0 TIOCC0, TIOCD0 | I/O | The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins |
| | TIOCA1, TIOCB1 | I/O | The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins |
| | TIOCA2, TIOCB2 | I/O | The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins |
| | TIOCA3, TIOCB3 TIOCC3, TIOCD3 | I/O | The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins |
| | TIOCA4, TIOCB4 | I/O | The TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins |
| | TIOCA5, TIOCB5 | I/O | The TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins |
| | TCLKA, TCLKB TCLKC, TCLKD | Input | Input pins for external clock signals |
| | TIOCA6, TIOCB6, TIOCC6, TIOCD6 | I/O | The TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins |
| | TIOCA7, TIOCB7 | I/O | The TGRA7 and TGRB7 input capture input/output compare output/ PWM output pins |
| | TIOCA8, TIOCB8 | I/O | The TGRA8 and TGRB8 input capture input/output compare output/ PWM output pins |
| | TIOCA9, TIOCB9, TIOCC9, TIOCD9 | I/O | The TGRA9 to TGRD9 input capture input/output compare output/ PWM output pins |
| | TIOCA10, TIOCB10 | I/O | The TGRA10 and TGRB10 input capture input/output compare output/PWM output pins |
| | TIOCA11, TIOCB11 | I/O | The TGRA11 and TGRB11 input capture input/output compare output/PWM output pins |
| | TCLKE, TCLKF, TCLKG, TCLKH | Input | Input pins for external clock signals |
| Programmable pulse generator | PO0 to PO31 | Output | Output pins for the pulse signals |
| 8-bit timer | TMO0 to TMO3 | Output | Compare match output pins |
| | TMCI0 to TMCI3 | Input | Input pins for external clocks to be input to the counter |
| | TMRI0 to TMRI3 | Input | Input pins for the counter reset |
| Serial communications interface (SCIc) | • Asynchronous mode/clock synchronous mode | | |
| | SCK0 to SCK11 | I/O | Input/output pins for the clock |
| | RXD0 to RXD11 | Input | Input pins for received data |
| | TXD0 to TXD11 | Output | Output pins for transmitted data |
| | CTS0# to CTS11# | Input | Input pins for controlling the start of transmission and reception |
| | RTS0# to RTS11# | Output | Output pins for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL0 to SSCL11 | I/O | Input/output pins for the $I^2C$ clock |
| | SSDA0 to SSDA11 | I/O | Input/output pins for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK0 to SCK11 | I/O | Input/output pins for the clock |
| | SMISO0 to SMISO11 | I/O | Input/output pins for slave transmission of data |
| | SMOSI0 to SMOSI11 | I/O | Input/output pins for master transmission of data |
| | SS0# to SS11# | Input | Chip-select input pins |

**Table 1.4 Pin Functions (4/5)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Serial communications interface (SCId) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | RXD12 | Input | Input pin for received data |
| | TXD12 | Output | Output pin for transmitted data |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL12 | I/O | Input/output pin for the $I^2C$ clock |
| | SSDA12 | I/O | Input/output pin for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | SMISO12 | I/O | Input/output pin for slave transmission of data |
| | SMOSI12 | I/O | Input/output pin for master transmission of data |
| | SS12# | Input | Chip-select input pin |
| | • Extended serial mode | | |
| | RXDX12 | Input | Input pin for received data |
| | TXDX12 | Output | Output pin for transmitted data |
| | SIOX12 | I/O | Input/output pin for received or transmitted data |
| $I^2C$ bus interface | SCL0[FM+], SCL1 to SCL3 | I/O | Input/output pins for clocks. Bus can be directly driven by the N-channel open drain |
| | SDA0[FM+], SDA1 to SDA3 | I/O | Input/output pins for data. Bus can be directly driven by the N-channel open drain |
| USB power pins | VCC_USB | Input | Power supply pin. When the USB is not to be used, connect it to the VCC pin. |
| | VSS_USB | Input | Ground pin. When the USB is not to be used, connect it to the VSS pin. |
| USB 2.0 function module | USB0_DP | I/O | Inputs or outputs D+ data for the USB bus |
| | USB0_DM | I/O | Inputs or outputs D- data for the USB bus |
| | USB0_DPUPE | Output | Pull-up pin |
| | USB0_VBUS | Input | Input pin for detection of connection and disconnection of the USB cable |
| CAN module | CRX0 to CRX2 | Input | Input pins |
| | CTX0 to CTX2 | Output | Output pins |
| Serial peripheral interface | RSPCKA, RSPCKB RSPCKC | I/O | Clock input/output pins |
| | MOSIA, MOSIB, MOSIC | I/O | Inputs or outputs data output from the master |
| | MISOA, MISOB, MISOC | I/O | Inputs or outputs data output from the slave |
| | SSLA0, SSLB0, SSLC0 | I/O | Input or output pins for slave selection |
| | SSLA1 to SSLA3 SSLB1 to SSLB3 SSLC1 to SSLC3 | Output | Output pins for slave selection |
| IEBus controller | IERXD | Input | Input pin for data reception |
| | IETXD | Output | Output pin for data transmission |
| Realtime clock | RTCOUT | Output | Output pin for 1-Hz clock |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pin |

**Table 1.4 Pin Functions (5/5)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| 12-bit A/D converter | AN000 to AN020 | Input | Input pins for the analog signals to be processed by the A/D converter |
| | ADTRG0# | Input | Input pins for the external trigger signals that start the A/D conversion |
| 10-bit A/D converter | AN0 to AN7 | Input | Input pins for the analog signals to be processed by the A/D converter |
| | ANEX0 | Output | Extended analog output pin |
| | ANEX1 | Input | Extended analog input pin |
| | ADTRG# | Input | Input pins for the external trigger signals that start the A/D conversion |
| D/A converter | DA0, DA1 | Output | Output pins for the analog signals to be processed by the D/A converter |
| Analog power supply | AVCC0 | Input | Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used |
| | AVSS0 | Input | Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used |
| | VREFH0 | Input | Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used |
| | VREFL0 | Input | Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used |
| | VREFH | Input | Reference voltage input pin for the 10-bit A/D converter and D/A converter. This is used as the analog power supply for the respective modules. Connect this pin to VCC if neither the 10-bit A/D converter nor the D/A converter is in use |
| | VREFL | Input | Reference ground pin for the 10-bit A/D converter and D/A converter. This is used as the analog ground for the respective modules. Set this pin to the same potential as the VSS pin |
| I/O ports | P00 to P03, P05, P07 | I/O | 6-bit input/output pins |
| | P10 to P17 | I/O | 8-bit input/output pins |
| | P20 to P27 | I/O | 8-bit input/output pins |
| | P30 to P37 | I/O | 8-bit input/output pins (P35: input pin) |
| | P40 to P47 | I/O | 8-bit input/output pins |
| | P50 to P57 | I/O | 8-bit input/output pins |
| | P60 to P67 | I/O | 8-bit input/output pins |
| | P70 to P77 | I/O | 8-bit input/output pins |
| | P80 to P87 | I/O | 8-bit input/output pins |
| | P90 to P97 | I/O | 8-bit input/output pins |
| | PA0 to PA7 | I/O | 8-bit input/output pins |
| | PB0 to PB7 | I/O | 8-bit input/output pins |
| | PC0 to PC7 | I/O | 8-bit input/output pins |
| | PD0 to PD7 | I/O | 8-bit input/output pins |
| | PE0 to PE7 | I/O | 8-bit input/output pins |
| | PF0 to PF5 | I/O | 6-bit input/output pins |
| | PG0 to PG7 | I/O | 8-bit input/output pins |
| | PH4, PH5 | I/O | 2-bit input/output pins |
| | PJ3, PJ5 | I/O | 2-bit input/output pins |
| | PK0 to PK7 | I/O | 8-bit input/output pins |
| | PL0 to PL4 | I/O | 5-bit input/output pins |

## 1.5 Pin Assignments

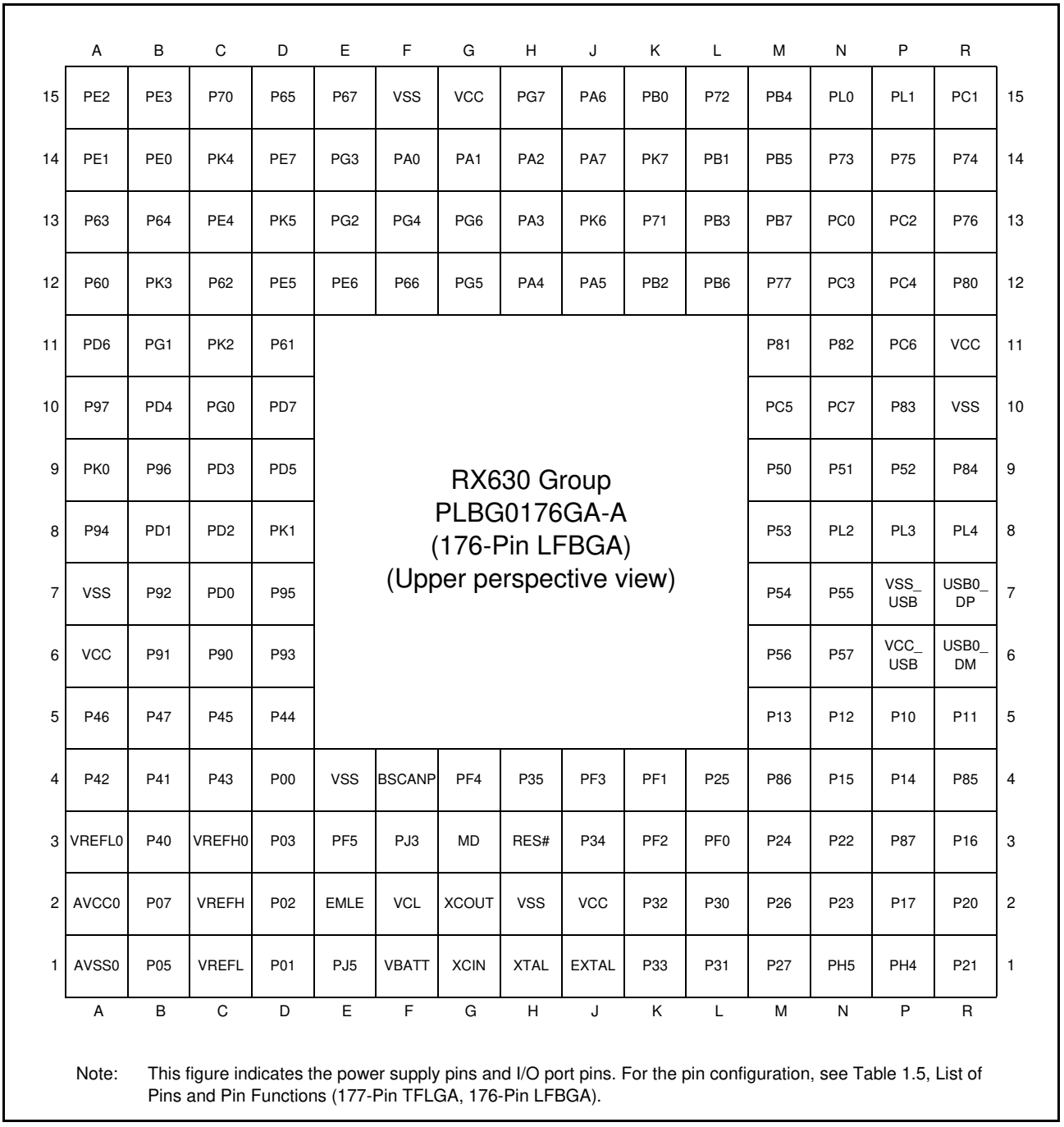
Figure 1.3 to Figure 1.10 show the pin assignments. Table 1.5 to Table 1.11 show the lists of pins and pin functions.

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | PE2 | PE3 | P70 | P65 | P67 | VSS | VCC | PG7 | PA6 | PB0 | P72 | PB4 | PL0 | PL1 | PC1 | 15 |
| 14 | PE1 | PE0 | PK4 | PE7 | PG3 | PA0 | PA1 | PA2 | PA7 | PK7 | PB1 | PB5 | P73 | P75 | P74 | 14 |
| 13 | P63 | P64 | PE4 | PK5 | PG2 | PG4 | PG6 | PA3 | PK6 | P71 | PB3 | PB7 | PC0 | PC2 | P76 | 13 |
| 12 | P60 | PK3 | P62 | PE5 | PE6 | P66 | PG5 | PA4 | PA5 | PB2 | PB6 | P77 | PC3 | PC4 | P80 | 12 |
| 11 | PD6 | PG1 | PK2 | P61 | | | | | | | | P81 | P82 | PC6 | VCC | 11 |
| 10 | P97 | PD4 | PG0 | PD7 | | | | | | | | PC5 | PC7 | P83 | VSS | 10 |
| 9 | PK0 | P96 | PD3 | PD5 | | | | | | | | P50 | P51 | P52 | P84 | 9 |
| 8 | P94 | PD1 | PD2 | PK1 | | | | | | | | P53 | PL2 | PL3 | PL4 | 8 |
| 7 | VSS | P92 | PD0 | P95 | | | | | | | | P54 | P55 | VSS_ USB | USB0_ DP | 7 |
| 6 | VCC | P91 | P90 | P93 | | | | | | | | P56 | P57 | VCC_ USB | USB0_ DM | 6 |
| 5 | P46 | P47 | P45 | P44 | NC | | | | | | | P13 | P12 | P10 | P11 | 5 |
| 4 | P42 | P41 | P43 | P00 | VSS | BSCANP | PF4 | P35 | PF3 | PF1 | P25 | P86 | P15 | P14 | P85 | 4 |
| 3 | VREFL0 | P40 | VREFH0 | P03 | PF5 | PJ3 | MD | RES# | P34 | PF2 | PF0 | P24 | P22 | P87 | P16 | 3 |
| 2 | AVCC0 | P07 | VREFH | P02 | EMLE | VCL | XCOUT | VSS | VCC | P32 | P30 | P26 | P23 | P17 | P20 | 2 |
| 1 | AVSS0 | P05 | VREFL | P01 | PJ5 | VBATT | XCIN | XTAL | EXTAL | P33 | P31 | P27 | PH5 | PH4 | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

RX630 Group
PTLG0177KA-A
(177-Pin TFLGA)
(Upper perspective view)

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

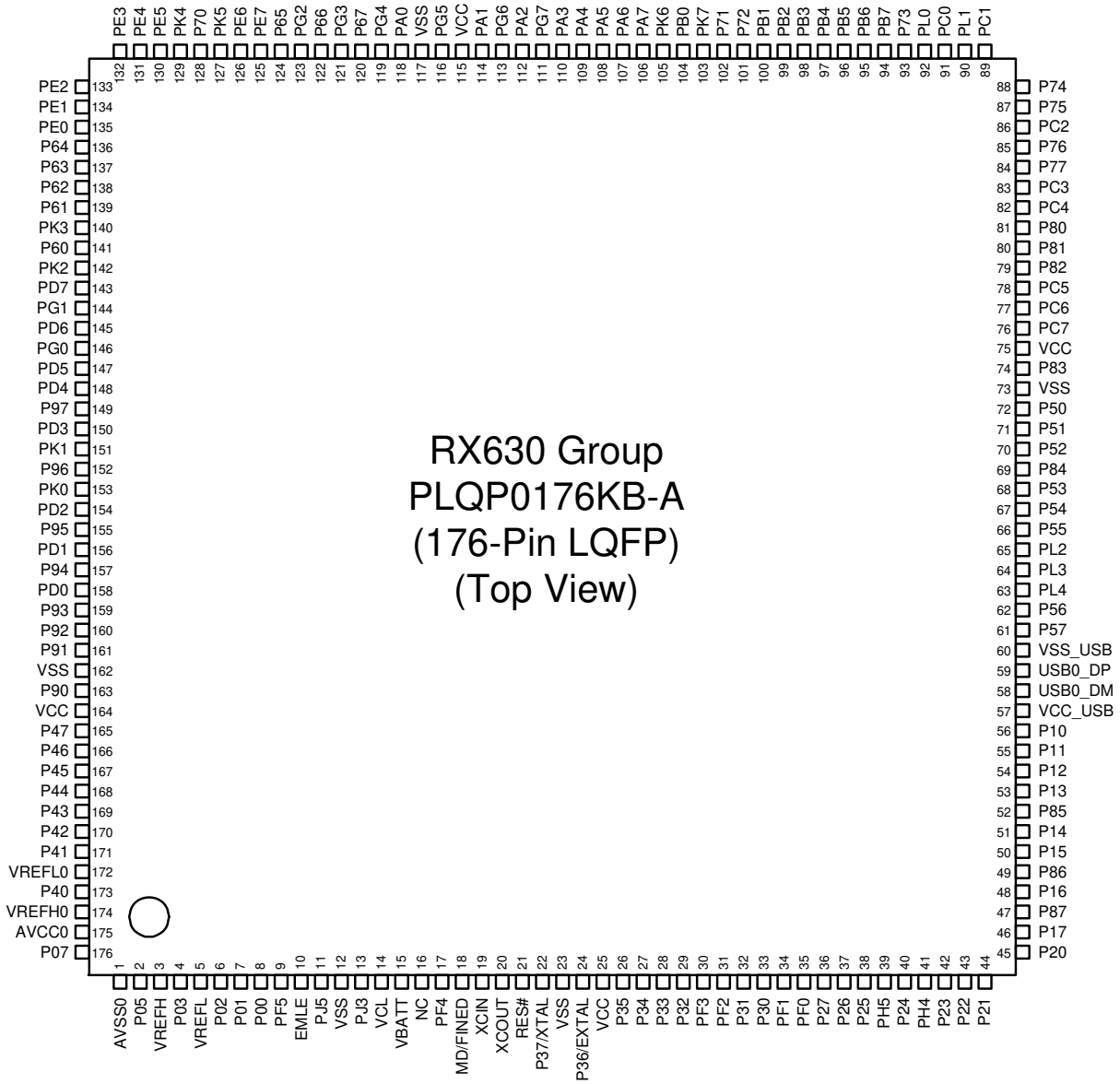
**Figure 1.3 Pin Assignment (177-Pin TFLGA)**




| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | PE2 | PE3 | P70 | P65 | P67 | VSS | VCC | PG7 | PA6 | PB0 | P72 | PB4 | PL0 | PL1 | PC1 | 15 |
| 14 | PE1 | PE0 | PK4 | PE7 | PG3 | PA0 | PA1 | PA2 | PA7 | PK7 | PB1 | PB5 | P73 | P75 | P74 | 14 |
| 13 | P63 | P64 | PE4 | PK5 | PG2 | PG4 | PG6 | PA3 | PK6 | P71 | PB3 | PB7 | PC0 | PC2 | P76 | 13 |
| 12 | P60 | PK3 | P62 | PE5 | PE6 | P66 | PG5 | PA4 | PA5 | PB2 | PB6 | P77 | PC3 | PC4 | P80 | 12 |
| 11 | PD6 | PG1 | PK2 | P61 | | | | | | | | P81 | P82 | PC6 | VCC | 11 |
| 10 | P97 | PD4 | PG0 | PD7 | | | | | | | | PC5 | PC7 | P83 | VSS | 10 |
| 9 | PK0 | P96 | PD3 | PD5 | | | | | | | | P50 | P51 | P52 | P84 | 9 |
| 8 | P94 | PD1 | PD2 | PK1 | | | | | | | | P53 | PL2 | PL3 | PL4 | 8 |
| 7 | VSS | P92 | PD0 | P95 | | | | | | | | P54 | P55 | VSS_ USB | USB0_ DP | 7 |
| 6 | VCC | P91 | P90 | P93 | | | | | | | | P56 | P57 | VCC_ USB | USB0_ DM | 6 |
| 5 | P46 | P47 | P45 | P44 | | | | | | | | P13 | P12 | P10 | P11 | 5 |
| 4 | P42 | P41 | P43 | P00 | VSS | BSCANP | PF4 | P35 | PF3 | PF1 | P25 | P86 | P15 | P14 | P85 | 4 |
| 3 | VREFL0 | P40 | VREFH0 | P03 | PF5 | PJ3 | MD | RES# | P34 | PF2 | PF0 | P24 | P22 | P87 | P16 | 3 |
| 2 | AVCC0 | P07 | VREFH | P02 | EMLE | VCL | XCOUT | VSS | VCC | P32 | P30 | P26 | P23 | P17 | P20 | 2 |
| 1 | AVSS0 | P05 | VREFL | P01 | PJ5 | VBATT | XCIN | XTAL | EXTAL | P33 | P31 | P27 | PH5 | PH4 | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

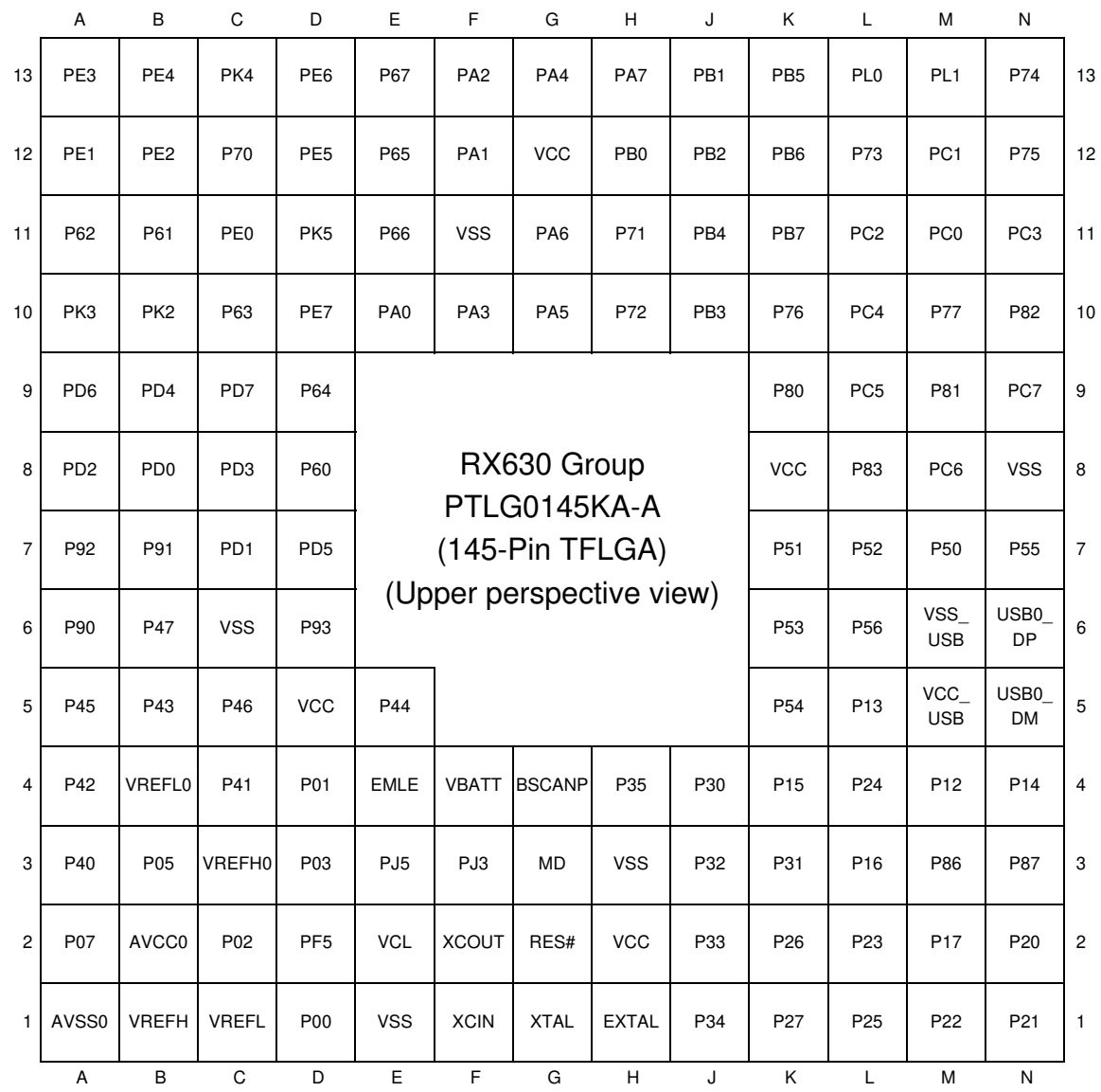
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

**Figure 1.4 Pin Assignment (176-Pin LFBGA)**



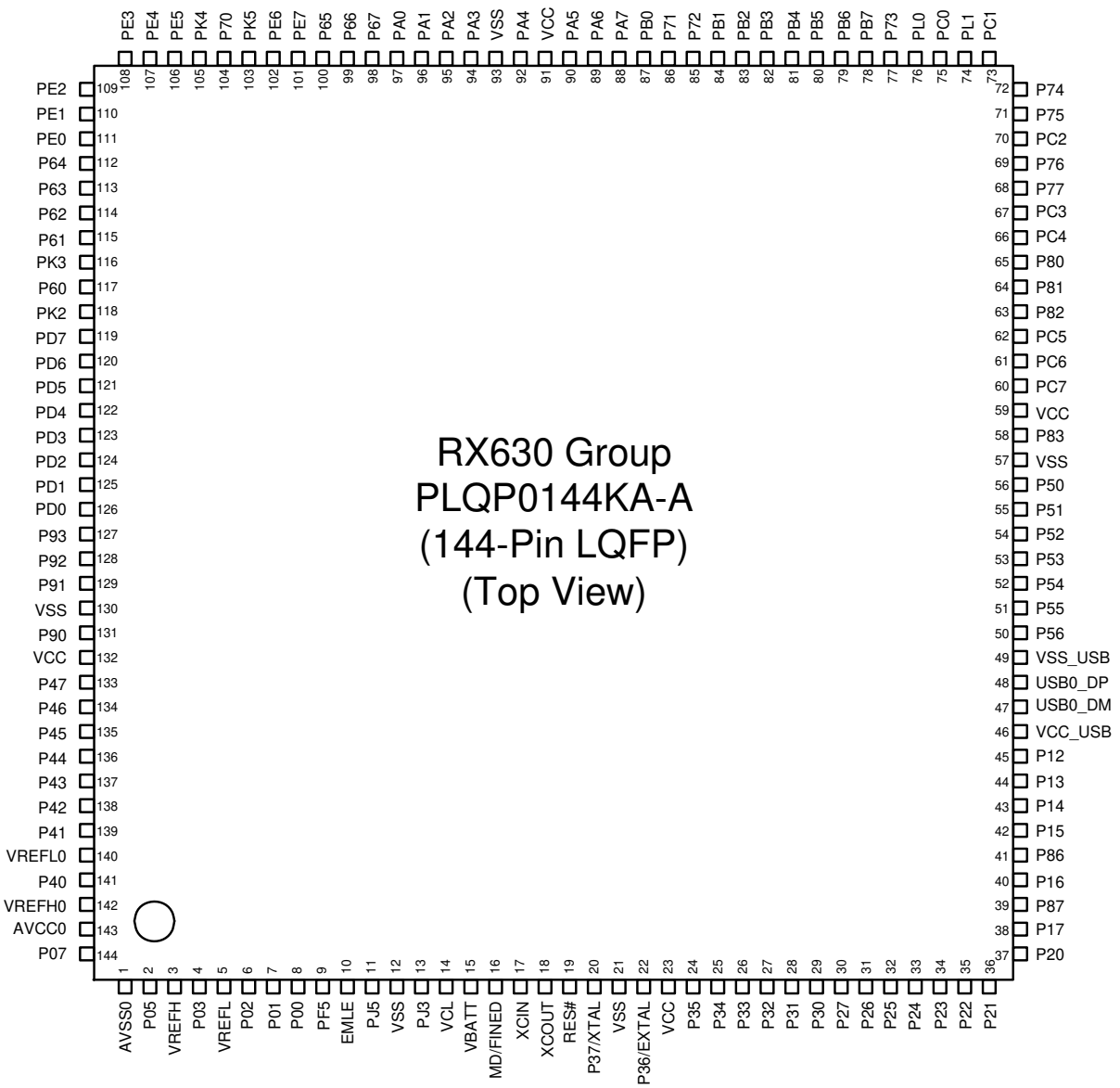

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (176-Pin LQFP).

**Figure 1.5 Pin Assignment (176-Pin LQFP)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

**Figure 1.6 Pin Assignment (145-Pin TFLGA)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pins and Pin Functions (144-Pin LQFP).

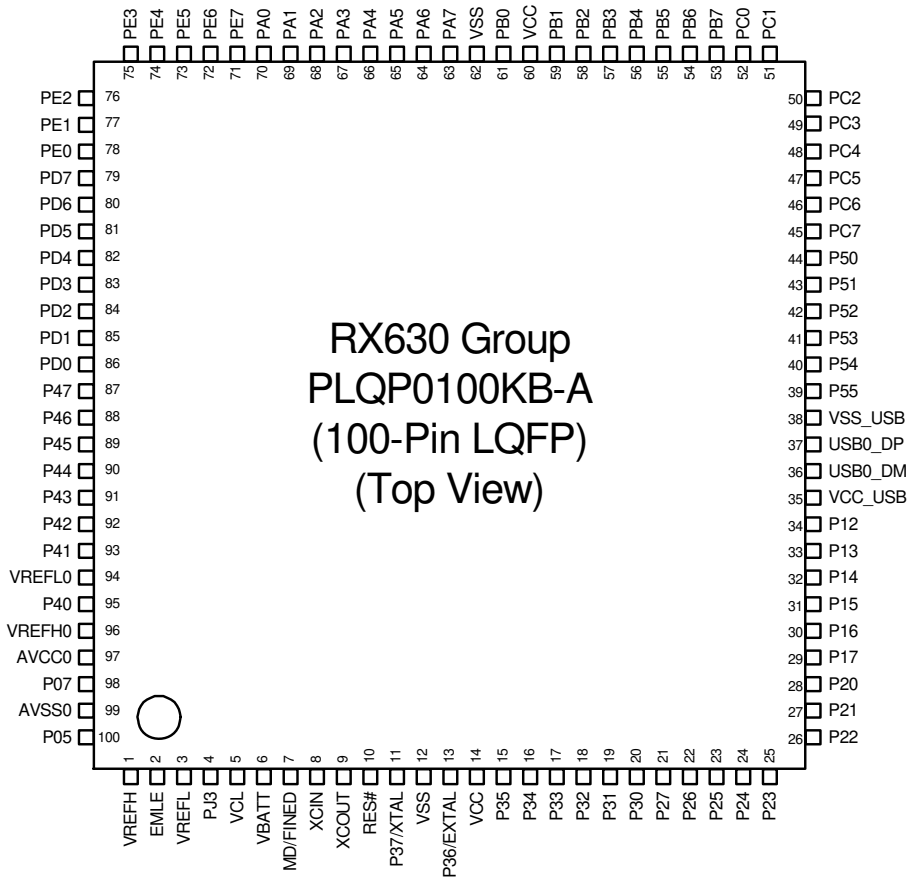
**Figure 1.7 Pin Assignment (144-Pin LQFP)**

RX630 Group
PTLG0100KA-A (100-Pin TFLGA)
(Top View)

| | A | B | C | D | E | F | G | H | J | K | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | PE2 | PE3 | PE4 | PA0 | PA3 | VSS | VCC | PB7 | PC1 | PC2 | 10 |
| 9 | PE1 | PD7 | PE5 | PA1 | PA5 | PA7 | PB1 | PB6 | PC0 | PC3 | 9 |
| 8 | PE0 | PD6 | PD5 | PE7 | PA4 | PB0 | PB4 | PC6 | PC4 | PC5 | 8 |
| 7 | PD4 | PD3 | PD2 | PE6 | PA6 | PB2 | PB5 | PC7 | P50 | P51 | 7 |
| 6 | PD0 | PD1 | P47 | P46 | PA2 | PB3 | P52 | P54 | VCC_ USB | USB0_ DP | 6 |
| 5 | P43 | P44 | P42 | P45 | P41 | P12 | P53 | P55 | VSS_ USB | USB0_ DM | 5 |
| 4 | VREFL0 | P40 | VREFH0 | VBATT | P34 | P32 | P27 | P15 | P13 | P14 | 4 |
| 3 | P07 | AVCC0 | PJ3 | MD | RES# | P35 | P30 | P16 | P17 | P20 | 3 |
| 2 | VREFH | AVSS0 | VREFL | XCOUT | VSS | VCC | P31 | P25 | P21 | P22 | 2 |
| 1 | P05 | EMLE | VCL | XCIN | XTAL | EXTAL | P33 | P26 | P24 | P23 | 1 |
| | A | B | C | D | E | F | G | H | J | K | |

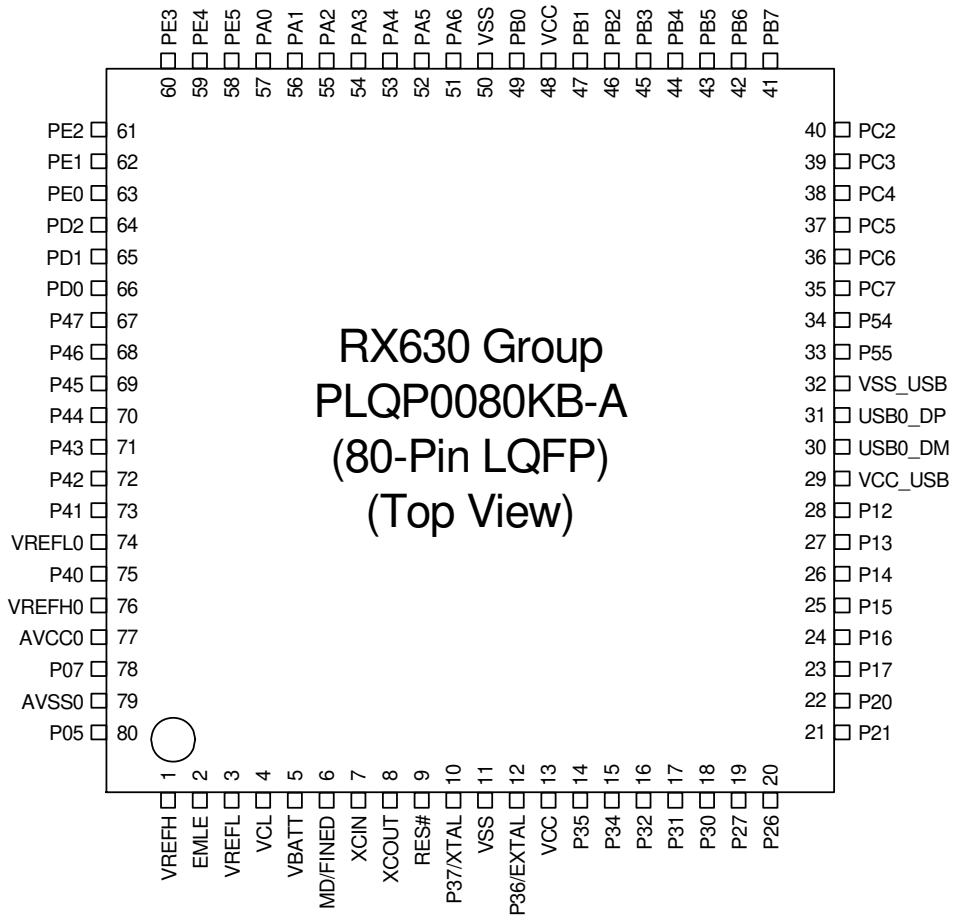
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

**Figure 1.8 Pin Assignment (100-Pin TFLGA)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (100-Pin LQFP).

**Figure 1.9 Pin Assignment (100-Pin LQFP)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.11, List of Pins and Pin Functions (80-Pin LQFP).

**Figure 1.10 Pin Assignment (80-Pin LQFP)**

**Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/5)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD, AD, DA |
|---|---|---|---|---|---|---|---|
| A1 | AVSS0 | | | | | | |
| A2 | AVCC0 | | | | | | |
| A3 | VREFL0 | | | | | | |
| A4 | | P42 | | | | IRQ10-DS | AN002 |
| A5 | | P46 | | | | IRQ14-DS | AN006 |
| A6 | VCC | | | | | | |
| A7 | VSS | | | | | | |
| A8 | | P94 | A20/D20 | | | | |
| A9 | | PK0 | | | | | |
| A10 | | P97 | A23/D23 | | | | |
| A11 | | PD6 | D6[A6/D6] | MTIC5V/POE1# | SSLC2 | IRQ6 | AN6 |
| A12 | | P60 | CS0# | | SCK9 | | |
| A13 | | P63 | CS3# | | | | |
| A14 | | PE1 | D9[A9/D9] | MTIOC4C/TIOCD9/PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB | | ANEX1 |
| A15 | | PE2 | D10[A10/D10] | MTIOC4A/TIOCA9/PO23 | RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB | IRQ7-DS | AN0 |
| B1 | | P05 | | | | IRQ13 | DA1 |
| B2 | | P07 | | | | IRQ15 | ADTRG0# |
| B3 | | P40 | | | | IRQ8-DS | AN000 |
| B4 | | P41 | | | | IRQ9-DS | AN001 |
| B5 | | P47 | | | | IRQ15-DS | AN007 |
| B6 | | P91 | A17/D17 | | SCK7 | | AN015 |
| B7 | | P92 | A18/D18 | | RXD7/SMISO7/SSCL7 | | AN016 |
| B8 | | PD1 | D1[A1/D1] | MTIOC4B/TIOCB7/ TCLKG | MOSIC/CTX0 | IRQ1 | AN009 |
| B9 | | P96 | A22/D22 | | | | |
| B10 | | PD4 | D4[A4/D4] | POE3# | SSLC0 | IRQ4 | AN012 |
| B11 | | PG1 | D25 | | | | |
| B12 | | PK3 | | | RXD9/SMISO9/SSCL9 | | |
| B13 | | P64 | CS4# | | | | |
| B14 | | PE0 | D8[A8/D8] | TIOCC9 | SCK12/SSLB1 | | ANEX0 |
| B15 | | PE3 | D11[A11/D11] | MTIOC4B/TIOCB9/PO26/ POE8# | CTS12#/RTS12#/SS12#/ MISOB | | AN1 |
| C1 | VREFL | | | | | | |
| C2 | VREFH | | | | | | |
| C3 | VREFH0 | | | | | | |
| C4 | | P43 | | | | IRQ11-DS | AN003 |
| C5 | | P45 | | | | IRQ13-DS | AN005 |
| C6 | | P90 | A16/D16 | | TXD7/SMOSI7/SSDA7 | | AN014 |
| C7 | | PD0 | D0[A0/D0] | TIOCA7 | | IRQ0 | AN008 |
| C8 | | PD2 | D2[A2/D2] | MTIOC4D/TIOCA8 | MISOC/CRX0 | IRQ2 | AN010 |
| C9 | | PD3 | D3[A3/D3] | TIOCB8/TCLKH/POE8# | RSPCKC | IRQ3 | AN011 |
| C10 | | PG0 | D24 | | | | |
| C11 | | PK2 | | | TXD9/SMOSI9/SSDA9 | | |
| C12 | | P62 | CS2# | | | | |