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1. Overview

1.1 Features

The M16C Family offers a robust platform of 32-/16-bit CISC microcomputers (MCUs) featuring high ROM code efficiency, extensive EMI/EMS noise immunity, ultra-low power consumption, high-speed processing in actual applications, and numerous and varied integrated peripherals. Extensive device scalability from low- to high-end, featuring a single architecture as well as compatible pin assignments and peripheral functions, provides support for a vast range of application fields.

The R32C/100 Series is a high-end microcontroller series in the M16C Family. With a 4-Gbyte memory space, it achieves maximum code efficiency and high-speed processing with 32-bit CISC architecture, multiplier, multiply-accumulate unit, and floating point unit. The selection from the broadest choice of on-chip peripheral devices — UART, CRC, DMAC, A/D and D/A converters, timers, I²C-bus interface, and watchdog timer enables to minimize external components.

The R32C/111 Group is the standard MCU within the R32C/100 Series. This product, provided as 100-pin plastic molded LGA, and 100-/64-pin plastic molded LQFP packages, has a maximum of nine channels of serial interface.

1.1.1 Applications

Audio, cameras, television, home appliance, printer, meter, office/industrial equipment, communication/portable devices

1.1.2 Performance Overview

Tables 1.1 to 1.4 show the performance overview of the R32C/111 Group.

Table 1.1 Performance Overview for the 100-pin Package (1/2)

Unit	Function	Explanation
CPU	Central processing unit	R32C/100 Series CPU Core <ul style="list-style-type: none"> • Basic instructions: 108 • Minimum instruction execution time: 20 ns ($f(\text{CPU}) = 50 \text{ MHz}$) • Multiplier: 32-bit \times 32-bit \rightarrow 64-bit • Multiply-accumulate unit: 32-bit \times 32-bit + 64-bit \rightarrow 64-bit • IEEE-754 compatible FPU: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional ⁽¹⁾)
Memory		Flash memory: 256 to 512 Kbytes RAM: 32 to 63 Kbytes Data flash: 4 Kbytes \times 2 blocks Refer to Table 1.5 for memory size of each product group
Voltage Detector	Low voltage detector	Optional ⁽¹⁾ Low voltage detection interrupt
Clock	Clock generator	<ul style="list-style-type: none"> • 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
External Bus Expansion	Bus and memory expansion	<ul style="list-style-type: none"> • Address space: 4 Gbytes (of which up to 64 Mbytes is user accessible) • External bus Interface: Support for wait-state insertion, 4 chip select outputs, 3V/5V interface • Bus format: Separate bus/Multiplexed bus selectable, data bus width selectable (8/16 bits)
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}} \times 6$, key input $\times 4$ Interrupt priority levels: 7
Watchdog Timer		15 bits \times 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels <ul style="list-style-type: none"> • Cycle-steal transfer mode • Request sources: 51 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	<ul style="list-style-type: none"> • Triggered by an interrupt request of any peripheral • 3 characteristic transfer functions: Immediate data transfer, calculation result transfer, chain transfer
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> • 2 input-only ports • 82 CMOS I/O ports • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:

1. Contact a Renesas Electronics sales office to use the optional features.

Table 1.2 Performance Overview for the 100-pin Package (2/2)

Unit	Function	Explanation
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART8	Asynchronous/synchronous serial interface × 9 channels <ul style="list-style-type: none"> • I²C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (optional ⁽¹⁾) (UART0 to UART6)
A/D Converter		10-bit resolution × 26 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 19 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional ⁽¹⁾)
Flash Memory		Programming and erasure supply voltage: VCC1 = VCC2 = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		50 MHz/VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Operating Temperature		-20°C to 85°C (N version) -40°C to 85°C (D version)
Current Consumption		32 mA (VCC1 = VCC2 = 5.0 V, f(CPU) = 50 MHz) 8 μA (VCC1 = VCC2 = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		100-pin plastic molded LQFP (PLQP0100KB-A) 100-pin plastic molded TFLGA (PTLG0100KA-A)

Note:

1. Contact a Renesas Electronics sales office to use the optional features.

Table 1.3 Performance Overview for the 64-pin Package (1/2)

Unit	Function	Explanation
CPU	Central processing unit	R32C/100 Series CPU Core <ul style="list-style-type: none"> • Basic instructions: 108 • Minimum instruction execution time: 20 ns ($f(\text{CPU}) = 50 \text{ MHz}$) • Multiplier: 32-bit \times 32-bit \rightarrow 64-bit • Multiply-accumulate unit: 32-bit \times 32-bit + 64-bit \rightarrow 64-bit • IEEE-754 compatible FPU: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode
Memory		Flash memory: 128/256 Kbytes RAM: 32 Kbytes Data flash: 4 Kbytes \times 2 blocks Refer to Table 1.5 for memory size of each product group
Voltage Detector	Low voltage detector	Optional ⁽¹⁾ Low voltage detection interrupt
Clock	Clock generator	<ul style="list-style-type: none"> • 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}} \times 6$, key input $\times 4$ Interrupt priority levels: 7
Watchdog Timer		15 bits \times 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels <ul style="list-style-type: none"> • Cycle-steal transfer mode • Request sources: 45 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	<ul style="list-style-type: none"> • Triggered by an interrupt request of any peripheral • 3 characteristic transfer functions: Immediate data transfer, calculation result transfer, chain transfer
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> • 1 input-only port • 49 CMOS I/O ports • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:

1. Contact a Renesas Electronics sales office to use the optional features.

Table 1.4 Performance Overview for the 64-pin Package (2/2)

Unit	Function	Explanation
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 ⁽¹⁾ Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART3, UART5, UART8	Asynchronous/synchronous serial interface × 6 channels • I ² C-bus (UART0 to UART3, UART5) • Special mode 2 (UART0 to UART3, UART5) • IEBus (optional ⁽²⁾) (UART0 to UART3, UART5)
A/D Converter		10-bit resolution × 20 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 1
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 19 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional ⁽²⁾)
Flash Memory		Programming and erasure supply voltage: VCC1 = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		50 MHz/VCC1 = 3.0 to 5.5 V
Operating Temperature		-40°C to 85°C (D version)
Current Consumption		32 mA (VCC1 = 5.0 V, f(CPU) = 50 MHz) 8 μA (VCC1 = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		64-pin plastic molded LQFP (PLQP0064KB-A)

Notes:

1. Timer B4 is available in timer mode only.
2. Contact a Renesas Electronics sales office to use the optional features.

1.2 Product Information

Table 1.5 lists the product information and Figure 1.1 shows the details of the part number.

Table 1.5 R32C/111 Group Product List

As of March, 2014

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F64110DFB	PLQP0100KB-A	256 Kbytes +8 Kbytes	63 Kbytes	-40°C to 85°C (D version)
R5F64111DFB		384 Kbytes +8 Kbytes		
R5F64112DFB		512 Kbytes +8 Kbytes		
R5F64114DFB		256 Kbytes +8 Kbytes	40 Kbytes	
R5F64115DFB		384 Kbytes +8 Kbytes		
R5F64116DFB		512 Kbytes +8 Kbytes		
R5F64111NLG	PTLG0100KA-A	384 Kbytes +8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64112NLG		512 Kbytes +8 Kbytes		
R5F6411FNLG		256 Kbytes +8 Kbytes	32 Kbytes	
R5F6411EDFN	PLQP064KB-A	128 Kbytes +8 Kbytes	32 Kbytes	-40°C to 85°C (D version)
R5F6411FDFN		256 Kbytes +8 Kbytes		

Notes:

- The old package codes are as follows:
 PLQP0100KB-A: 100P6Q-A
 PTLG0100KA-A: 100F0M
 PLQP0064KB-A: 64P6Q-A
- “+ 8 Kbytes” in the ROM capacity column indicates the data flash capacity.

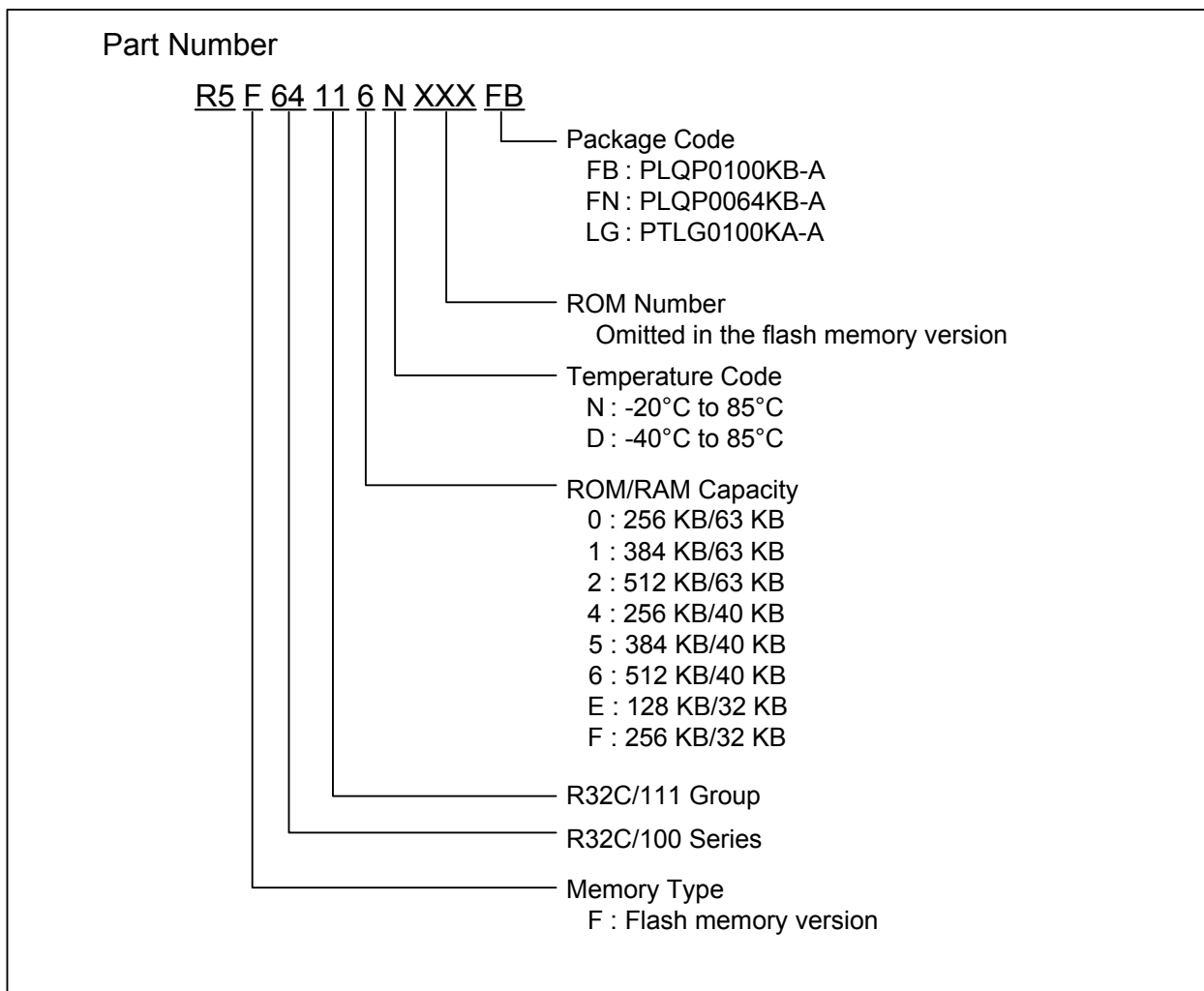


Figure 1.1 Part Numbering

1.3 Block Diagram

Figures 1.2 and 1.3 show block diagram of the R32C/111 Group.

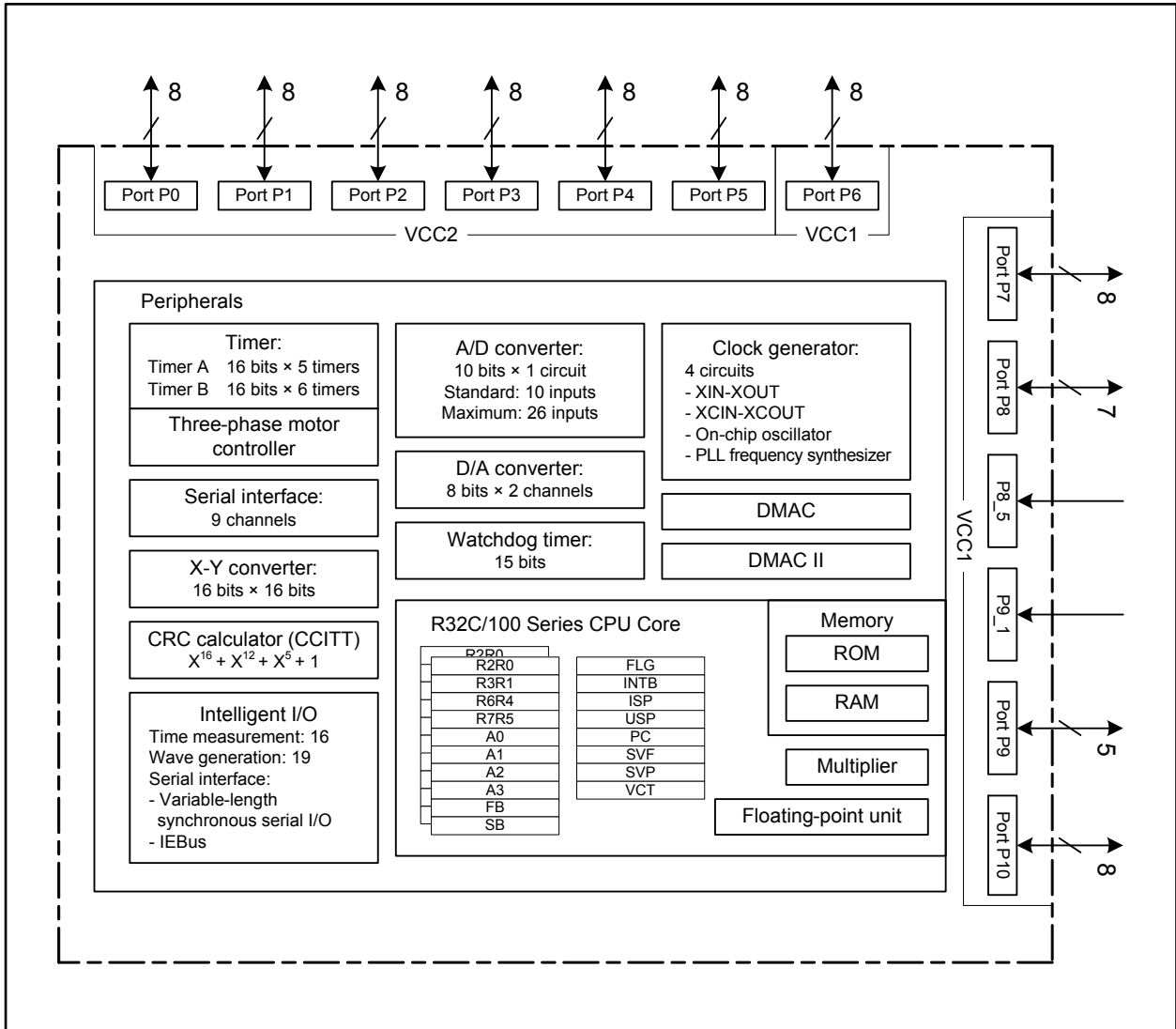


Figure 1.2 R32C/111 Group Block Diagram for the 100-pin Package

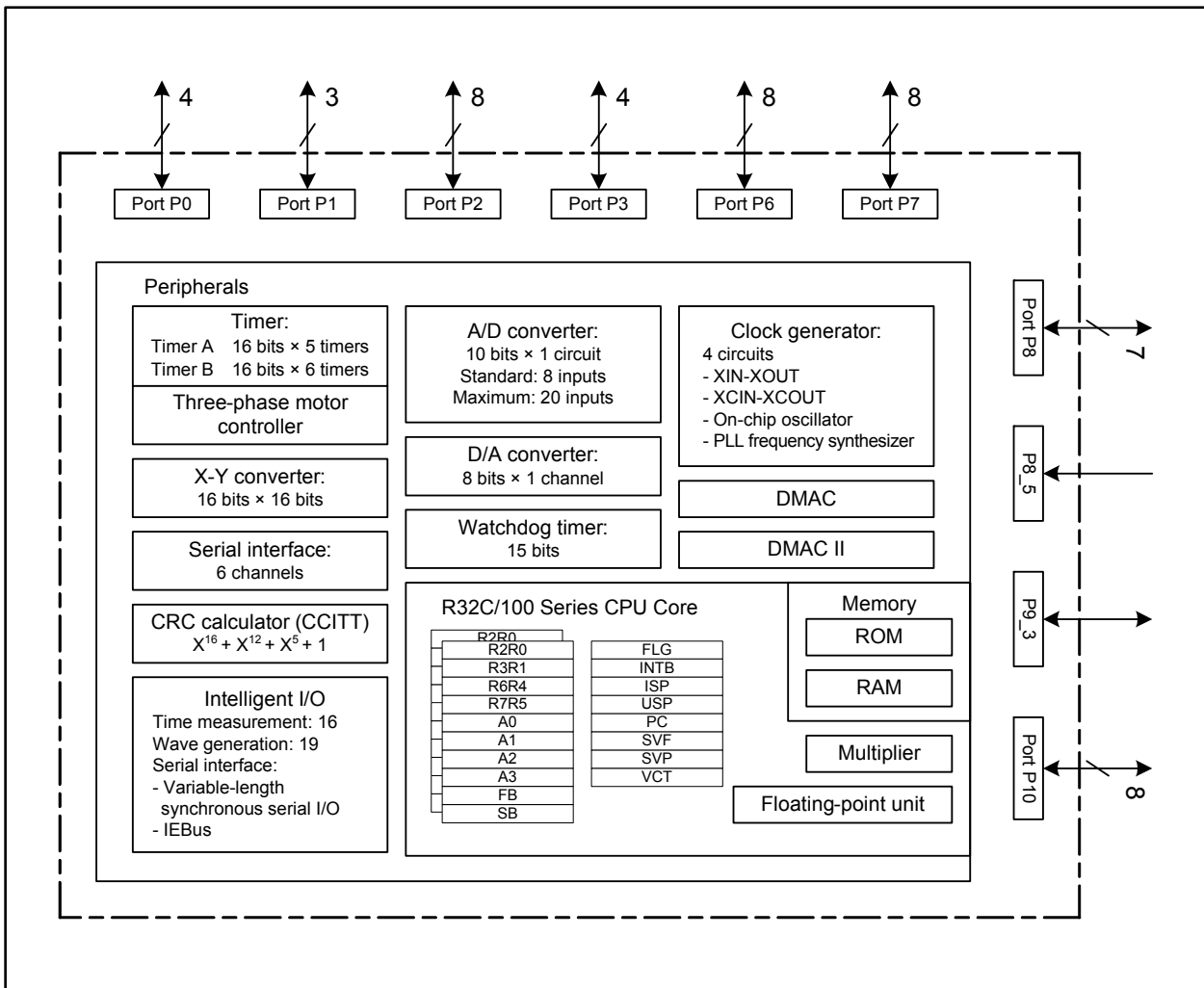


Figure 1.3 R32C/111 Group Block Diagram for the 64-pin Package

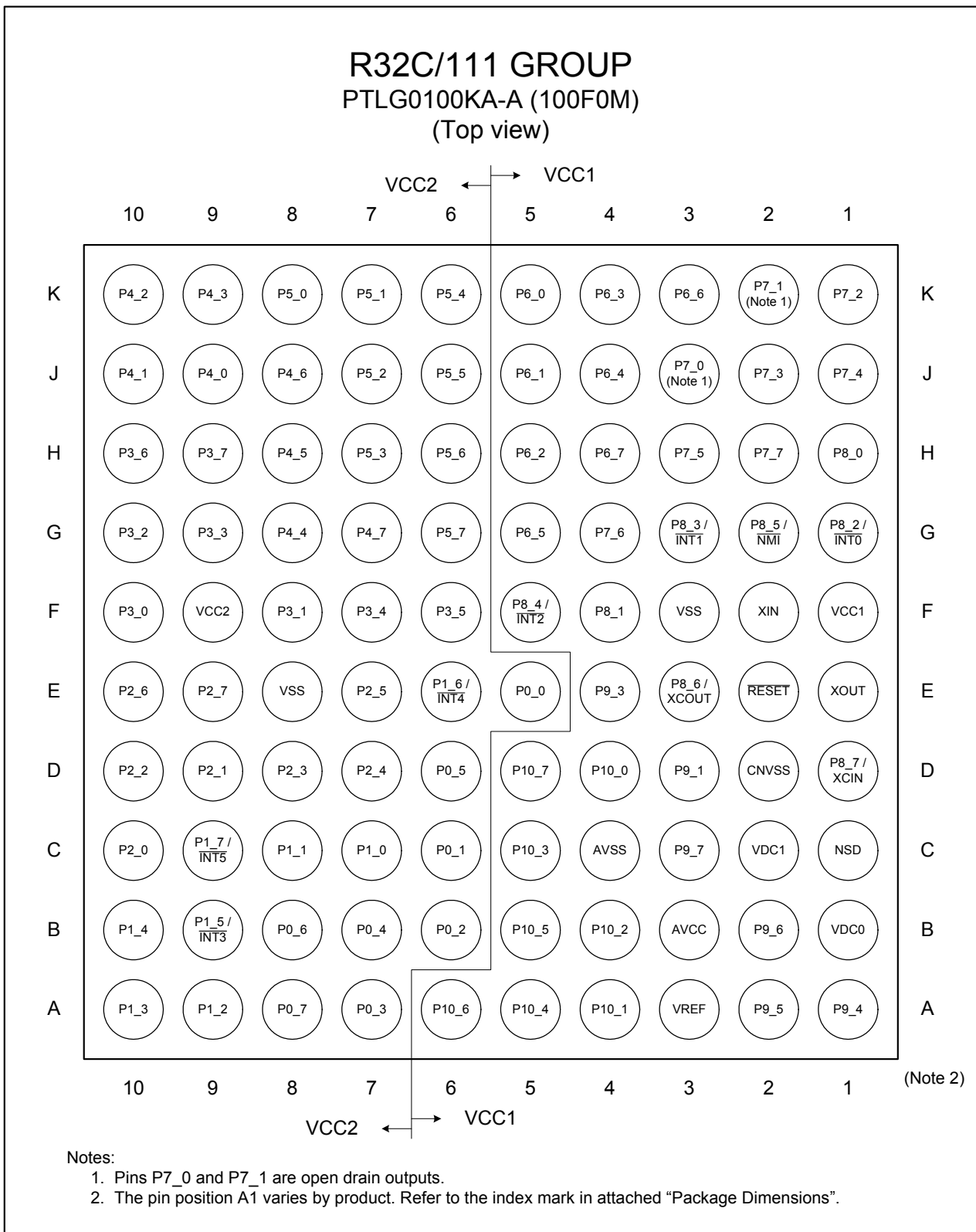


Figure 1.5 Pin Assignment for the 100-pin LGA Package (top view)

Table 1.6 Pin Characteristics for the 100-pin Package (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
1	A1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
2	E4		P9_3		TB3IN			DA0	
3	B1	VDC0							
4	D3		P9_1						
5	C2	VDC1							
6	C1	NSD							
7	D2	CNVSS							
8	D1	XCIN	P8_7						
9	E3	XCOU	P8_6						
10	E2	RESET							
11	E1	XOUT							
12	F3	VSS							
13	F2	XIN							
14	F1	VCC1							
15	G2		P8_5	NMI					
16	F5		P8_4	INT2					
17	G3		P8_3	INT1					
18	G1		P8_2	INT0					
19	F4		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
20	H1		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
21	H2		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B		
22	G4		P7_6		TA3OUT	TXD5/SDA5/ SRXD5/CTS8/RTS8	IIO1_3/UD0A/UD1A		
23	H3		P7_5		TA2IN/W	RXD8	IIO1_2		
24	J1		P7_4		TA2OUT/W	CLK8	IIO1_1		
25	J2		P7_3		TA1IN/V	CTS2/RTS2/SS2/ TXD8	IIO1_0		
26	K1		P7_2		TA1OUT/V	CLK2			
27	K2		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN		
28	J3		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
29	H4		P6_7			TXD1/SDA1/SRXD1			
30	K3		P6_6			RXD1/SCL1/STXD1			
31	G5		P6_5			CLK1			
32	J4		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
33	K4		P6_3			TXD0/SDA0/SRXD0			
34	H5		P6_2		TB2IN	RXD0/SCL0/STXD0			
35	J5		P6_1		TB1IN	CLK0			
36	K5		P6_0		TB0IN	CTS0/RTS0/SS0			
37	G6		P5_7			CTS7/RTS7			RDY/CS3
38	H6		P5_6			RXD7			ALE/CS2
39	J6		P5_5			CLK7			HOLD

Table 1.7 Pin Characteristics for the 100-pin Package (2/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
40	K6		P5_4			TXD7			HLDA/CS1
41	H7		P5_3						CLKOUT/ BCLK
42	J7		P5_2						RD
43	K7		P5_1						WR1/BC1
44	K8		P5_0						WR0/WR
45	G7		P4_7			TXD6/SDA6/SRXD6			CS0/A23
46	J8		P4_6			RXD6/SCL6/STXD6			CS1/A22
47	H8		P4_5			CLK6			CS2/A21
48	G8		P4_4			CTS6/RTS6/SS6			CS3/A20
49	K9		P4_3			TXD3/SDA3/SRXD3	OUTC2_0/ISTXD2/ IEOUT		A19
50	K10		P4_2			RXD3/SCL3/STXD3	ISRXD2/IEIN		A18
51	J10		P4_1			CLK3			A17
52	J9		P4_0			CTS3/RTS3/SS3			A16
53	H9		P3_7		TA4IN/U				A15(/D15)
54	H10		P3_6		TA4OUT/U				A14(/D14)
55	F6		P3_5		TA2IN/W				A13(/D13)
56	F7		P3_4		TA2OUT/W				A12(/D12)
57	G9		P3_3		TA1IN/V				A11(/D11)
58	G10		P3_2		TA1OUT/V				A10(/D10)
59	F8		P3_1		TA3OUT		UD0B/UD1B		A9(/D9)
60	F9	VCC2							
61	F10		P3_0		TA0OUT		UD0A/UD1A		A8(/D8)
62	E8	VSS							
63	E9		P2_7					AN2_7	A7(/D7)
64	E10		P2_6					AN2_6	A6(/D6)
65	E7		P2_5					AN2_5	A5(/D5)
66	D7		P2_4					AN2_4	A4(/D4)
67	D8		P2_3					AN2_3	A3(/D3)
68	D10		P2_2					AN2_2	A2(/D2)
69	D9		P2_1					AN2_1	A1(/D1)
70	C10		P2_0					AN2_0	A0(/D0)/ BC0(/D0)
71	C9		P1_7	INT5			IIO0_7/IIO1_7		D15
72	E6		P1_6	INT4			IIO0_6/IIO1_6		D14
73	B9		P1_5	INT3			IIO0_5/IIO1_5		D13
74	B10		P1_4				IIO0_4/IIO1_4		D12
75	A10		P1_3				IIO0_3/IIO1_3		D11
76	A9		P1_2				IIO0_2/IIO1_2		D10
77	C8		P1_1				IIO0_1/IIO1_1		D9
78	C7		P1_0				IIO0_0/IIO1_0		D8
79	A8		P0_7					AN0_7	D7

Table 1.8 Pin Characteristics for the 100-pin Package (3/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
80	B8		P0_6					AN0_6	D6
81	D6		P0_5					AN0_5	D5
82	B7		P0_4					AN0_4	D4
83	A7		P0_3					AN0_3	D3
84	B6		P0_2					AN0_2	D2
85	C6		P0_1					AN0_1	D1
86	E5		P0_0					AN0_0	D0
87	D5		P10_7	KI3				AN_7	
88	A6		P10_6	KI2				AN_6	
89	B5		P10_5	KI1				AN_5	
90	A5		P10_4	KI0				AN_4	
91	C5		P10_3					AN_3	
92	B4		P10_2					AN_2	
93	A4		P10_1					AN_1	
94	C4	AVSS							
95	D4		P10_0					AN_0	
96	A3	VREF							
97	B3	AVCC							
98	C3		P9_7			RXD4/SCL4/STXD4		ADTRG	
99	B2		P9_6			TXD4/SDA4/SRXD4		ANEX1	
100	A2		P9_5			CLK4		ANEX0	

Table 1.9 Pin Characteristics for the 64-pin Package (1/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin
1	VDC1						
2	NSD						
3	CNVSS						
4	XCIN	P8_7					
5	XCOU \bar{T}	P8_6					
6	RESE \bar{T}						
7	XOUT						
8	VSS						
9	XIN						
10	VCC1						
11		P8_5	NMI				
12		P8_4	INT2				
13		P8_3	INT1				
14		P8_2	INT0				
15		P8_1		TA4IN/ \bar{U}	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B	
16		P8_0		TA4OUT/ \bar{U}	RXD5/SCL5/STXD5	UD0A/UD1A	
17		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B	
18		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ CTS8/RTS8	IIO1_3/UD0A/UD1A	
19		P7_5		TA2IN/ \bar{W}	RXD8	IIO1_2	
20		P7_4		TA2OUT/ \bar{W}	CLK8	IIO1_1	
21		P7_3		TA1IN/ \bar{V}	CTS2/RTS2/SS2/TXD8	IIO1_0	
22		P7_2		TA1OUT/ \bar{V}	CLK2		
23		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN	
24		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT	
25		P6_7			TXD1/SDA1/SRXD1		
26		P6_6			RXD1/SCL1/STXD1		
27		P6_5			CLK1		
28		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2	
29		P3_3		TA1IN/ \bar{V}	CTS3/RTS3/SS3		
30		P3_2		TA1OUT/ \bar{V}	TXD3/SDA3/SRXD3		
31		P3_1		TA3OUT	RXD3/SCL3/STXD3	UD0B/UD1B	
32		P3_0		TA0OUT	CLK3	UD0A/UD1A	
33		P6_3			TXD0/SDA0/SRXD0		
34		P6_2		TB2IN	RXD0/SCL0/STXD0		
35		P6_1		TB1IN	CLK0		
36		P6_0		TB0IN	CTS0/RTS0/SS0		
37		P2_7				IIO0_7	AN2_7
38		P2_6				IIO0_6	AN2_6
39		P2_5				IIO0_5	AN2_5
40		P2_4				IIO0_4	AN2_4

Table 1.10 Pin Characteristics for the 64-pin Package (2/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin
41		P2_3				IIO0_3	AN2_3
42		P2_2				IIO0_2	AN2_2
43		P2_1				IIO0_1	AN2_1
44		P2_0				IIO0_0	AN2_0
45		P1_7	$\overline{\text{INT5}}$			IIO0_7/IIO1_7	
46		P1_6	$\overline{\text{INT4}}$			IIO0_6/IIO1_6	
47		P1_5	$\overline{\text{INT3}}$			IIO0_5/IIO1_5	$\overline{\text{ADTRG}}$
48		P0_3					AN0_3
49		P0_2					AN0_2
50		P0_1					AN0_1
51		P0_0					AN0_0
52		P10_7	$\overline{\text{KI3}}$				AN_7
53		P10_6	$\overline{\text{KI2}}$				AN_6
54		P10_5	$\overline{\text{KI1}}$				AN_5
55		P10_4	$\overline{\text{KI0}}$				AN_4
56		P10_3					AN_3
57		P10_2					AN_2
58		P10_1					AN_1
59	AVSS						
60		P10_0					AN_0
61	VREF						
62	AVCC						
63		P9_3		TB3IN			DA0
64	VDC0						

1.5 Pin Definitions and Functions

Tables 1.11 to 1.17 show the pin definitions and functions.

Table 1.11 Pin Definitions and Functions for the 100-pin Package (1/4)

Function	Symbol	I/O	Power Supply	Description
Power supply	VCC1, VCC2, VSS	I	—	Applicable as follows: VCC1 and VCC2 = 3.0 to 5.5 V (VCC1 ≥ VCC2), VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	VCC1	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC1 and VSS, respectively
Reset input	RESET	I	VCC1	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	VCC1	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	VCC1	This pin is to communicate with a debugger. It should be connected to VCC1 via a resistor of 1 to 4.7 kΩ
Main clock input	XIN	I	VCC1	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOU. An external clock should be input at the XCIN while leaving the XCOU open
Sub clock output	XCOU	O	VCC1	
BCLK output	BCLK	O	VCC2	BCLK output
Clock output	CLKOUT	O	VCC2	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	INT0 to INT5	I	VCC1 VCC2	Input for external interrupts
NMI input	P8_5/NMI	I	VCC1	Input for NMI
Key input interrupt	KI0 to KI3	I	VCC1	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	VCC2	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	VCC2	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A23	O	VCC2	Output of address bits A0 to A23

Table 1.12 Pin Definitions and Functions for the 100-pin Package (2/4)

Function	Symbol	I/O	Power Supply	Description
Bus control pins	A0/D0 to A7/D7	I/O	VCC2	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit multiplexed bus
	$\overline{BC0}/D0$	I/O	VCC2	Output of byte control ($\overline{BC0}$) and input/output of data (D0) by time-division while accessing an external memory space with multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	VCC2	Chip select output
	$\overline{WR0}/\overline{WR1}/\overline{WR}/\overline{BC0}/\overline{BC1}/\overline{RD}$	O	VCC2	Output of write, byte control, and read signals. Either \overline{WRx} or \overline{WR} and \overline{BCx} can be selected by a program. Data is read when \overline{RD} is low. <ul style="list-style-type: none"> • When $\overline{WR0}$, $\overline{WR1}$, and \overline{RD} are selected, data is written to the following address: an even address, when $\overline{WR0}$ is low an odd address, when $\overline{WR1}$ is low on 16-bit external data bus • When \overline{WR}, $\overline{BC0}$, $\overline{BC1}$, and \overline{RD} are selected, data is written, when \overline{WR} is low and the following address is accessed: an even address, when $\overline{BC0}$ is low an odd address, when $\overline{BC1}$ is low on 16-bit external data bus
	ALE	O	VCC2	Latch enable signal in multiplexed bus format
	\overline{HOLD}	I	VCC2	The MCU is in a hold state while this pin is held low
	HLDA	O	VCC2	This pin is driven low while the MCU is held in a hold state
	\overline{RDY}	I	VCC2	Bus cycle is extended by the CPU if this pin is low on the falling edge of BCLK

Table 1.13 Pin Definitions and Functions for the 100-pin Package (3/4)

Function	Symbol	I/O	Power Supply	Description
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7,	I/O	VCC2	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Pull-up resistors are selected for the following 4-pin units: Pi_0 to Pi_3 and Pi_4 to Pi_7 (i = 0 to 10); however, they are enabled only for the input pins. P7_0 and P7_1 outputs are N-channel open drain
	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7	I/O	VCC1	
Input port	P9_1	I	VCC1	Input port in CMOS. Pull-up resistors are selectable for P9_1 and P9_3
Timer A	TA0OUT to TA4OUT	I/O	VCC1 VCC2	Timers A0 to A4 input/output. TA0OUT output assigned for port P7_0 is N-channel open drain
	TA0IN to TA4IN	I	VCC1 VCC2	Timers A0 to A4 input
Timer B	TB0IN to TB5IN	I	VCC1	Timers B0 to B5 input
Three-phase motor control timer output	U, \bar{U} , V, \bar{V} , W, \bar{W}	O	VCC1 VCC2	Three-phase motor control timer output
Serial interface	$\overline{CTS0}$ to $\overline{CTS8}$	I	VCC1 VCC2	Handshake input
	$\overline{RTS0}$ to $\overline{RTS8}$	O	VCC1 VCC2	Handshake output
	CLK0 to CLK8	I/O	VCC1 VCC2	Transmit/receive clock input/output
	RXD0 to RXD8	I	VCC1 VCC2	Serial data input
	TXD0 to TXD8	O	VCC1 VCC2	Serial data output. TXD2 output is N-channel open drain
I ² C-bus (simplified)	SDA0 to SDA6	I/O	VCC1 VCC2	Serial data input/output. SDA2 output is N-channel open drain
	SCL0 to SCL6	I/O	VCC1 VCC2	Transmit/receive clock input/output. SCL2 output is N-channel open drain

Table 1.14 Pin Definitions and Functions for the 100-pin Package (4/4)

Function	Symbol	I/O	Power Supply	Description
Serial interface special functions	STXD0 to STXD6	O	VCC1 VCC2	Serial data output in slave mode. STXD2 is N-channel open drain
	SRXD0 to SRXD6	I	VCC1 VCC2	Serial data input in slave mode
	$\overline{SS}0$ to $\overline{SS}6$	I	VCC1 VCC2	Input to control serial interface special functions
A/D converter	AN_0 to AN_7	I	VCC1	Analog input for the A/D converter
	AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC2	
	ADTRG	I	VCC1	External trigger input for the A/D converter
	ANEX0	I/O	VCC1	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	VCC1	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	VCC1	Output for the D/A converter
Reference voltage input	VREF	I	–	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	VCC1 VCC2	Input/output for Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	VCC1 VCC2	Input/output for Intelligent I/O group 1. Either input capture or output compare is selectable. IIO1_6 and IIO1_7 outputs assigned for ports P7_0 and P7_1 are N-channel open drain
	UD0A, UD0B, UD1A, UD1B	I	VCC1 VCC2	Input for the two-phase encoder
	OUTC2_0 to OUTC2_2	O	VCC1 VCC2	Output for OC (output compare) of Intelligent I/O group 2. OUTC2_0 and OUTC2_2 assigned for ports P7_0 and P7_1 are N-channel open drain
	ISCLK2	I/O	VCC1 VCC2	Clock input/output for the serial interface
	ISRXD2	I		Receive data input for the serial interface
	ISTXD2	O		Transmit data output for the serial interface. ISTXD2 assigned for port P7_0 is N-channel open drain
	IEIN	I	VCC1 VCC2	Receive data input for the serial interface
	IEOUT	O		Transmit data output for the serial interface. IEOUT assigned for port P7_0 is N-channel open drain

Table 1.15 Pin Definitions and Functions for 64-pin Package (1/3)

Function	Symbol	I/O	Description
Power supply	VCC1, VSS	I	Applicable as follows: VCC1 = 3.0 to 5.5 V, VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC1 via a resistor of 1 to 4.7 k Ω
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOU. An external clock should be input at the XCIN while leaving the XCOU open
Sub clock output	XCOU	O	
External interrupt input	INT0 to INT5	I	Input for external interrupts
NMI input	P8_5/ $\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	KI0 to KI3	I	Input for the key input interrupt
I/O port	P0_0 to P0_3, P1_5 to P1_7, P2_0 to P2_7, P3_0 to P3_3, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3, P10_0 to P10_7	I/O	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Pull-up resistors are selected for the following 4-pin units: Pi_0 to Pi_3 and Pi_4 to Pi_7 (i = 0 to 3, 6 to 10); however, they are enabled only for the input pins. P7_0 and P7_1 outputs are N-channel open drain
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output. TA0OUT output assigned for port P7_0 is N-channel open drain
	TA0IN to TA4IN	I	Timers A0 to A4 input
Timer B	TB0IN to TB3IN, TB5IN	I	Timers B0 to B3, and B5 input
Three-phase motor control timer output	U, \overline{U} , V, \overline{V} , W, \overline{W}	O	Three-phase motor control timer output

Table 1.16 Pin Definitions and Functions for the 64-pin Package (2/3)

Function	Symbol	I/O	Description
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS3}}$, $\overline{\text{CTS5}}$, $\overline{\text{CTS8}}$	I	Handshake input
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS3}}$, $\overline{\text{RTS5}}$, $\overline{\text{RTS8}}$	O	Handshake output
	CLK0 to CLK3, CLK5, CLK8	I/O	Transmit/receive clock input/output
	RXD0 to RXD3, RXD5, RXD8	I	Serial data input
	TXD0 to TXD3, TXD5, TXD8	O	Serial data output. TXD2 output is N-channel open drain
I ² C-bus (simplified)	SDA0 to SDA3, SDA5	I/O	Serial data input/output. SDA2 output is N-channel open drain
	SCL0 to SCL3, SCL5	I/O	Transmit/receive clock input/output. SCL2 output is N-channel open drain
Serial interface special functions	STXD0 to STXD3, STXD5	O	Serial data output in slave mode. STXD2 is N-channel open drain
	SRXD0 to SRXD3, SRXD5	I	Serial data input in slave mode
	$\overline{\text{SS0}}$ to $\overline{\text{SS3}}$, $\overline{\text{SS5}}$	I	Input to control serial interface special functions
A/D converter	AN_0 to AN_7, AN0_0 to AN0_3, AN2_0 to AN2_7	I	Analog input for the A/D converter
	ADTRG	I	External trigger input for the A/D converter
D/A converter	DA0	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter

Table 1.17 Pin Definitions and Functions for the 64-pin Package (3/3)

Function	Symbol	I/O	Description
Intelligent I/O	IIO0_0 to IIO0_7	I/O	Input/output for Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	Input/output for Intelligent I/O group 1. Either input capture or output compare is selectable. IIO1_6 and IIO1_7 outputs assigned for ports P7_0 and P7_1 are N-channel open drain
	UD0A, UD0B, UD1A, UD1B	I	Input for the two-phase encoder
	OUTC2_0 to OUTC2_2	O	Output for OC (output compare) of Intelligent I/O group 2. OUTC2_0 and OUTC2_2 assigned for ports P7_0 and P7_1 are N-channel open drain
	ISCLK2	I/O	Clock input/output for the serial interface
	ISRXD2	I	Receive data input for the serial interface
	ISTXD2	O	Transmit data output for the serial interface. ISTXD2 assigned for port P7_0 is N-channel open drain
	IEIN	I	Receive data input for the serial interface
	IEOUT	O	Transmit data output for the serial interface. IEOUT assigned for port P7_0 is N-channel open drain

2. Central Processing Unit (CPU)

The CPU contains the registers shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.

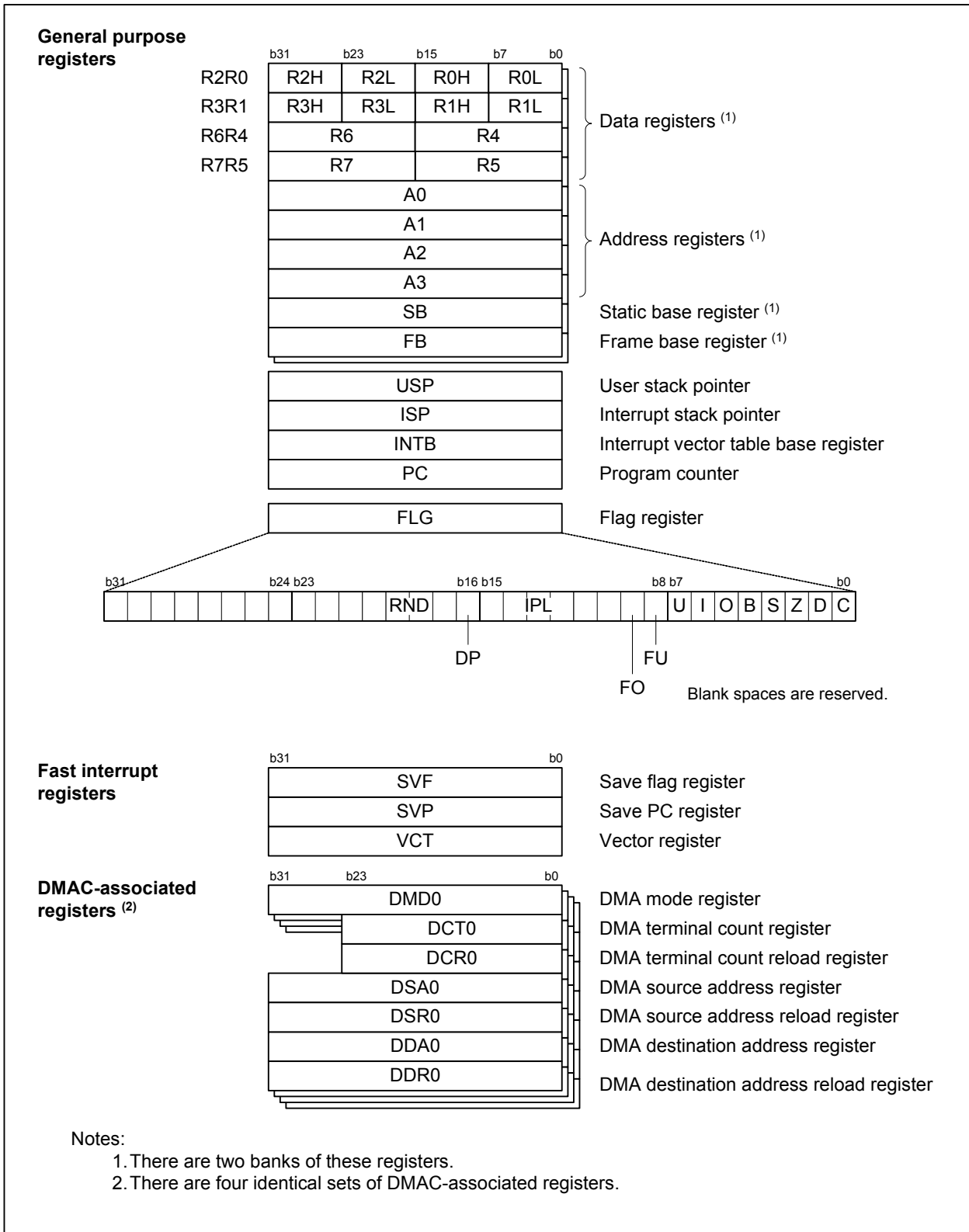


Figure 2.1 CPU Registers