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RENESAS

User's Manual

V850ES/IE2

32-bit Single-Chip Microcontrollers

Hardware

μPD70F3713
μPD70F3714

Document No. U17716EJ2V0UD00 (2nd edition)
Date Published February 2008 N

Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

PREFACE

Readers

This manual is intended for users who wish to understand the functions of the V850ES/IE2 to design application systems using the V850ES/IE2.

Purpose

This manual is intended to give users an understanding of the hardware functions.

Organization

The V850ES/IE2 User's Manual is divided into two parts: Hardware (this manual) and Architecture (V850ES Architecture User's Manual). The organization of each manual is as follows:

Hardware	Architecture
• Pin functions	• Data type
• CPU function	• Register set
• On-chip peripheral functions	• Instruction format and instruction set
• Flash memory programming	• Interrupts and exceptions
• Electrical specifications	• Pipeline operation

How to Read This Manual

It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

- To understand the overall functions of the V850ES/IE2
  →Read this manual according to the **CONTENTS**.

- To find the details of a register where the name is known
  →See **APPENDIX B REGISTER INDEX**.

- How to interpret the register format
  →For a bit whose bit number is enclosed in angle brackets < >, its bit name is defined as a reserved word in the device file.

- To understand the details of an instruction function
  →Refer to the **V850ES Architecture User's Manual**.

- To know the electrical specifications of the V850ES/IE2
  →See **CHAPTER 19 ELECTRICAL SPECIFICATIONS**.

The "yyy bit of the xxx register" is described as the "xxx.yyy bit" in this manual. Note with caution that if "xxx.yyy" is described as is in a program, however, the compiler/assembler cannot recognize it correctly.

The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Higher addresses on the top and lower addresses on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Prefix indicating power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$
Data type:	Word ... 32 bits
	Halfword ... 16 bits
	Byte ... 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850ES/IE2

Document Name	Document No.
V850ES Architecture User's Manual	U15943E
V850ES/IE2 Hardware User's Manual	This manual

Documents related to development tools (user's manuals)

Document Name		Document No.
QB-V850ESIX2 (in-circuit emulator)		U17909E
QB-MINI2 (On-Chip Debug Emulator with Programming Function)		U18371E
CA850 (Ver. 3.00) (C compiler package)	Operation	U17293E
	C Language	U17291E
	Assembly Language	U17292E
	Link Directive	U17294E
PM+ (Ver. 6.30) (Project manager)		U18416E
ID850QB (Ver. 3.40) (Integrated debugger)	Operation	U18604E
TW850 (Ver. 2.00) (Performance analysis tuning tool)		U17241E
RX850 (Ver. 3.20) (Real-time OS)	Basics	U13430E
	Installation	U17419E
	Technical	U13431E
	Task Debugger	U17420E
RX850 Pro (Ver. 3.21) (Real-time OS)	Basics	U18165E
	Installation	U17421E
	Technical	U13772E
	Task Debugger	U17422E
AZ850 (Ver. 3.30) (System performance analyzer)		U17423E
PG-FP4 Flash Memory Programmer		U15260E
PG-FP5 Flash Memory Programmer		U18865E

CONTENTS

CHAPTER 1 INTRODUCTION

The V850ES/IE2 is one of the low-power operation products in the NEC Electronics V850 Series of single-chip microcontrollers designed for real-time control applications.

1.1 General

The V850ES/IE2 is a 32-bit single-chip microcontroller that includes the V850ES CPU core and peripheral functions such as ROM/RAM, a timer/counter, serial interfaces, a watchdog timer, and an A/D converter.

In addition to high real-time response characteristics and 1-clock-pitch basic instructions, the V850ES/IE2 features instructions such as multiply instructions, saturated operation instructions, and bit manipulation instructions realized by a hardware multiplier, as optimum instructions for digital servo control applications. Moreover, as a real-time control system, the V850ES/IE2 enables an extremely high cost-performance for applications such as motor inverter control.

1.2 Features

○ Minimum instruction execution time:
50 ns (at internal 20 MHz operation)

○ General-purpose registers: 32 bits × 32

○ CPU features:
Signed multiplication (16 × 16 → 32): 1 to 2 clocks
Signed multiplication (32 × 32 → 64): 1 to 5 clocks
Saturated operation instructions (with overflow/underflow detection function)
32-bit shift instructions: 1 clock
Bit manipulation instructions
Load/store instructions with long/short format
Signed load instructions

○ Internal memory:

Part Number	Internal ROM	Internal RAM
μPD70F3713	64 KB (flash memory)	6 KB
μPD70F3714	128 KB (flash memory)	6 KB

○ Interrupts/exceptions:
Non-maskable interrupts: 1 source (external: none, internal: 1)
Maskable interrupts: 42 sources (external: 7, internal: 35)
Software exceptions: 32 sources
Exception traps: 2 sources

○ I/O lines:
I/O ports: 39

○ Timer/counter function:
16-bit interval timer M (TMM): 1 channel
16-bit timer/event counter Q (TMQ): 2 channels
16-bit timer/event counter P (TMP): 4 channels
Motor control function (uses timer TMQ: 1 channel (TMQ1), TMP: 1 channel (TMP1))
16-bit accuracy 6-phase PWM function with dead time: 1 channel
High-impedance output control function
Timer tuning operation function
Arbitrary cycle setting function
Arbitrary dead-time setting function
Watchdog timer: 1 channel

○ Serial interfaces:
Asynchronous serial interface A (UARTA)
3-wire variable length serial I/O (CSIB)
CSIB: 1 channel
UARTA: 2 channels

○ A/D converter:
10-bit resolution A/D converters (A/D converters 0 and 1): 4 channels × 2 units

- Clock generator: 2.5 MHz resonator connectable (external clock input prohibited)
  Multiplication function by PLL clock synthesizer (fixed to multiplication by eight, f_{XX} = 20 MHz)
  CPU clock division function (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$)
- Power-save function: HALT/IDLE/ STOP mode
- Power-on-clear function
- Low-voltage detection function
- Self programming: Supported only in the μPD70F3714 (not supported in the μPD70F3713)
- Package: 64-pin plastic LQFP (14 × 14)
- Operation supply voltage: $V_{DD} = EV_{DD}$ = 3.5 to 5.5 V
  AV_{DD0}, AV_{DD1} = 4.5 to 5.5 V
- Operation ambient temperature:
  T_A = –40 to +85°C

1.3 Applications

- Consumer appliances (such as inverter air conditioners, refrigerators, washing machines, etc.)
- Industrial equipment (such as motor control and general-purpose inverters, etc.)

1.4 Ordering Information

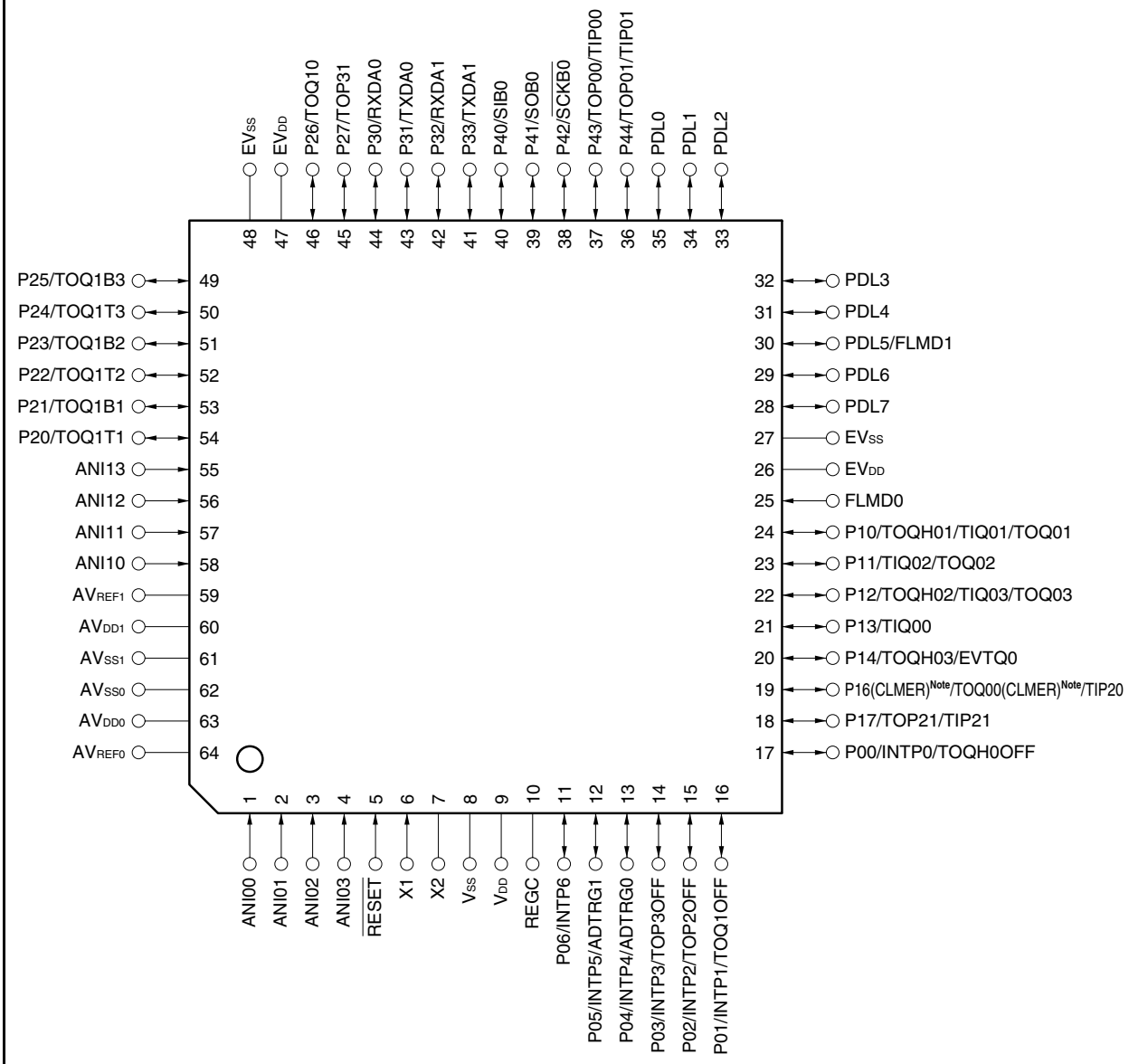
Part Number	Package	Internal ROM
μPD70F3713GC-8BS-A	64-pin plastic LQFP (14 × 14)	Flash memory (64 KB)
μPD70F3714GC-8BS-A	64-pin plastic LQFP (14 × 14)	Flash memory (128 KB)

Remark Products with -A at the end of the part number are lead-free products.

1.5 Pin Configuration

- **64-pin plastic LQFP (14 × 14)**
  μPD70F3713GC-8BS-A
  μPD70F3714GC-8BS-A

Top View



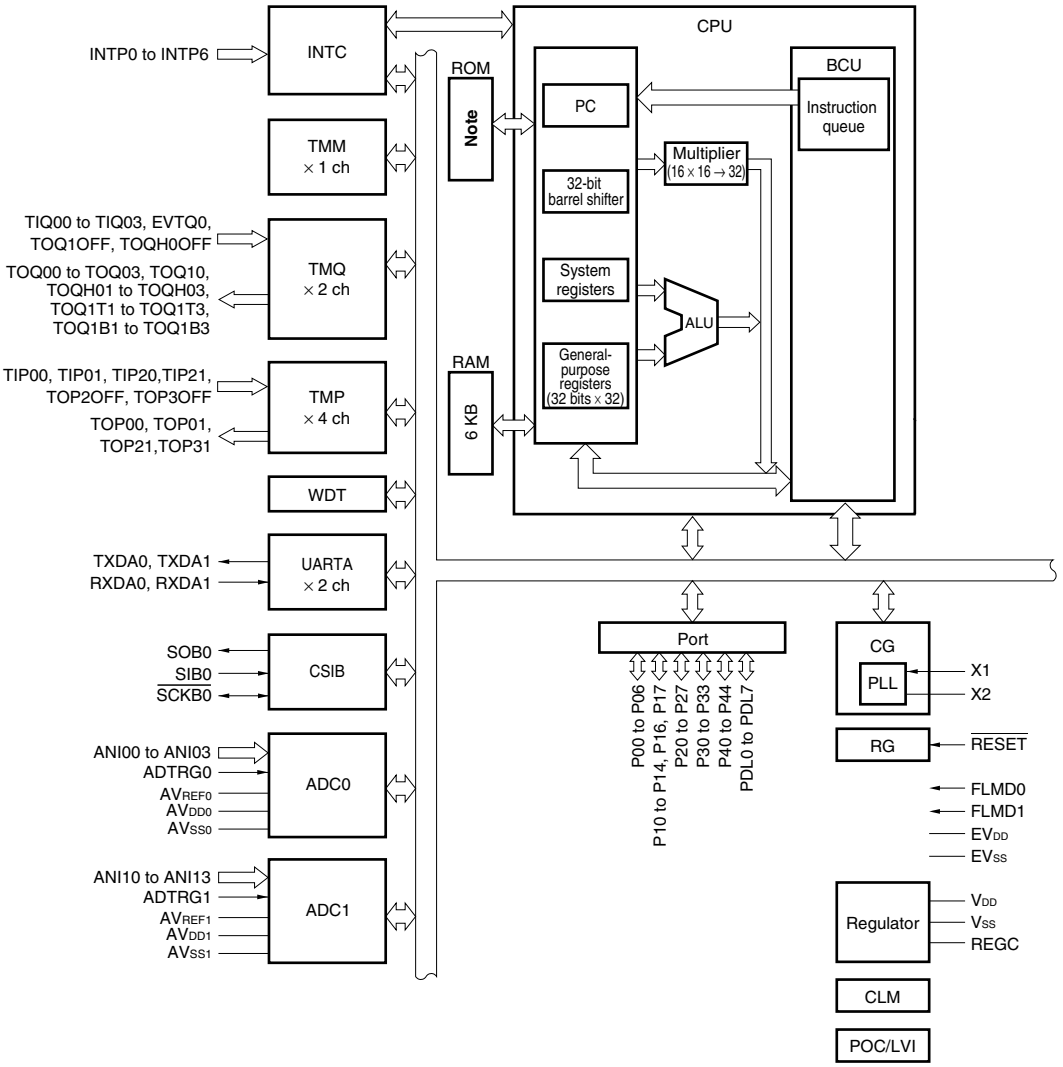
Note The CLMER signal is enabled only when P16 is specified as an output port or the output function of TOQ00. When an error (oscillator stop) is detected by the clock monitor, a low level is forcibly output. Low-level output is released by reset signal. For details, see **Table 4-5 Alternate-Function Pins of Port 1**.

Pin Identification

ADTRG0, ADTRG1:	A/D trigger input	$\overline{\text{SCKB0}}$:	Serial clock
ANI00 to ANI03,		SIB0:	Serial input
ANI10 to ANI13:	Analog input	SOB0:	Serial output
AV_{DD0}, AV_{DD1}:	Analog power supply	TIP00, TIP01,	
AV_{REF0}, AV_{REF1}:	Analog reference voltage	TIP20, TIP21,	
AV_{SS0}, AV_{SS1}:	Analog ground	TIQ00 to TIQ03:	Timer trigger input
EV_{DD}:	Power supply for port	TOP00, TOP01,	
EV_{SS}:	Ground for port	TOP21, TOP31,	
EVTQ0:	Timer event count input	TOQ1B1 to TOQ1B3,	
FLMD0, FLMD1:	Flash programming mode	TOQ1T1 to TOQ1T3,	
INTP0 to INTP6:	External interrupt input	TOQ00 to TOQ03,	
P00 to P06:	Port 0	TOQ10,	
P10 to P14, P16, P17:	Port 1	TOQH01 to TOQH03:	Timer output
P20 to P27:	Port 2	TOP2OFF, TOP3OFF,	
P30 to P33:	Port 3	TOQ1OFF, TOQH0OFF:	Timer output off
P40 to P44:	Port 4	TXDA0, TXDA1:	Transmit data
PDL0 to PDL7:	Port DL	V_{DD}:	Power supply
REGC:	Regulator control	V_{SS}:	Ground
$\overline{\text{RESET}}$:	Reset	X1, X2:	Clock oscillator pin
RXDA0, RXDA1:	Receive data		

1.6 Function Blocks

(1) Internal block diagram



Note μPD70F3713: 64 KB (flash memory)
μPD70F3714: 128 KB (flash memory)

(2) Internal units

(a) CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other instruction processing.

Other dedicated on-chip hardware, such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits), help accelerate complex processing.

(b) Bus control unit (BCU)

The BCU controls the internal bus.

(c) ROM

This is flash memory that is mapped from address 00000000H.

During instruction fetch, ROM/flash memory can be accessed from the CPU in 1-clock cycles. The internal ROM capacity and area differ as follows depending on the product.

Part Number	Internal ROM Capacity	Internal ROM Area
μPD70F3713	64 KB (flash memory)	xn000000H to xn00FFFFH
μPD70F3714	128 KB (flash memory)	xn000000H to xn01FFFFH

Remark n = xx11B

(d) RAM

This is a 6 KB internal RAM that is mapped to the addresses xnFFD800H to xnFFEFFFH.

During instruction fetch or data access, data can be accessed from the CPU in 1-clock cycles.

Remark n = xx11B

(e) Interrupt controller (INTC)

This controller handles hardware interrupt requests (INTP0 to INTP6) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiple-interrupt servicing control can be performed.

(f) Clock generator (CG)

The clock generator includes two basic operation modes: PLL mode (fixed to multiplication by eight) and clock-through mode. It generates four types of clocks (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$), and supplies one of them as the operating clock for the CPU (f_{CPU}).

(g) Timer/counter

This unit incorporates one 16-bit interval timer M (TMM) channel, two 16-bit timer/event counter Q (TMQ) channels, and four 16-bit timer/event counter P (TMP) channels, and can measure pulse interval widths or frequency, enable an inverter function for motor control, and output a programmable pulse.

(h) Watchdog timer (WDT)

A watchdog timer is equipped to detect program loops, system abnormalities, etc.

It generates a non-maskable interrupt request signal (INTWDT) or internal reset signal (WDTRES) after an overflow occurs.

(i) Serial interface

The V850ES/IE2 includes two asynchronous serial interface A (UARTA) channels and one 3-wire variable length serial I/O (CSIB) channel as the serial interface.

For UARTA, data is transferred via the TXDAn and RXDAn pins (n = 0, 1).

For CSIB, data is transferred via the SOB0, SIB0, and $\overline{\text{SCKB0}}$ pins.

(j) A/D converter (ADC)

The V850ES/IE2 includes two-channel 10-bit A/D converters (ADC0 and ADC1) with four analog input pins.

(k) Ports

As shown below, the following ports have general-purpose port functions and control pin functions.

Port	I/O	Alternate Function
Port 0	7-bit I/O	Timer/counter input, external interrupt input, external trigger input of A/D converter
Port 1	7-bit I/O	Timer/counter I/O
Port 2	8-bit I/O	Timer/counter output
Port 3	4-bit I/O	Serial interface I/O
Port 4	5-bit I/O	Serial interface I/O, timer/counter I/O
Port DL	8-bit I/O	–

CHAPTER 2 PIN FUNCTIONS

2.1 List of Pin Functions

The names and functions of the pins in the V850ES/IE2 are listed below. These pins can be divided into port pins and non-port pins according to their function.

There are two power supplies for the I/O buffer of a pin: power supply for A/D converter (AV_{DD0} and AV_{DD1}) and power supply for external pin (EV_{DD}). The relationship between each power supply and the pins is shown below.

Table 2-1. I/O Buffer Power Supplies for Each Pin

Power Supply	Corresponding Pins
AV_{DD0}, AV_{DD1}	ANI00 to ANI03, ANI10 to ANI13
EV_{DD}	Ports 0 to 4, port DL, $\overline{\text{RESET}}$

(1) Port pins

(1/2)

Pin Name	Pin No.	I/O	Function	Alternate Function
P00	17	I/O	Port 0 7-bit I/O port Input data read/output data write is enabled in 1-bit units. Use of an on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode and when the alternate function of the pin is used).	INTP0/TOQH0OFF
P01	16			INTP1/TOQ1OFF
P02	15			INTP2/TOP2OFF
P03	14			INTP3/TOP3OFF
P04	13			INTP4/ADTRG0
P05	12			INTP5/ADTRG1
P06	11			INTP6
P10	24	I/O	Port 1 7-bit I/O port Input data read/output data write is enabled in 1-bit units. Use of an on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode, when the input mode of alternate function of the pin is used, and when TOP21 and TOQH01 to TOQH03 pins, which function as output pins when their alternate function is used, go into a high-impedance state).	TOQH01/TIQ01/TOQ01
P11	23			TIQ02/TOQ02
P12	22			TOQH02/TIQ03/TOQ03
P13	21			TIQ00
P14	20			TOQH03/EVTQ0
P16 (CLMER)[Note]	19			TOQ00 (CLMER)[Note]/TIP20
P17	18			TOP21/TIP21

Note The CLMER signal is enabled only when P16 is specified as an output port or the output function of TOQ00. When an error (oscillator stop) is detected by the clock monitor, a low level is forcibly output. Low-level output is released by reset signal. For details, see **Table 4-5 Alternate-Function Pins of Port 1**.

(2/2)

Pin Name	Pin No.	I/O	Function	Alternate Function
P20	54	I/O	Port 2 8-bit I/O port Input data read/output data write is enabled in 1-bit units. Use of an on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode, or when TOQ1T1 to TOQ1T3 and TOQ1B1 to TOQ1B3 and TOP31 pins, which function as output pins when their alternate function is used, go into a high-impedance state).	TOQ1T1
P21	53			TOQ1B1
P22	52			TOQ1T2
P23	51			TOQ1B2
P24	50			TOQ1T3
P25	49			TOQ1B3
P26	46			TOQ10
P27	45			TOP31
P30	44	I/O	Port 3 4-bit I/O port Input data read/output data write is enabled in 1-bit units. Use of an on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode and when the input mode of the alternate function of the pin is used).	RXDA0
P31	43			TXDA0
P32	42			RXDA1
P33	41			TXDA1
P40	40	I/O	Port 4 5-bit I/O port Input data read/output data write is enabled in 1-bit units. An on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode, including the case where the $\overline{\text{SCKB0}}$ pin in the slave mode, and when the alternate function of the pin is used in the input mode).	SIB0
P41	39			SOB0
P42	38			$\overline{\text{SCKB0}}$
P43	37			TOP00/TIP00
P44	36			TOP01/TIP01
PDL0	35	I/O	Port DL 8-bit I/O port Input data read/output data write is enabled in 1-bit units. An on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected when the pins are in the port mode and input mode).	–
PDL1	34			–
PDL2	33			–
PDL3	32			–
PDL4	31			–
PDL5	30			FLMD1
PDL6	29			–
PDL7	28			–