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The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

SH7724

User's Manual: Hardware

Renesas 32-Bit RISC Microcomputer
SH7780 Series

R8A7724

[Portions omitted in accordance with NDA]

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(2012.4)

General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.

The NC (not connected) pins are either not connected to any of the internal circuitry or are they are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.

Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.

The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.

The undefined or reserved addresses may be used to expand functions, or test registers may have been allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

5. Reading from/Writing to Reserved Bit of Each Register

Note: Treat the reserved bit of register used in each module as follows except in cases where the specifications for values which are read from or written to the bit are provided in the description.

The bit is always read as 0. The write value should be 0 or one, which has been read immediately before writing.

Writing the value, which has been read immediately before writing has the advantage of preventing the bit from being affected on its extended function when the function is assigned.

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules

- CPU and System-Control Modules
- On-Chip Peripheral Modules

The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

- i) Feature
- ii) Input/Output Pin
- iii) Register Description
- iv) Operation
- v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. Electrical Characteristics
8. Appendix
9. Index

Preface

This LSI is a RISC (Reduced Instruction Set Computer) microcomputer which includes a Renesas original RISC CPU as its core, and the peripheral functions required to configure a system.

Target Users: This manual was written for users who will be using this LSI in the design of application systems. Users of this manual are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of this LSI to the above users.

Notes on reading this manual:

- In order to understand the overall functions of the chip
Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details on FPU functions and each instructions
Read the additional volume, SH-4A Extended Functions Software Manual.

Rules:

Bit order:	The MSB is on the left and the LSB is on the right.
Number notation:	Binary is B'xxxx, hexadecimal is H'xxxx, decimal is xxxx.
Signal notation:	An overbar is added to a low-active signal: $\overline{\text{xxxx}}$

Abbreviations

ATAPIATAPI Controller

CPG Clock Pulse Generator

DMAC Direct Memory Access Controller

E-DMAC Ethernet Controller Direct Memory Access Controller

EtherCEthernet Controller

FLCTL NAND Flash Memory Controller

G2D 2D Graphics Engine

GPIO General Purpose I/O

H-UDI User Debugging Interface

IIC I2C Bus Interface

INTC Interrupt Controller

MCU Memory Controller Unit

MMU Memory Management Unit

SCIF Serial Communication Interface with FIFO

TMU Timer Unit

UBC User Break Controller

USB USB Host/Function Interface

VDC2 Video Display Controller 2

WDT Watchdog Timer and Reset

SSI Serial Sound Interface

LCDC LCD Controller

SRC Sampling Rate Converter

bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
Hi-Z	High Impedance
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop

Main Revisions for This Edition

Item	Page	Revision (See Manual for Details)																																																								
1.3 Overview of Module Specifications	5	Table amended																																																								
Table 1.2 Overview of Module Specifications		<table border="1"> <thead> <tr> <th>Item</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Memory management unit (MMU)</td> <td> <ul style="list-style-type: none"> 4-Gbyte address space, 256 address space identifiers (8-bit ASIDs) </td> </tr> </tbody> </table>	Item	Description	Memory management unit (MMU)	<ul style="list-style-type: none"> 4-Gbyte address space, 256 address space identifiers (8-bit ASIDs) 																																																				
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1.5 Pin Assignment (BGA449)	19	Table amended																																																								
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109	E9	DV12_0	DV12	—	—	—	open																																																			
15.5.3 Initialization Sequence	447	Description amended																																																								
		<p>Before permitting accesses to the SDRAM after a reset, the SDRAM should be initialized according to the appropriate sequence as shown below. Since the shown sequence of issuing the commands to SDRAM is merely an example, provide the appropriate sequence given in the datasheet supplied by the memory vendor.</p>																																																								

Item	Page	Revision (See Manual for Details)
16.5.6 Timing of rizeing TE bit and TEND interrupt request	531	Newly added

17.5.1 Frequency Control Register A (FRQCRA)	541	Table amended
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Bit	Bit Name	Initial Value	R/W	Description
23 to 20	IFC[3:0]	See table 17.2.	R/W	CPU Clock (I ϕ) Frequency Division Ratio
				0000: $\times 1/2$ 1000: $\times 1/24$
				0001: $\times 1/3$ 1001: $\times 1/32$
				0010: $\times 1/4$ 1010: $\times 1/36$
				0011: $\times 1/6$ 1011: $\times 1/48$
				0100: $\times 1/8$ 1101: $\times 1/72$
				0101: $\times 1/12$ Other settings are prohibited
				0110: $\times 1/16$
15 to 12	SFC[3:0]	See table 17.2.	R/W	S Clock (S ϕ) Frequency Division Ratio
				0010: $\times 1/4$ 1000: $\times 1/24$
				0011: $\times 1/6$ 1001: $\times 1/32$
				0100: $\times 1/8$ 1010: $\times 1/36$
				0101: $\times 1/12$ 1011: $\times 1/48$
				0110: $\times 1/16$ 1101: $\times 1/72$
				Other settings are prohibited

17.5.2 Frequency Control Register B (FRQCRB)	543	Description added
--	-----	-------------------

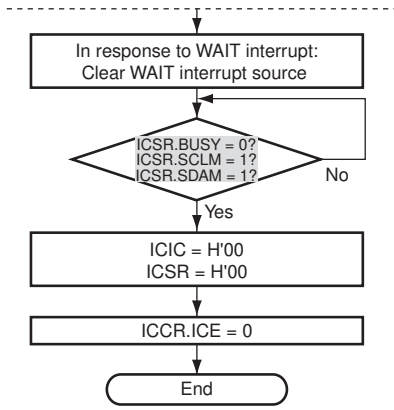
5. S ϕ : M1 ϕ ; B ϕ
Integer clock ratio S ϕ : M1 ϕ •B ϕ = 2 : 1 : 1, 2 : 2 : 1, 1
If 2DG is used, the following clock frequency ratio must also be satisfied.
S ϕ : B ϕ : P ϕ = 4 : 2 : 1

31.5.1 System Control (1) Power Control Procedures	1104	Description amended
--	------	---------------------

— After using USB0, set bit10, 9 to 0 before USB0 Power OFF.
When USB is not used, USB power pins are open, UPONCR register value should be initial vlue. When USB power pins are supplied, either USB is used or not, UPON[1:0] bits should be set to 11.

32.4.8 Wait Operation	1204	Figure amended
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Figure 32.16 Example Flow of Software for Transmission with Use of Wait Interrupt

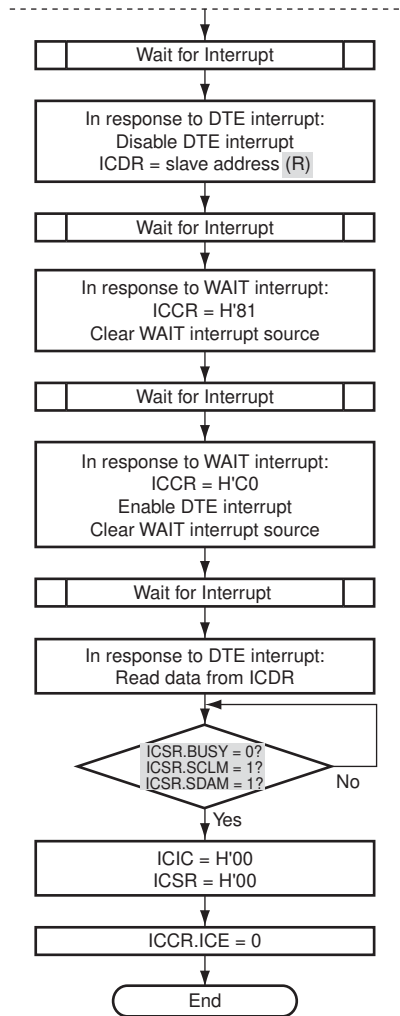


32.4.8 Wait Operation

1205

Figure title and Figure amended

Figure 32.17 Example Flow of Software for 1-Byte Read with Use of Wait Interrupt



Item	Page	Revision (See Manual for Details)
32.4.8 Wait Operation Figure 32.18 Example Flow of Software for n-Byte Write/Read with Use of Wait Interrupt	1206	Figure amended
<pre> graph TD Start(()) --> Decision{ICSR.BUSY = 0? ICSR.SCLM = 1? ICSR.SDAM = 1?} Decision -- No --> Start Decision -- Yes --> Process1[ICIC = H'00 ICSR = H'00] Process1 --> Process2[ICCR.ICE = 0] Process2 --> End([End]) </pre>		
Figure 32.19 Example Flow of Software for Transmission (WAIT = 0)	1207	Figure amended
<pre> graph TD Start(()) --> Decision{ICSR.BUSY = 0? ICSR.SCLM = 1? ICSR.SDAM = 1?} Decision -- No --> Start Decision -- Yes --> Process1[ICIC = H'00 ICSR = H'00] Process1 --> Process2[ICCR.ICE = 0] Process2 --> End([END]) </pre>		
35.2 Functional Overview of VEU Figure 35.1 Block Diagram of VEU	1447	Figure amended
Section38 2D Graphic Accelerator (2DG)	1687	Description added Note: If 2DG is used, Clock frequency ratio must be set as following, $S\phi : B\phi : P\phi = 4 : 2 : 1$

38.3.1 System Control Registers 1811 Table amended

(1) System Control Register (SCLR)

Bit	Bit Name	Abbrev.	Initial Value	Description
31	Software Reset	SRES	1	Resets the 2DG. 0: Command processing execution is enabled. 1: Reset state This bit is set to 1 when a hardware reset is performed. Clear this bit to 0 in initialization. When this bit is set to 1 by software, a reset is performed for drawing operations only. The 2DG registers are also initialized. While this bit is set to 1, this is the only register that can be written to. Note: After a software reset is executed during the drawing period (from rendering start to TRAP command execution), execute the following process in order to cancel the software reset. (1) Set SRES to 1. (2) Wait 1 vsync. (3) Set HRES to 1 (for at least 4 CLKP cycles). (4) Clear HRES to 0. (5) Clear SRES to 0.
30		HRES	0	Resets the 2DG (hardware reset). This bit must be used only to cancel the software reset, is prohibited to use during 2DG is active.

39.4.1 LCDC Display Features 1898 Description amended

- Display Resolution
Up to WXGA and HD (1280 × 720) supported.

39.6 Examples of Clock and LCD Data Signals 1912 Figure Replaced

Figure 39.15 Example of Clock and LCD Data Signals (3)

40.3.8 VOU Display Size Register (VOUDSR) 1931 Table amended

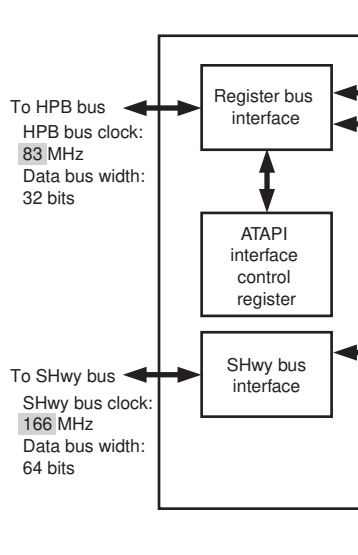
Bit	Bit Name	Initial Value	R/W	Description
25 to 17	HDS[8:1]	H'2D0	R/W	Horizontal Image Size These bits specify the horizontal image size. Use these bits to adjust the display. The VOU outputs data for the size specified by these bits. Note that since the horizontal image size is limited to 2n, the lowest bit must be cleared to 0. The initial value is 720. These bits (VOUDSR.HDS) should be set according to the following restriction. Display Size (VOUDSR.HDS) ≥ Display Position (VOUDPR.HP) + Source Image Size (VOUISR.HSZ)
8 to 0	VDS[8:0]	H'0F0	R/W	Vertical Image Size These bits specify the vertical image size. The VOU outputs lines for the size specified by these bits. The initial value is 240. These bits (VOUDSR.VDS) should be set according to the following restriction. Display Size (VOUDSR.VDS) ≥ Display Position (VOUDPR.VP) + Source Image Size (VOUISR.VSZ)

Item	Page	Revision (See Manual for Details)															
40.3.9 VOU Valid Pixel Start Position Register (VOUVPR)	1932	Table amended															
<table border="1"> <thead> <tr> <th>Bit</th> <th>Bit Name</th> <th>Initial Value</th> <th>R/W</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>23 to 17</td> <td>HVP[7:1]</td> <td>H'78</td> <td>R/W</td> <td>Horizontal Valid Pixel Start Position</td> </tr> <tr> <td>16</td> <td>HVP[0]</td> <td></td> <td>R</td> <td>These bits specify the horizontal position where output data becomes valid in pixel clock cycles. The sum of the setting of these bits and the setting of the HDS[9:0] bits in VOUDSR should be 858 or less (for NTSC), or 864 or less (for PAL) in case of BT.601, 856 or less (for NTSC) in case of BT.656. Note that since the horizontal valid pixel start position is limited to 2n, the lowest bit must be cleared to 0. The initial value is 120. Note: When scaling up the horizontal size of the image, the HVP bit in VOUVPR the HP bit in VOUDPR should be more than 9.</td> </tr> </tbody> </table>			Bit	Bit Name	Initial Value	R/W	Description	23 to 17	HVP[7:1]	H'78	R/W	Horizontal Valid Pixel Start Position	16	HVP[0]		R	These bits specify the horizontal position where output data becomes valid in pixel clock cycles. The sum of the setting of these bits and the setting of the HDS[9:0] bits in VOUDSR should be 858 or less (for NTSC), or 864 or less (for PAL) in case of BT.601, 856 or less (for NTSC) in case of BT.656. Note that since the horizontal valid pixel start position is limited to 2n, the lowest bit must be cleared to 0. The initial value is 120. Note: When scaling up the horizontal size of the image, the HVP bit in VOUVPR the HP bit in VOUDPR should be more than 9.
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23 to 17	HVP[7:1]	H'78	R/W	Horizontal Valid Pixel Start Position													
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40.3.12 VOU Mode Setting Register (VOUMSR)	1937	Table amended															
<table border="1"> <thead> <tr> <th>Bit</th> <th>Bit Name</th> <th>Initial Value</th> <th>R/W</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31</td> <td>LMD</td> <td>0</td> <td>R/W</td> <td>LCDC Compatible Mode Specifies the VOU mode as LCDC compatible mode. LCDC compatible mode should be used with a 24.5454-MHz input clock. The HDS bit in VOUDSR should be set to 640. 0: Normal operating mode 1: LCDC compatible mode</td> </tr> </tbody> </table>			Bit	Bit Name	Initial Value	R/W	Description	31	LMD	0	R/W	LCDC Compatible Mode Specifies the VOU mode as LCDC compatible mode. LCDC compatible mode should be used with a 24.5454-MHz input clock. The HDS bit in VOUDSR should be set to 640. 0: Normal operating mode 1: LCDC compatible mode					
Bit	Bit Name	Initial Value	R/W	Description													
31	LMD	0	R/W	LCDC Compatible Mode Specifies the VOU mode as LCDC compatible mode. LCDC compatible mode should be used with a 24.5454-MHz input clock. The HDS bit in VOUDSR should be set to 640. 0: Normal operating mode 1: LCDC compatible mode													
41.2.1 ICBnn Control Register (MEnnCTRL)	1961	Table amended															
<table border="1"> <thead> <tr> <th>Bit</th> <th>Bit Name</th> <th>Initial Value</th> <th>R/W</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>24 to 16</td> <td>MSAR[8:0]</td> <td>H'000</td> <td>R/W</td> <td>Specify the start address of a memory area reserved in the MERAM in units of Kbytes (0 to 127). Set a multiple of the number calculated by rounding up (MEnnBSIZE.XSZM1[15:0] + 1) into units of 2^n Kbytes (units of 1 Kbyte are also included).</td> </tr> </tbody> </table>			Bit	Bit Name	Initial Value	R/W	Description	24 to 16	MSAR[8:0]	H'000	R/W	Specify the start address of a memory area reserved in the MERAM in units of Kbytes (0 to 127). Set a multiple of the number calculated by rounding up (MEnnBSIZE.XSZM1[15:0] + 1) into units of 2^n Kbytes (units of 1 Kbyte are also included).					
Bit	Bit Name	Initial Value	R/W	Description													
24 to 16	MSAR[8:0]	H'000	R/W	Specify the start address of a memory area reserved in the MERAM in units of Kbytes (0 to 127). Set a multiple of the number calculated by rounding up (MEnnBSIZE.XSZM1[15:0] + 1) into units of 2^n Kbytes (units of 1 Kbyte are also included).													
41.3.4 Additional Remarks on Line Numbers and Offset Addresses (2) Adjusting Stride Length of Image Modules to Values in External Memory	1992	Description amended															
<ul style="list-style-type: none"> Specify the number of buffer lines to be allocated in the BNM bits in MEnnMCNF in 1-Kbyte units. Set the values calculated as follows in the KRBNM bits in MEnnMCNF and the KWBNM bits in MEnnMCNF. Use n as the desired number of lines to be retained for each IP that is described in section 41.5, Settings for Each Associated Module. 																	
41.5.5 Image Output of VPU (2) Conditions for the Number of Lines Retained	2006	Description amended															
<ul style="list-style-type: none"> Buffer corresponding to VP4_DWY_ADDR in the VPU: Equal to or larger than 20 Buffer corresponding to VP4_DWC_ADDR in the VPU: Equal to or larger than 12 																	
42.1 Features Figure 42.1 Block Diagram of 2D-DMAC	2014	Figure Replaced															
42.5.1 Restriction on horizontal size of extracted image	2043	Newly added															

Item **Page** **Revision (See Manual for Details)**

46.4 Block Diagram 2243 Figure amended

Figure 46.1 ATAPI Block Diagram



50.4.2 H-UDI Reset 2528 Description amended

A system reset is generated by the SDIR command. After the H-UDI reset assert command has been sent from the H-UDI pin, sending the H-UDI reset negate command resets the CPU (see Figure 50.3). The required time between the H-UDI reset assert and H-UDI reset negate commands is the same as the time for holding the reset pin low in order to reset this LSI by a system reset.

51.1 Register Addresses 2528 Table amended

Register Name	Abbreviation	R/W	Address	Module	Access Size
PRI control register 4(ICB)	PRPRICR 4	R/W	HFF80 0048	Super	32
PRI control register 5	Reserved	R/W	HFF80 0050	Hyway	32

2533 Table amended

Register Name	Abbreviation	R/W	Address	Module	Access Size
DBSC SDRAM kind select register	DBKIND	R/W	HFD00 0008	DBSC	32
DBSC status register	DBSTATE	R	HFD00 000C		32

Item	Page	Revision (See Manual for Details)
52.2 Recommended Operating Conditions	2614	Table deleted
Table 52.2 Recommended Operating Conditions		

Item	Symbol	Min.	Typ.	Max.	Unit	Product number
Power supply voltage	Core power supply V_{CC}	1.15	—	1.35	V	$M1\phi \leq 125$ MHz
		1.25	—	1.35	V	$M1\phi \leq 166$ MHz
	Power supply for PLL V_{CC_PLL}	1.15	—	1.35	V	$M1\phi \leq 125$ MHz
		1.25	—	1.35	V	$M1\phi \leq 166$ MHz
	Power supply for FLL V_{CC_FLL}	1.15	—	1.35	V	$M1\phi \leq 125$ MHz
		1.25	—	1.35	V	$M1\phi \leq 166$ MHz
	Power supply for DDR V_{CC_DDR}	1.7	1.8	1.9	V	

52.3.1 Power-on Order	2616	Description amended
		<ul style="list-style-type: none"> When any of the clock modes 3 to 7 is in use, RTC_CLK supply is required. Input RTC_CLK before turning on the 1.2-V power supplies, after turning on the VCCQ power supply.

Table 52.3 Recommended Timing in Power-On	2617	Table added

Item	Symbol	Time	Unit
V_{CCQ} power settling time	trV_{CCQ}	≤ 300	μ s
Settling time difference between V_{CC} power supplies	tdV_{CCQ}	≥ 0	ms
Time difference between 3.3-V V_{DD} and 1.2-V V_{DD} at power-on	t_{PMU}	0 to 10	ms
V_{DD} power settling time	trV_{DD}	≤ 1	ms
Time over which the state is undefined	t_{UNC}	$t_{PMU} + trV_{DD} + 3TRCLK^2$	ms
I/O power supplies other than V_{CCQ} Setting Time	trV_{IO}	≤ 1	ms

52.5.5 DBSC Bus Timing	2648	Table deleted
Table 52.12 DDR2-SDRAM Interface Timing		

Item	Symbol	Min.	Max.	Unit	Reference
CK cycle	t_{CK}	6.0	8	ns	Figure 52.25
CK high period	t_{CH} (abs)	0.45	0.55	t_{CK}	
CK low period	t_{CL} (abs)	0.45	0.55	t_{CK}	

Figure 52.32 Relation between DQS and DQ/DQM Output Waveforms (Write)	2653	Figure amended

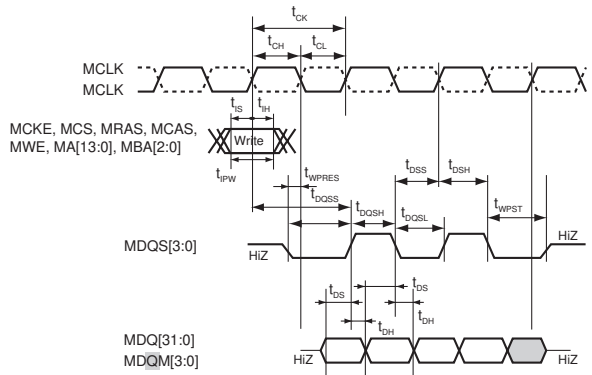
MDQS[1:0] (Solid line)

MDQS[1:0]# (Broken line)

MDQ[15:0]

MDQM[1:0]

Figure 52.34 Mobile-DDR-SDRAM Output Timing (Write)



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