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SH7780

Hardware Manual

Renesas 32-Bit RISC Microcomputer
SuperH™ RISC Engine Family
SH7780 Series

R8A77800A

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General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.

The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.

Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.

The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.

The undefined or reserved addresses may be used to expand functions, or test registers may have been allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

5. Reading from/Writing Reserved Bit of Each Register

Note: Treat the reserved bit of register used in each module as follows except in cases where the specifications for values which are read from or written to the bit are provided in the description.

The bit is always read as 0. The write value should be 0 or one, which has been read immediately before writing.

Writing the value, which has been read immediately before writing has the advantage of preventing the bit from being affected on its extended function when the function is assigned.

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules
 - CPU and System-Control Modules
 - On-Chip Modules

The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

 - i) Feature
 - ii) Input/Output Pin
 - iii) Register Description
 - iv) Operation
 - v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. Electrical Characteristics
8. Appendix
9. Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

10. Index

Preface

This LSI is a RISC (Reduced Instruction Set Computer) microcomputer which includes a Renesas Technology-original RISC CPU as its core, and the peripheral functions required to configure a system.

Target Users: This manual was written for users who will be using this LSI in the design of application systems. Users of this manual are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of this LSI to the above users.

Notes on reading this manual:

- In order to understand the overall functions of the chip
Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.

Rules:

| | |
|------------------|---|
| Bit order: | The MSB is on the left and the LSB is on the right. |
| Number notation: | Binary is B'xxxx, hexadecimal is H'xxxx, decimal is xxxx. |
| Signal notation: | An overbar is added to a low-active signal: $\overline{\text{xxx}}$ |

Abbreviations

| | |
|-------|-------------------------------------|
| ALU | Arithmetic Logic Unit |
| ASID | Address Space Identifier |
| BGA | Ball Grid Array |
| CMT | Compare Match Timer (Timer/Counter) |
| CPG | Clock Pulse Generator |
| CPU | Central Processing Unit |
| DDR | Double Data Rate |
| DDRIF | DDR-SDRAM Interface |
| DMA | Direct Memory Access |
| DMAC | Direct Memory Access Controller |
| FIFO | First-In First-Out |
| FLCTL | NAND Flash Memory Controller |
| FPU | Floating-point Unit |
| HAC | Audio Codec |
| HSPI | Serial Protocol Interface |
| H-UDI | User Debugging Interface |
| INTC | Interrupt Controller |
| JTAG | Joint Test Action Group |
| LBSC | Local Bus State Controller |
| LRAM | L Memory |
| LRU | Least Recently Used |
| LSB | Least Significant Bit |

| | |
|-------|---|
| MMCIF | Multimedia Card Interface |
| MMU | Memory Management Unit |
| MSB | Most Significant Bit |
| PC | Program Counter |
| PCI | Peripheral Component Interconnect |
| PCIC | PCI (local bus) Controller |
| RISC | Reduced Instruction Set Computer |
| RTC | Realtime Clock |
| SCIF | Serial Communication Interface with FIFO |
| SIOF | Serial Interface with FIFO |
| SSI | Serial Sound Interface |
| TAP | Test Access Port |
| TLB | Translation Lookaside Buffer |
| TMU | Timer Unit |
| UART | Universal Asynchronous Receiver/Transmitter |
| UBC | User Break Controller |
| WDT | Watchdog Timer |

Contents

| | |
|---|----|
| Section 1 Overview | 1 |
| 1.1 SH7780 Features | 1 |
| 1.2 Block Diagram | 9 |
| 1.3 Pin Arrangement | 10 |
| 1.4 Pin Functions | 11 |
| 1.5 Memory Address Map | 27 |
| 1.6 SuperHyway Bus | 30 |
| 1.7 SuperHyway Memory (SuperHyway RAM)..... | 31 |
| Section 2 Programming Model | 33 |
| 2.1 Data Formats | 33 |
| 2.2 Register Descriptions | 34 |
| 2.2.1 Privileged Mode and Banks | 34 |
| 2.2.2 General Registers | 37 |
| 2.2.3 Floating-Point Registers..... | 38 |
| 2.2.4 Control Registers | 40 |
| 2.2.5 System Registers | 42 |
| 2.3 Memory-Mapped Registers..... | 46 |
| 2.4 Data Formats in Registers | 47 |
| 2.5 Data Formats in Memory | 48 |
| 2.6 Processing States..... | 49 |
| 2.7 Usage Note..... | 50 |
| 2.7.1 Notes on self-modified codes..... | 50 |
| Section 3 Instruction Set | 51 |
| 3.1 Execution Environment | 51 |
| 3.2 Addressing Modes | 53 |
| 3.3 Instruction Set | 57 |
| Section 4 Pipelining | 73 |
| 4.1 Pipelines..... | 73 |
| 4.2 Parallel-Executability | 84 |
| 4.3 Issue Rates and Execution Cycles..... | 87 |
| Section 5 Exception Handling | 97 |
| 5.1 Summary of Exception Handling..... | 97 |

| | | |
|--|--|-----|
| 5.2 | Register Descriptions | 97 |
| 5.2.1 | TRAPA Exception Register (TRA) | 98 |
| 5.2.2 | Exception Event Register (EXPEVT)..... | 99 |
| 5.2.3 | Interrupt Event Register (INTEVT)..... | 100 |
| 5.3 | Exception Handling Functions..... | 101 |
| 5.3.1 | Exception Handling Flow | 101 |
| 5.3.2 | Exception Handling Vector Addresses | 101 |
| 5.4 | Exception Types and Priorities | 102 |
| 5.5 | Exception Flow | 104 |
| 5.5.1 | Exception Flow | 104 |
| 5.5.2 | Exception Source Acceptance..... | 106 |
| 5.5.3 | Exception Requests and BL Bit | 107 |
| 5.5.4 | Return from Exception Handling..... | 107 |
| 5.6 | Description of Exceptions..... | 108 |
| 5.6.1 | Resets | 108 |
| 5.6.2 | General Exceptions | 110 |
| 5.6.3 | Interrupts..... | 124 |
| 5.6.4 | Priority Order with Multiple Exceptions | 125 |
| 5.7 | Usage Notes | 127 |
| Section 6 Floating-Point Unit (FPU)..... | | 129 |
| 6.1 | Features..... | 129 |
| 6.2 | Data Formats..... | 130 |
| 6.2.1 | Floating-Point Format..... | 130 |
| 6.2.2 | Non-Numbers (NaN) | 133 |
| 6.2.3 | Denormalized Numbers | 134 |
| 6.3 | Register Descriptions | 135 |
| 6.3.1 | Floating-Point Registers | 135 |
| 6.3.2 | Floating-Point Status/Control Register (FPSCR) | 137 |
| 6.3.3 | Floating-Point Communication Register (FPUL) | 140 |
| 6.4 | Rounding..... | 141 |
| 6.5 | Floating-Point Exceptions..... | 142 |
| 6.5.1 | General FPU Disable Exceptions and Slot FPU Disable Exceptions | 142 |
| 6.5.2 | FPU Exception Sources | 142 |
| 6.5.3 | FPU Exception Handling | 142 |
| 6.6 | Graphics Support Functions..... | 144 |
| 6.6.1 | Geometric Operation Instructions..... | 144 |
| 6.6.2 | Pair Single-Precision Data Transfer..... | 145 |

| | | |
|-----------|---|-----|
| Section 7 | Memory Management Unit (MMU) | 147 |
| 7.1 | Overview of MMU | 147 |
| 7.1.1 | Address Spaces | 149 |
| 7.2 | Register Descriptions | 156 |
| 7.2.1 | Page Table Entry High Register (PTEH) | 157 |
| 7.2.2 | Page Table Entry Low Register (PTEL) | 158 |
| 7.2.3 | Translation Table Base Register (TTB) | 159 |
| 7.2.4 | TLB Exception Address Register (TEA) | 159 |
| 7.2.5 | MMU Control Register (MMUCR) | 160 |
| 7.2.6 | Physical Address Space Control Register (PASCRCR) | 164 |
| 7.2.7 | Instruction Re-Fetch Inhibit Control Register (IRMCR) | 165 |
| 7.3 | TLB Functions | 167 |
| 7.3.1 | Unified TLB (UTLB) Configuration | 167 |
| 7.3.2 | Instruction TLB (ITLB) Configuration | 170 |
| 7.3.3 | Address Translation Method | 171 |
| 7.4 | MMU Functions | 173 |
| 7.4.1 | MMU Hardware Management | 173 |
| 7.4.2 | MMU Software Management | 173 |
| 7.4.3 | MMU Instruction (LDTLB) | 174 |
| 7.4.4 | Hardware ITLB Miss Handling | 175 |
| 7.4.5 | Avoiding Synonym Problems | 176 |
| 7.5 | MMU Exceptions | 177 |
| 7.5.1 | Instruction TLB Multiple Hit Exception | 177 |
| 7.5.2 | Instruction TLB Miss Exception | 178 |
| 7.5.3 | Instruction TLB Protection Violation Exception | 179 |
| 7.5.4 | Data TLB Multiple Hit Exception | 180 |
| 7.5.5 | Data TLB Miss Exception | 180 |
| 7.5.6 | Data TLB Protection Violation Exception | 181 |
| 7.5.7 | Initial Page Write Exception | 182 |
| 7.6 | Memory-Mapped TLB Configuration | 183 |
| 7.6.1 | ITLB Address Array | 184 |
| 7.6.2 | ITLB Data Array | 185 |
| 7.6.3 | UTLB Address Array | 186 |
| 7.6.4 | UTLB Data Array | 187 |
| 7.7 | 32-Bit Address Extended Mode | 188 |
| 7.7.1 | Overview of 32-Bit Address Extended Mode | 189 |
| 7.7.2 | Transition to 32-Bit Address Extended Mode | 189 |
| 7.7.3 | Privileged Space Mapping Buffer (PMB) Configuration | 189 |
| 7.7.4 | PMB Function | 191 |

| | | |
|--------------------------------|--|------------|
| 7.7.5 | Memory-Mapped PMB Configuration..... | 192 |
| 7.7.6 | Notes on Using 32-Bit Address Extended Mode..... | 194 |
| Section 8 Caches..... | | 197 |
| 8.1 | Features..... | 197 |
| 8.2 | Register Descriptions..... | 200 |
| 8.2.1 | Cache Control Register (CCR)..... | 201 |
| 8.2.2 | Queue Address Control Register 0 (QACR0)..... | 203 |
| 8.2.3 | Queue Address Control Register 1 (QACR1)..... | 204 |
| 8.2.4 | On-Chip Memory Control Register (RAMCR)..... | 205 |
| 8.3 | Operand Cache Operation..... | 207 |
| 8.3.1 | Read Operation..... | 207 |
| 8.3.2 | Prefetch Operation..... | 208 |
| 8.3.3 | Write Operation..... | 209 |
| 8.3.4 | Write-Back Buffer..... | 211 |
| 8.3.5 | Write-Through Buffer..... | 211 |
| 8.3.6 | OC Two-Way Mode..... | 211 |
| 8.4 | Instruction Cache Operation..... | 212 |
| 8.4.1 | Read Operation..... | 212 |
| 8.4.2 | Prefetch Operation..... | 213 |
| 8.4.3 | IC Two-Way Mode..... | 213 |
| 8.5 | Cache Operation Instruction..... | 214 |
| 8.5.1 | Coherency between Cache and External Memory..... | 214 |
| 8.5.2 | Prefetch Operation..... | 215 |
| 8.6 | Memory-Mapped Cache Configuration..... | 216 |
| 8.6.1 | IC Address Array..... | 217 |
| 8.6.2 | IC Data Array..... | 219 |
| 8.6.3 | OC Address Array..... | 220 |
| 8.6.4 | OC Data Array..... | 222 |
| 8.7 | Store Queues..... | 223 |
| 8.7.1 | SQ Configuration..... | 223 |
| 8.7.2 | Writing to SQ..... | 223 |
| 8.7.3 | Transfer to External Memory..... | 224 |
| 8.7.4 | Determination of SQ Access Exception..... | 225 |
| 8.7.5 | Reading from SQ..... | 225 |
| 8.8 | Notes on Using 32-Bit Address Extended Mode..... | 226 |
| Section 9 L Memory..... | | 227 |
| 9.1 | Features..... | 227 |
| 9.2 | Register Descriptions..... | 228 |

| | | |
|---|--|------------|
| 9.2.1 | On-Chip Memory Control Register (RAMCR) | 229 |
| 9.2.2 | L Memory Transfer Source Address Register 0 (LSA0) | 230 |
| 9.2.3 | L Memory Transfer Source Address Register 1 (LSA1) | 232 |
| 9.2.4 | L Memory Transfer Destination Address Register 0 (LDA0) | 234 |
| 9.2.5 | L Memory Transfer Destination Address Register 1 (LDA1) | 236 |
| 9.3 | Operation | 238 |
| 9.3.1 | Access from the CPU and FPU | 238 |
| 9.3.2 | Access from the SuperHyway Bus Master Module | 238 |
| 9.3.3 | Block Transfer | 238 |
| 9.4 | L Memory Protective Functions | 240 |
| 9.5 | Usage Notes | 241 |
| 9.5.1 | Page Conflict | 241 |
| 9.5.2 | L Memory Coherency | 241 |
| 9.5.3 | Sleep Mode | 241 |
| 9.6 | Note on Using 32-Bit Address Extended Mode | 241 |
| Section 10 Interrupt Controller (INTC) | | 243 |
| 10.1 | Features | 243 |
| 10.1.1 | Interrupt Method | 245 |
| 10.1.2 | Interrupt Types in INTC | 246 |
| 10.2 | Input/Output Pins | 250 |
| 10.3 | Register Descriptions | 251 |
| 10.3.1 | Interrupt Control Register 0 (ICR0) | 255 |
| 10.3.2 | Interrupt Control Register 1 (ICR1) | 258 |
| 10.3.3 | Interrupt Priority Register (INTPRI) | 259 |
| 10.3.4 | Interrupt Source Register (INTREQ) | 260 |
| 10.3.5 | Interrupt Mask Registers (INTMSK0 to INTMSK2) | 261 |
| 10.3.6 | Interrupt Mask Clear Registers (INTMSKCLR0 to INTMSKCLR2) | 266 |
| 10.3.7 | NMI Flag Control Register (NMIFCR) | 271 |
| 10.3.8 | User Interrupt Mask Level Register (USERIMASK) | 273 |
| 10.3.9 | On-chip Module Interrupt Priority Registers (INT2PRI0 to INT2PRI7) | 276 |
| 10.3.10 | Interrupt Source Register (INT2A0: Not affected by Mask States) | 277 |
| 10.3.11 | Interrupt Source Register (INT2A1: Affected by Mask States) | 280 |
| 10.3.12 | Interrupt Mask Register (INT2MSKR) | 282 |
| 10.3.13 | Interrupt Mask Clear Register (INT2MSKCR) | 285 |
| 10.3.14 | On-chip Module Interrupt Source Registers (INT2B0 to INT2B7) | 287 |
| 10.3.15 | GPIO Interrupt Set Register (INT2GPIC) | 294 |
| 10.4 | Interrupt Sources | 296 |
| 10.4.1 | NMI Interrupt | 296 |
| 10.4.2 | IRQ Interrupts | 296 |

| | | |
|--|---|------------|
| 10.4.3 | IRL Interrupts | 297 |
| 10.4.4 | On-chip Module Interrupts | 299 |
| 10.4.5 | Interrupt Priority Levels of On-chip Module Interrupts | 300 |
| 10.4.6 | Interrupt Exception Handling and Priority..... | 301 |
| 10.5 | Operation | 308 |
| 10.5.1 | Interrupt Sequence | 308 |
| 10.5.2 | Multiple Interrupts | 310 |
| 10.5.3 | Interrupt Masking by MAI Bit..... | 310 |
| 10.6 | Interrupt Response Time..... | 311 |
| 10.7 | Usage Notes | 312 |
| 10.7.1 | To Clear Interrupt Request When Holding Function Selected | 312 |
| 10.7.2 | Notes on Setting IRQ/IRL[7:0] Pin Function | 313 |
| 10.7.3 | To clear IRQ and IRL interrupt requests | 313 |
| Section 11 Local Bus State Controller (LBSC)..... | | 315 |
| 11.1 | Features..... | 315 |
| 11.2 | Input/Output Pins | 318 |
| 11.3 | Area Overview | 320 |
| 11.3.1 | Space Divisions | 320 |
| 11.3.2 | Memory Bus Width | 324 |
| 11.3.3 | Data Alignment..... | 325 |
| 11.3.4 | PCMCIA Support | 325 |
| 11.4 | Register Descriptions..... | 329 |
| 11.4.1 | Memory Address Map Select Register (MMSELR)..... | 331 |
| 11.4.2 | Bus Control Register (BCR)..... | 333 |
| 11.4.3 | CSn Bus Control Register (CSnBCR) | 336 |
| 11.4.4 | CSn Wait Control Register (CSnWCR)..... | 342 |
| 11.4.5 | CSn PCMCIA Control Register (CSnPCR)..... | 347 |
| 11.5 | Operation | 352 |
| 11.5.1 | Endian/Access Size and Data Alignment..... | 352 |
| 11.5.2 | Areas..... | 357 |
| 11.5.3 | SRAM interface | 361 |
| 11.5.4 | Burst ROM (Clock Asynchronous) Interface | 370 |
| 11.5.5 | PCMCIA Interface..... | 372 |
| 11.5.6 | MPX Interface | 383 |
| 11.5.7 | Byte Control SRAM Interface | 389 |
| 11.5.8 | Wait Cycles between Accesses | 393 |
| 11.5.9 | Bus Arbitration | 395 |
| 11.5.10 | Bus Release and Acquire Sequence | 397 |
| 11.5.11 | Cooperation between Master and Slave..... | 399 |

| | | |
|------------|---|-----|
| Section 12 | DDR-SDRAM Interface (DDRIF) | 401 |
| 12.1 | Features | 401 |
| 12.2 | Input/Output Pins | 403 |
| 12.3 | Address Space, Bus Width, and Data Alignment | 404 |
| 12.3.1 | Address Space of the DDRIF | 404 |
| 12.3.2 | Memory Data Bus Width | 405 |
| 12.3.3 | Data Alignment | 406 |
| 12.4 | Register Descriptions | 410 |
| 12.4.1 | Memory Interface Mode Register (MIM) | 412 |
| 12.4.2 | SDRAM Control Register (SCR) | 416 |
| 12.4.3 | SDRAM Timing Register (STR) | 418 |
| 12.4.4 | SDRAM Row Attribute Register (SDR) | 421 |
| 12.4.5 | SDRAM Mode Register (SDMR) | 422 |
| 12.4.6 | DDR-SDRAM Back-up Register (DBK) | 424 |
| 12.5 | Operation | 425 |
| 12.5.1 | DDR-SDRAM Access | 425 |
| 12.5.2 | DDR-SDRAM Initialization Sequence | 425 |
| 12.5.3 | Supported SDRAM Commands | 426 |
| 12.5.4 | SDRAM Access Mode | 427 |
| 12.5.5 | Power-Down Modes | 427 |
| 12.5.6 | Address Multiplexing | 429 |
| 12.6 | DDR-SDRAM Basic Timing | 430 |
| 12.7 | Usage Notes | 440 |
| 12.7.1 | Operating Frequency | 440 |
| 12.7.2 | Stopping Clock | 440 |
| 12.7.3 | Using SCR to Issue REFA Command (Outside the Initialization Sequence) | 440 |
| 12.7.4 | Timing of Connected SDRAM | 440 |
| 12.7.5 | Setting Auto-Refresh Interval | 441 |
| Section 13 | PCI Controller (PCIC) | 443 |
| 13.1 | Features | 443 |
| 13.2 | Input/Output Pins | 446 |
| 13.3 | Register Descriptions | 449 |
| 13.3.1 | PCIC Enable Control Register (PCIECR) | 455 |
| 13.3.2 | Configuration Registers | 456 |
| 13.3.3 | Local Register | 481 |
| 13.4 | Operation | 522 |
| 13.4.1 | Supported PCI Commands | 522 |
| 13.4.2 | PCIC Initialization | 523 |
| 13.4.3 | Master Access | 524 |

| | | |
|---|--|------------|
| 13.4.4 | Target Access..... | 532 |
| 13.4.5 | Host Bus Bridge Mode | 541 |
| 13.4.6 | Normal mode | 544 |
| 13.4.7 | Power Management | 544 |
| 13.4.8 | PCI Local Bus Basic Interface..... | 545 |
| Section 14 Direct Memory Access Controller (DMAC)..... | | 557 |
| 14.1 | Features..... | 557 |
| 14.2 | Input/Output Pins..... | 559 |
| 14.3 | Register Descriptions..... | 561 |
| 14.3.1 | DMA Source Address Registers 0 to 11 (SAR0 to SAR11)..... | 567 |
| 14.3.2 | DMA Source Address Registers B0 to B3, B6 to B9 (SARB0 to SARB3, SARB6 to SARB9)..... | 568 |
| 14.3.3 | DMA Destination Address Registers 0 to 11 (DAR0 to DAR11) | 568 |
| 14.3.4 | DMA Destination Address Registers B0 to B3, B6 to B9 (DARB0 to DARB3, DARB6 to DARB9) | 569 |
| 14.3.5 | DMA Transfer Count Registers 0 to 11 (TCR0 to TCR11)..... | 570 |
| 14.3.6 | DMA Transfer Count Registers B0 to B3, B6 to B9 (TCRB0 to TCRB3, TCRB6 to TCRB9)..... | 571 |
| 14.3.7 | DMA Channel Control Registers 0 to 11 (CHCR0 to CHCR11) | 572 |
| 14.3.8 | DMA Operation Register 0, 1 (DMAOR0 and DMAOR1)..... | 581 |
| 14.3.9 | DMA Extended Resource Selectors (DMARS0 to DMARS2)..... | 584 |
| 14.4 | Operation | 588 |
| 14.4.1 | DMA Transfer Requests | 588 |
| 14.4.2 | Channel Priority..... | 592 |
| 14.4.3 | DMA Transfer Types..... | 595 |
| 14.4.4 | DMA Transfer Flow | 602 |
| 14.4.5 | Repeat Mode Transfer | 604 |
| 14.4.6 | Reload Mode Transfer | 605 |
| 14.4.7 | DREQ Pin Sampling Timing | 606 |
| 14.5 | Usage Notes | 608 |
| 14.5.1 | Module Stop | 608 |
| 14.5.2 | Address Error..... | 608 |
| 14.5.3 | Notes on Burst Mode Transfer..... | 608 |
| 14.5.4 | DACK output division..... | 609 |
| 14.5.5 | Clear DMINT Interrupt..... | 609 |
| 14.5.6 | \overline{CS} Output Settings and Transfer Size Larger than External Bus Width..... | 609 |
| 14.5.7 | DACK Assertion and DREQ Sampling..... | 609 |

| | | |
|------------|---|-----|
| Section 15 | Clock Pulse Generator (CPG) | 613 |
| 15.1 | Features | 613 |
| 15.2 | Input/Output Pins | 616 |
| 15.3 | Clock Operating Modes | 617 |
| 15.4 | Register Descriptions | 618 |
| 15.4.1 | Frequency Control Register (FRQCR) | 619 |
| 15.4.2 | PLL Control Register (PLLCR) | 621 |
| 15.5 | Notes on Board Design | 622 |
| Section 16 | Watchdog Timer and Reset | 625 |
| 16.1 | Features | 625 |
| 16.2 | Input/Output Pins | 627 |
| 16.3 | Register Descriptions | 628 |
| 16.3.1 | Watchdog Timer Stop Time Register (WDTST) | 629 |
| 16.3.2 | Watchdog Timer Control/Status Register (WDTCSR) | 630 |
| 16.3.3 | Watchdog timer Base Stop Time Register (WDTBST) | 631 |
| 16.3.4 | Watchdog Timer Counter (WDCNT) | 632 |
| 16.3.5 | Watchdog Timer Base Counter (WDTBCNT) | 632 |
| 16.4 | Operation | 633 |
| 16.4.1 | Reset request | 633 |
| 16.4.2 | Using watchdog timer mode | 634 |
| 16.4.3 | Using Interval timer mode | 634 |
| 16.4.4 | Time for WDT Overflow | 635 |
| 16.4.5 | Clearing WDT Counter | 636 |
| 16.5 | Status Pin Change Timing during Reset | 636 |
| 16.5.1 | Power-On Reset by PRESET | 636 |
| 16.5.2 | Power-On Reset by Watchdog Timer Overflow | 638 |
| 16.5.3 | Manual Reset by Watchdog Timer Overflow | 640 |
| Section 17 | Power-Down Mode | 643 |
| 17.1 | Features | 643 |
| 17.1.1 | Types of Power-Down Modes | 643 |
| 17.2 | Input/Output Pins | 645 |
| 17.3 | Register Descriptions | 645 |
| 17.3.1 | Standby Control Register (MSTPCR) | 646 |
| 17.4 | Sleep Mode | 648 |
| 17.4.1 | Transition to Sleep mode | 648 |
| 17.4.2 | Cancellation of Sleep Mode | 648 |

| | | |
|---|--|---------|
| 17.5 | Module Standby State..... | 649 |
| 17.5.1 | Transition to Module Standby Mode | 649 |
| 17.5.2 | Cancellation of Module Standby Mode and Resume..... | 649 |
| 17.6 | DDR-SDRAM Power Supply Backup..... | 650 |
| 17.6.1 | Self-Refresh and Initialization | 650 |
| 17.6.2 | DDR-SDRAM Backup Sequence when Turning Off System Power Supply | 651 |
| 17.7 | RTC Power Supply Backup..... | 653 |
| 17.7.1 | Transition to RTC Power Supply Backup..... | 653 |
| 17.7.2 | Cancellation of RTC Power Supply Backup..... | 653 |
| 17.8 | Mode Transitions | 655 |
| 17.9 | STATUS Pin Change Timing | 656 |
| 17.9.1 | In Reset..... | 656 |
| 17.9.2 | In Sleep..... | 656 |
| Section 18 Timer Unit (TMU)..... | | 657 |
| 18.1 | Features..... | 657 |
| 18.2 | Input/Output Pins..... | 659 |
| 18.3 | Register Descriptions..... | 660 |
| 18.3.1 | Timer Output Control Register (TOCR)..... | 662 |
| 18.3.2 | Timer Start Register (TSTR0, TSTR1)..... | 663 |
| 18.3.3 | Timer Constant Register (TCORn) (n = 0 to 5)..... | 665 |
| 18.3.4 | Timer Counter (TCNTn) (n = 0 to 5)..... | 665 |
| 18.3.5 | Timer Control Registers (TCRn) (n = 0 to 5) | 666 |
| 18.3.6 | Input Capture Register 2 (TCPR2) | 668 |
| 18.4 | Operation | 669 |
| 18.4.1 | Counter Operation | 669 |
| 18.4.2 | Input Capture Function | 673 |
| 18.5 | Interrupts..... | 674 |
| 18.6 | Usage Notes..... | 675 |
| 18.6.1 | Register Writes | 675 |
| 18.6.2 | Reading from TCNT..... | 675 |
| 18.6.3 | Reset RTC Frequency Divider Circuit..... | 675 |
| 18.6.4 | External Clock Frequency | 675 |
| Section 19 Compare Match Timer (CMT)..... | | 677 |
| 19.1 | Features..... | 677 |
| 19.2 | Input/Output Pins..... | 679 |
| 19.3 | Register Descriptions..... | 679 |
| 19.3.1 | Configuration Register (CMTCFG)..... | 681 |
| 19.3.2 | Free-Running Timer (CMTFRT)..... | 684 |

| | | |
|---------------------------------------|---|-----|
| 19.3.3 | Control Register (CMTCTL) | 684 |
| 19.3.4 | Interrupt Status Register (CMTIRQS) | 688 |
| 19.3.5 | Channels 0 to 3 Time Registers (CMTCH0T to CMTCH3T)..... | 689 |
| 19.3.6 | Channels 0 to 1 Stop Time Registers (CMTCH0ST to CMTCH1ST)..... | 689 |
| 19.3.7 | Channels 0 to 3 Counters (CMTCH0C to CMTCH3C)..... | 690 |
| 19.4 | Operation | 691 |
| 19.4.1 | Edge Detection..... | 691 |
| 19.4.2 | 32-Bit Timer: Input Capture | 692 |
| 19.4.3 | 32-Bit Timer: Output Compare..... | 693 |
| 19.4.4 | 16-Bit Timer: Input Capture | 697 |
| 19.4.5 | 16-Bit Timer: Output Compare..... | 699 |
| 19.4.6 | Counter: Up-counter | 701 |
| 19.4.7 | Counter: Updown-counter | 703 |
| 19.4.8 | Counter: Rotary Switch Operation of Updown-counter | 705 |
| 19.4.9 | Interrupts..... | 706 |
| Section 20 Realtime Clock (RTC) | | 707 |
| 20.1 | Features..... | 707 |
| 20.1.1 | Block Diagram..... | 708 |
| 20.2 | Input/Output Pins | 709 |
| 20.3 | Register Descriptions | 710 |
| 20.3.1 | 64 Hz Counter (R64CNT)..... | 712 |
| 20.3.2 | Second Counter (RSECCNT) | 712 |
| 20.3.3 | Minute Counter (RMINCNT) | 713 |
| 20.3.4 | Hour Counter (RHRCNT)..... | 713 |
| 20.3.5 | Day-of-Week Counter (RWKCNT)..... | 714 |
| 20.3.6 | Day Counter (RDAYCNT)..... | 715 |
| 20.3.7 | Month Counter (RMONCNT) | 716 |
| 20.3.8 | Year Counter (RYRCNT)..... | 716 |
| 20.3.9 | Second Alarm Register (RSECAR) | 717 |
| 20.3.10 | Minute Alarm Register (RMINAR)..... | 717 |
| 20.3.11 | Hour Alarm Register (RHRAR) | 718 |
| 20.3.12 | Day-of-Week Alarm Register (RWKAR)..... | 718 |
| 20.3.13 | Day Alarm Register (RDAYAR)..... | 719 |
| 20.3.14 | Month Alarm Register (RMONAR) | 720 |
| 20.3.15 | Year-Alarm Register (RYRAR)..... | 720 |
| 20.3.16 | RTC Control Register 1 (RCR1)..... | 721 |
| 20.3.17 | RTC Control Register 2 (RCR2)..... | 723 |
| 20.3.18 | RTC Control Register (RCR3)..... | 726 |

| | | |
|---|---|------------|
| 20.4 | Operation | 727 |
| 20.4.1 | Time Setting Procedures | 727 |
| 20.4.2 | Time Reading Procedures | 728 |
| 20.4.3 | Alarm Function | 729 |
| 20.5 | Interrupts | 730 |
| 20.6 | Usage Notes | 730 |
| 20.6.1 | Register Initialization | 730 |
| 20.6.2 | Crystal Oscillator Circuit | 730 |
| 20.6.3 | Interrupt source and request generating order | 732 |
| Section 21 Serial Communication Interface with FIFO (SCIF) | | 733 |
| 21.1 | Features | 733 |
| 21.2 | Input/Output Pins | 739 |
| 21.3 | Register Descriptions | 740 |
| 21.3.1 | Receive Shift Register (SCRSR) | 742 |
| 21.3.2 | Receive FIFO Data Register (SCFRDR) | 742 |
| 21.3.3 | Transmit Shift Register (SCTSR) | 743 |
| 21.3.4 | Transmit FIFO Data Register (SCFTDR) | 743 |
| 21.3.5 | Serial Mode Register (SCSMR) | 744 |
| 21.3.6 | Serial Control Register (SCSCR) | 747 |
| 21.3.7 | Serial Status Register n (SCFSR) | 751 |
| 21.3.8 | Bit Rate Register n (SCBRR) | 758 |
| 21.3.9 | FIFO Control Register n (SCFCR) | 759 |
| 21.3.10 | Transmit FIFO Data Count Register n (SCTFDR) | 762 |
| 21.3.11 | Receive FIFO Data Count Register n (SCRFDR) | 763 |
| 21.3.12 | Serial Port Register n (SCSPTR) | 764 |
| 21.3.13 | Line Status Register n (SCLSR) | 767 |
| 21.3.14 | Serial Error Register n (SCRER) | 768 |
| 21.4 | Operation | 769 |
| 21.4.1 | Overview | 769 |
| 21.4.2 | Operation in Asynchronous Mode | 772 |
| 21.4.3 | Operation in Clocked Synchronous Mode | 783 |
| 21.5 | SCIF Interrupt Sources and the DMAC | 792 |
| 21.6 | Usage Notes | 794 |
| Section 22 Serial I/O with FIFO (SIOF) | | 797 |
| 22.1 | Features | 797 |
| 22.2 | Input/Output Pins | 799 |
| 22.3 | Register Descriptions | 800 |
| 22.3.1 | Mode Register (SIMDR) | 802 |

| | | |
|-------------------|---|------------|
| 22.3.2 | Clock Select Register (SISCR) | 804 |
| 22.3.3 | Control Register (SICTR) | 806 |
| 22.3.4 | Transmit Data Register (SITDR) | 809 |
| 22.3.5 | Receive Data Register (SIRDR) | 810 |
| 22.3.6 | Transmit Control Data Register (SITCR) | 811 |
| 22.3.7 | Receive Control Data Register (SIRCR) | 812 |
| 22.3.8 | Status Register (SISTR) | 813 |
| 22.3.9 | Interrupt Enable Register (SIIER) | 819 |
| 22.3.10 | FIFO Control Register (SIFCTR) | 821 |
| 22.3.11 | Transmit Data Assign Register (SITDAR) | 823 |
| 22.3.12 | Receive Data Assign Register (SIRDAR) | 824 |
| 22.3.13 | Control Data Assign Register (SICDAR) | 825 |
| 22.4 | Operation | 827 |
| 22.4.1 | Serial Clocks | 827 |
| 22.4.2 | Serial Timing | 829 |
| 22.4.3 | Transfer Data Format | 830 |
| 22.4.4 | Register Allocation of Transfer Data | 832 |
| 22.4.5 | Control Data Interface | 834 |
| 22.4.6 | FIFO | 836 |
| 22.4.7 | Transmit and Receive Procedures | 838 |
| 22.4.8 | Interrupts | 843 |
| 22.4.9 | Transmit and Receive Timing | 845 |
| Section 23 | Serial Protocol Interface (HSPI) | 849 |
| 23.1 | Features | 849 |
| 23.2 | Input/Output Pins | 851 |
| 23.3 | Register Descriptions | 851 |
| 23.3.1 | Control Register (SPCR) | 852 |
| 23.3.2 | Status Register (SPSR) | 854 |
| 23.3.3 | System Control Register (SPSCR) | 857 |
| 23.3.4 | Transmit Buffer Register (SPTBR) | 859 |
| 23.3.5 | Receive Buffer Register (SPRBR) | 860 |
| 23.4 | Operation | 861 |
| 23.4.1 | Operation Overview without DMA (FIFO Mode Disabled) | 861 |
| 23.4.2 | Operation Overview with DMA | 862 |
| 23.4.3 | Operation with FIFO Mode Enabled | 862 |
| 23.4.4 | Timing Diagrams | 863 |
| 23.4.5 | HSPI Software Reset | 864 |
| 23.4.6 | Clock Polarity and Transmit Control | 864 |
| 23.4.7 | Transmit and Receive Routines | 864 |

| | | |
|------------|--|-----|
| Section 24 | Multimedia Card Interface (MMCIF) | 865 |
| 24.1 | Features | 865 |
| 24.2 | Input/Output Pins | 866 |
| 24.3 | Register Descriptions | 867 |
| 24.3.1 | Command Registers 0 to 5 (CMDR0 to CMDR5) | 871 |
| 24.3.2 | Command Start Register (CMDSTRT) | 872 |
| 24.3.3 | Operation Control Register (OPCR) | 873 |
| 24.3.4 | Card Status Register (CSTR) | 875 |
| 24.3.5 | Interrupt Control Registers 0 to 2 (INTCR0 to INTCR2) | 877 |
| 24.3.6 | Interrupt Status Registers 0 to 2 (INTSTR0 to INTSTR2) | 880 |
| 24.3.7 | Transfer Clock Control Register (CLKON) | 885 |
| 24.3.8 | Command Timeout Control Register (CTOCR) | 886 |
| 24.3.9 | Transfer Byte Number Count Register (TBCR) | 887 |
| 24.3.10 | Mode Register (MODER) | 888 |
| 24.3.11 | Command Type Register (CMDTYR) | 889 |
| 24.3.12 | Response Type Register (RSPTYR) | 890 |
| 24.3.13 | Transfer Block Number Counter (TBNCR) | 894 |
| 24.3.14 | Response Registers 0 to 16, D (RSPR0 to RSPR16, RSPRD) | 895 |
| 24.3.15 | Data Timeout Register (DTOUTR) | 897 |
| 24.3.16 | Data Register (DR) | 898 |
| 24.3.17 | FIFO Pointer Clear Register (FIFOCLR) | 899 |
| 24.3.18 | DMA Control Register (DMACR) | 900 |
| 24.4 | Operation | 901 |
| 24.4.1 | Operations in MMC Mode | 901 |
| 24.5 | MMCIF Interrupt Sources | 931 |
| 24.6 | Operations when Using DMA | 932 |
| 24.6.1 | Operation in Read Sequence | 932 |
| 24.6.2 | Operation in Write Sequence | 942 |
| 24.7 | Register Accesses with Little Endian Specification | 953 |
| Section 25 | Audio Codec Interface (HAC) | 955 |
| 25.1 | Features | 955 |
| 25.2 | Input/Output Pins | 956 |
| 25.3 | Register Descriptions | 957 |
| 25.3.1 | Control and Status Register (HACCR) | 958 |
| 25.3.2 | Command/Status Address Register (HACCSAR) | 960 |
| 25.3.3 | Command/Status Data Register (HACCSDR) | 962 |
| 25.3.4 | PCM Left Channel Register (HACPCML) | 963 |
| 25.3.5 | PCM Right Channel Register (HACPCMR) | 965 |
| 25.3.6 | TX Interrupt Enable Register (HACTIER) | 966 |

| | | |
|---|--|-------------|
| 25.3.7 | TX Status Register (HACTSR)..... | 967 |
| 25.3.8 | RX Interrupt Enable Register (HACRIER)..... | 969 |
| 25.3.9 | RX Status Register (HACRSR)..... | 970 |
| 25.3.10 | HAC Control Register (HACACR)..... | 971 |
| 25.4 | AC 97 Frame Slot Structure..... | 973 |
| 25.5 | Operation..... | 974 |
| 25.5.1 | Receiver..... | 974 |
| 25.5.2 | Transmitter..... | 975 |
| 25.5.3 | DMA..... | 975 |
| 25.5.4 | Interrupts..... | 975 |
| 25.5.5 | Initialization Sequence..... | 976 |
| 25.5.6 | Notes..... | 981 |
| 25.5.7 | Reference..... | 981 |
| Section 26 Serial Sound Interface (SSI) Module..... | | 983 |
| 26.1 | Features..... | 983 |
| 26.2 | Input/Output Pins..... | 984 |
| 26.3 | Register Descriptions..... | 985 |
| 26.3.1 | Control Register (SSICR)..... | 986 |
| 26.3.2 | Status Register (SSISR)..... | 992 |
| 26.3.3 | Transmit Data Register (SSITDR)..... | 997 |
| 26.3.4 | Receive Data Register (SSIRDR)..... | 997 |
| 26.4 | Operation..... | 998 |
| 26.4.1 | Bus Format..... | 998 |
| 26.4.2 | Non-Compressed Modes..... | 999 |
| 26.4.3 | Compressed Modes..... | 1008 |
| 26.4.4 | Operation Modes..... | 1011 |
| 26.4.5 | Transmit Operation..... | 1012 |
| 26.4.6 | Receive Operation..... | 1015 |
| 26.4.7 | Serial Clock Control..... | 1018 |
| 26.5 | Usage Note..... | 1019 |
| 26.5.1 | Restrictions when an Overflow Occurs during Receive DMA Operation..... | 1019 |
| Section 27 NAND Flash Memory Controller (FLCTL)..... | | 1021 |
| 27.1 | Features..... | 1021 |
| 27.2 | Input/Output Pins..... | 1024 |
| 27.3 | Register Descriptions..... | 1025 |
| 27.3.1 | Common Control Register (FLCMNCR)..... | 1026 |
| 27.3.2 | Command Control Register (FLCMDCR)..... | 1028 |
| 27.3.3 | Command Code Register (FLCMCDR)..... | 1030 |