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RAA23021x

5.5V Input, 3A, Step-Down DC/DC Converter + LDO

R18DS0013EJ0102
Rev.1.02
Jul 23, 2014

Description

The RAA23021x is a high efficiency monolithic step-down DC/DC synchronous converter plus a LDO (low dropout) regulator which has an ultra-low power mode.

Features

- DC/DC converter (ch1)
  - Synchronous rectification type step-down circuit
  - Integrated power MOSFETs
  - Preset output voltage (There are also products that have adjustable output voltage using external resistors.)
  - Internal phase compensator
  - Switching frequency: 1 MHz (fixed)
  - Internal timer-latch-type short-circuit protector (fixed delay time)
  - 100% duty cycle operation
- LDO (ch2)
  - 500mA
  - Internal over current protector (foldback-current limiting)
  - Ultra low-power save mode (25uA typical)
- Common Features
  - Internal rise up sequencer
  - Internal digital soft-start function (2 ms fixed soft-start time)
  - Internal discharge circuit
  - Power good function
  - Internal timer-latch-type thermal shutdown circuit (shutdown temperature: 150°C or higher)
  - Internal recovery-type under voltage lockout circuit

Application

- Communication
- Industrial
- Building
- Smart meter

  And, usable around MCU, ASIC, FPGA, etc.

Ordering Information

Ordering Part No.	Package	Tape and Reel
RAA230214GSB#HA0 RAA230215GSB#HA0	20-pin HTSSOP	Embossed taping. 2,500pcs/reel

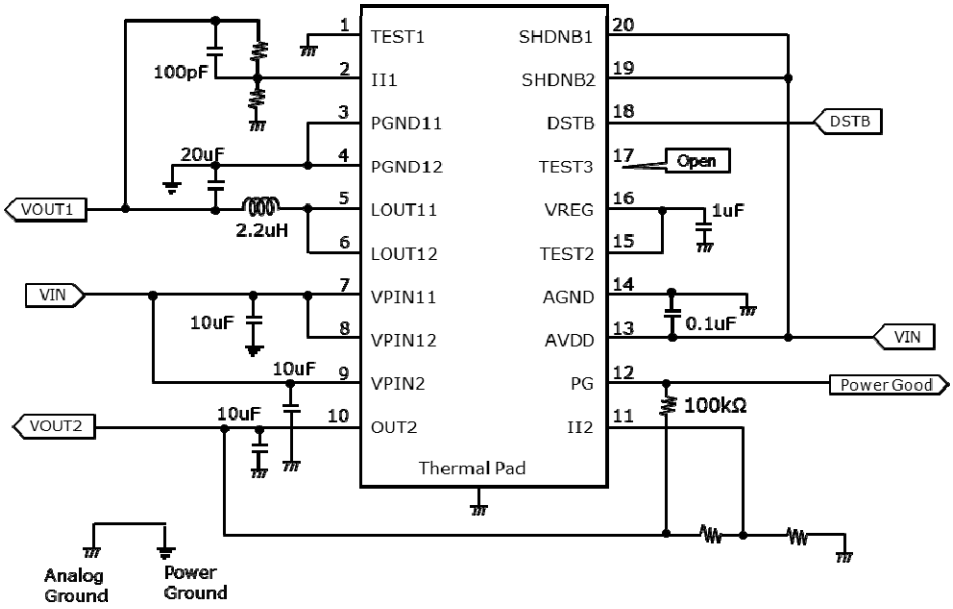
Note: A quality grade of these ICs is “Standard”. Recommended applications are indicated below.

Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, and industrial robots, etc.

Part No Summary

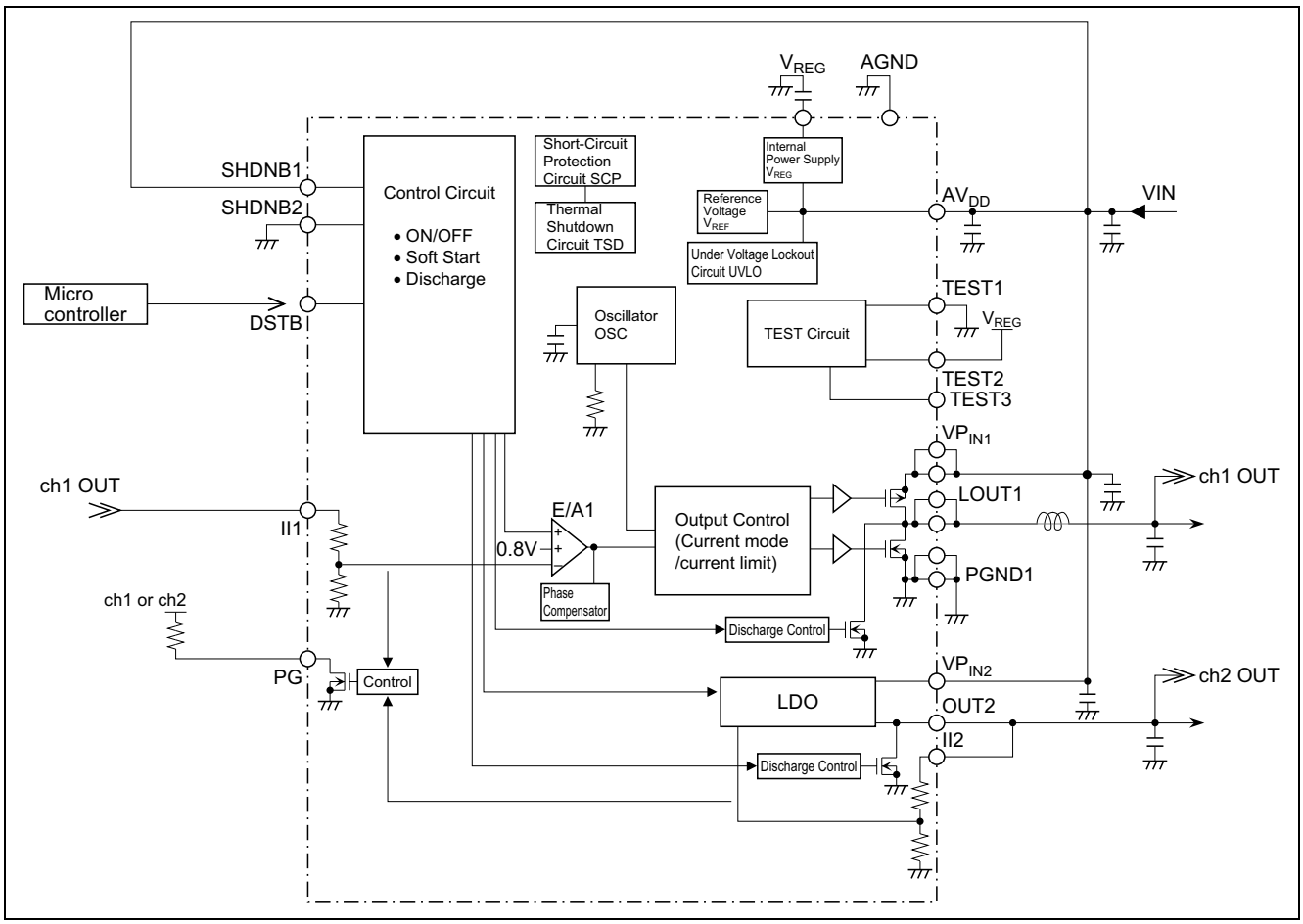
Part No.	Output	Input Voltage	Output Voltage		Maximum Output Current	Switching Frequency	Package
			ch1	ch2			
RAA230214GSB	ch1:DC/DC (step-down, current mode) ch2:LDO	3.0 V to 5.5 V	3.3	3.3	ch1:3 A ch2:0.5 A	1 MHz (fixed)	20-pin HTSSOP
RAA230215GSB			0.9 V to VIN×0.8 (Adjustable each output individually by external resistor)				

Circuit example (RAA230215GSB)

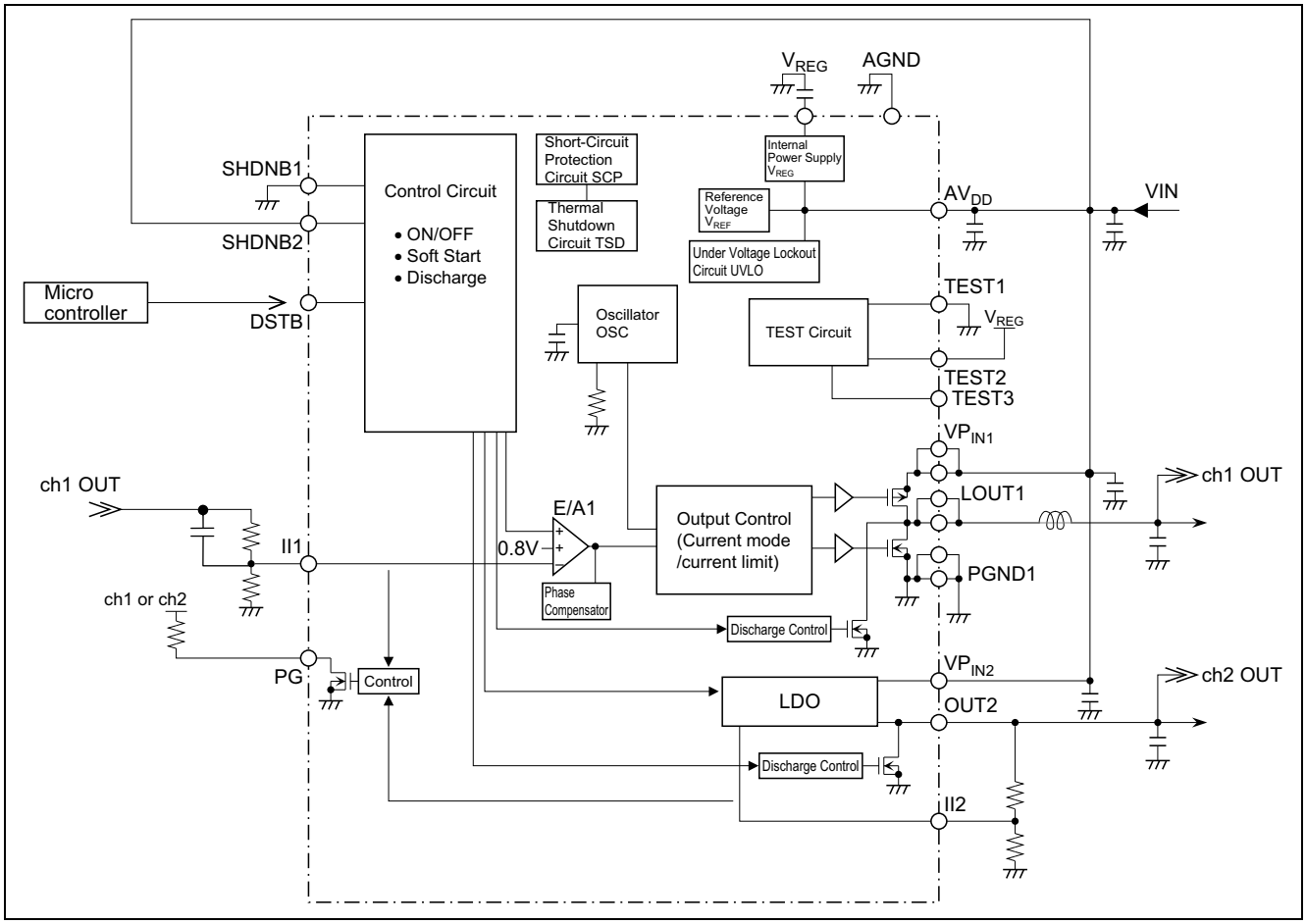


Block Diagram

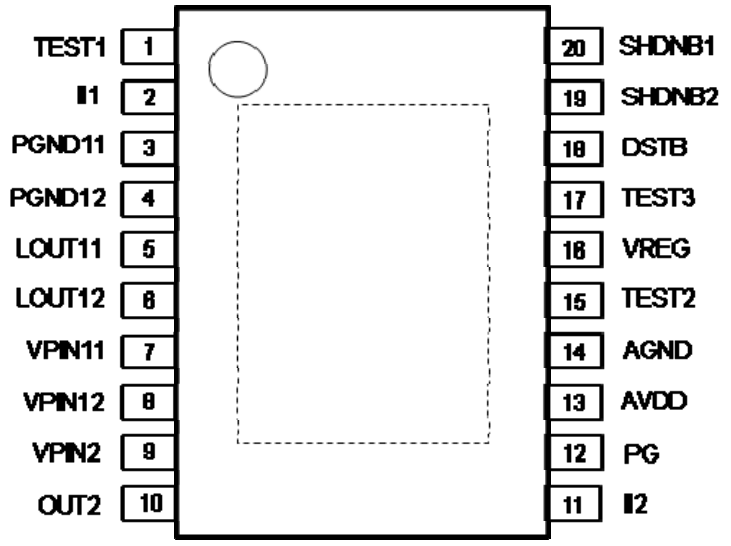
ch1/ch2: Preset output voltage by internal resistor. Sequence pattern 1 (ch1 followed by ch2)



ch1/ch2: Adjustable output voltage by external resistor.
Sequence pattern 2 (ch2 followed by ch1)



Pin Configuration



(Top View)

Pin Function

Pin No.	Symbol	I/O	Function
1	TEST1	—	Test pin 1 (connect to AGND)
2	II1	Input	Inverted input for error amplifier of ch1
3	PGND11	Ground	Power ground
4	PGND12	Ground	Power ground
5	LOUT11	Output	Inductor connection 1 for ch1
6	LOUT12	Output	Inductor connection 2 for ch1
7	VP_{IN11}	Power supply	Output stage power input 1 of ch1
8	VP_{IN12}	Power supply	Output stage power input 2 of ch1
9	VP_{IN2}	Power supply	Output stage power input of ch2
10	OUT2	Output	Output of ch2
11	II2	Input	Inverted input for error amplifier of ch2
12	PG	Output	Power-good output (open-drain)
13	AV_{DD}	Power supply	Analog block power supply
14	AGND	Ground	Analog ground
15	TEST2	—	Test pin 2 (connect to V_{REG})
16	V_{REG}	Output	Internal power supply output (connect 1uF)
17	TEST3	—	Test pin 3 (open)
18	DSTB	Input	Light-load operation mode setting pin
19	SHDNB2	Input	Output ON/OFF of ch2
20	SHDNB1	Input	Output ON/OFF of ch1

Absolute Maximum Ratings

(Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	Ratings	Unit	Condition
Analog power supply (AV_{DD} pin)	AV_{DD}	–0.5 to +6.5	V	AV_{DD}
VP_{IN} pin applied voltage	VP_{IN}	–0.5 to +6.5	V	VP_{IN11}, VP_{IN12}, VP_{IN2}
SHDNB pin applied voltage	V_{SHDNB}	–0.5 to +6.5	V	SHDNB1, SHDNB2
DSTB pin applied voltage	V_{DSTB}	–0.5 to +6.5	V	DSTB
PG pin applied voltage	V_{PG}	–0.5 to +6.5	V	PG
II pin applied voltage	V_{II}	–0.5 to +6.5	V	II1, II2
VP_{IN11}+VP_{IN12} pin sink current (peak)	$IP_{IN1(peak)-}$	3500	mA	VP_{IN11}+VP_{IN12}
LOUT11+LOUT12 pin output source current (peak)	$I_{LO1(peak)+}$	3500	mA	LOUT11, LOUT12
VP_{IN2} pin sink current (DC)	$IP_{IN2(DC)-}$	500	mA	VP_{IN2}
OUT2 pin output source current (DC)	$I_{O2(DC)+}$	500	mA	OUT2
LOUT11+LOUT12, OUT2 pin output source current (DC)	$I_{LO1,O2(DC)-}$	100	mA	when discharge circuit is operation.
Total power dissipation	P_T	3400*1	mW	$T_A \leq$ +25°C
Operating ambient temperature	T_A	–40 to +85	°C	
Junction temperature	T_J	–40 to +150	°C	
Storage temperature	T_{stg}	–55 to +150	°C	

Note:

*1 This is the value at $T_A \leq$ +25°C. At T_A > +25°C, the total power dissipation is derated by 34mW/°C.
Board specification : 4-layers glass epoxy board, 76.2mm x 114.3mm x 1.664mm.
Copper coverage area: 50%, 0.070mm thickness (top and bottom layers)
95%, 0.035mm thickness (layers 2 and 3).
Connecting exposed pad

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Condition

(Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Analog power supply voltage (AV_{DD} pin)	AV_{DD}	3.0	5.0	5.5	V	AV_{DD}
VP_{IN} pin applied voltage	VP_{IN}	—	AV_{DD}	—	V	VP_{IN11}, VP_{IN12}, VP_{IN2}
SHDNB pin applied voltage	V_{SHDNB}	0	—	AV_{DD}	V	SHDNB1, SHDNB2
DSTB pin applied voltage	V_{DSTB}	0	—	AV_{DD}	V	DSTB
PG pin applied voltage	V_{PG}	0	—	AV_{DD}	V	PG
II pin applied voltage	V_{II}	0	—	AV_{DD}	V	II1, II2
V_{REG} pin capacitance	C_{REG}	—	1.0	—	µF	V_{REG}
Operating junction temperature	T_{JO}	–40	—	+125	°C	

Electrical Characteristics

(Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} = VP_{IN2} = 5.0 V, VOUT2 = 3.3 V, f_{OSC} = 1 MHz, DSTB = L)

Parameter		Symbol	Min	Typ	Max	Unit	Condition
Total	Standby current	$I_{DD(STNBY)}$	—	1	2	μA	AI_{DD}+IP_{IN1}+IP_{IN2} SHDNB1 = SHDNB2 = AGND
	Circuit operation current 1	I_{DD1}	—	1.2	2	mA	AI_{DD}, SHDNB1 = SHDNB2 = AV_{DD} DSTB = GND (normal mode)
	Circuit operation current 2	I_{DD2}	—	25	45	μA	AI_{DD}, SHDNB1 = SHDNB2 = AV_{DD} DSTB = AV_{DD} (ultra low-power mode)
Internal power supply block (V_{REG})	Internal power supply voltage	V_{REG}	2.25	2.4	2.55	V	I_{REG} = 0mA
Under voltage lock out circuit (UVLO)	Operation start voltage during rise time	$AV_{DD(L-H)}$	2.7	2.9	3.0	V	AV_{DD} pin voltage is detected
	Operation stop voltage	$AV_{DD(H-L)}$	2.6	2.8	3.0	V	AV_{DD} pin voltage is detected
Short-circuit protection circuit (SCP)	II1 input detection voltage (ch1)	$V_{TH(II)1}$	65	75	85	%	II1 pin, Ratio to the output voltage or E/A1 threshold voltage
	Delay time	$t_{(DLY)}$	—	10	20	ms	
Oscillation block	Oscillation frequency	f_{OSC}	—	1000	—	kHz	
Soft start block	Soft start time	t_{ss}	0.9	2.0	4.0	ms	ch1, ch2
PWM block	Maximum duty	$D_{MAX.(PWM)}$	—	100	—	%	ch1
Output voltage accuracy (with resistor inside)	ch1 output voltage accuracy	V_{OUT1}	–2.5	—	+2.5	%	I_{O1} = 200mA, (with internal resistor)
	ch2 output voltage accuracy	V_{OUT2}	–1	—	+1	%	I_{O2} = 10mA, (with internal resistor)
E/A block (with resistor outside)	E/A 1 input threshold voltage	V_{ITH1}	0.780	0.800	0.820	V	Including input offset, (with external resistor)
	E/A 2 input threshold voltage	V_{ITH2}	0.792	0.800	0.808	V	Including input offset, (with external resistor)
Output block	P-ch ON resistance	R_{on-p1}	—	0.15	0.3	Ω	I_O = 100mA
	N-ch ON resistance	R_{on-n1}	—	0.15	0.3	Ω	I_O = –100mA
Discharging circuit block	ch1 ON resistance	R_{ondc1}	—	100	200	Ω	ch1, I_{DC} = 20mA
	ch2 ON resistance	R_{ondc2}	—	200	400	Ω	ch2, I_{DC} = 20mA
Series regulator block (ch2, DSTB = AGND: normal mode)	The voltage between the input and output	V_{DIF2}	0.5	—	—	V	I_{O2} = 20mA
	Input regulation	REG_{IN2}	—	—	50	mV	I_{O2} = 20mA, VP_{IN} = 3.0V to 5.5V
	Load regulation	REG_{L2}	—	—	50	mV	I_{O2} = 1mA to 500mA
	Output short-circuit current	$I_{O2short}$	—	100	—	mA	OUT2=AGND
	Peak output current	I_{O2peak}	550	—	—	mA	
Series regulator block (ch2, DSTB = AV_{DD}: ultra low-power mode)	The voltage between the input and output	V_{DIF2}	0.5	—	—	V	I_{O2} = 10μA
	Input regulation	REG_{IN2}	—	—	100	mV	I_{O2} = 10μA, VP_{IN} = 3.0V to 5.5V
	Load regulation	REG_{L2}	—	—	100	mV	I_{O2} = 10μA to 50mA

Electrical Characteristics (cont.)

(Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} = VP_{IN2} = 5.0 V, VOUT2 = 3.3 V, f_{OSC} = 1 MHz, DSTB = L)

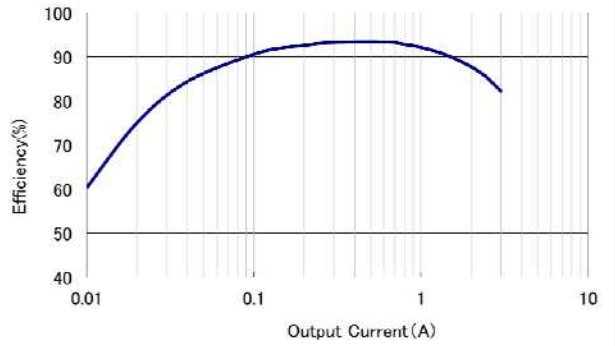
Parameter		Symbol	Min	Typ	Max	Unit	Condition
Power-good circuit block	Threshold voltage	$V_{TH(PG)}$	86	90	94	%	PG = "HiZ"→"L", "L"→"HiZ" Ratio to the output voltage
	PG pin output voltage	V_{PG}	—	—	0.1	V	I_{PG-} = 0.1mA
	PG pin leakage current	$I_{LEAK-PG}$	—	—	1	µA	SHDNB1, SHDNB2 = AGND
	Delay time	t_{DLY-PG}	—	—	2	ms	Time from detecting of output startup until change form L to HiZ on PG pin
ON/OFF controller block	Threshold voltage	V_{TH}	0.6	—	1.4	V	SHDNB1, SHDNB2, DSTB

Typical Performance Characteristics

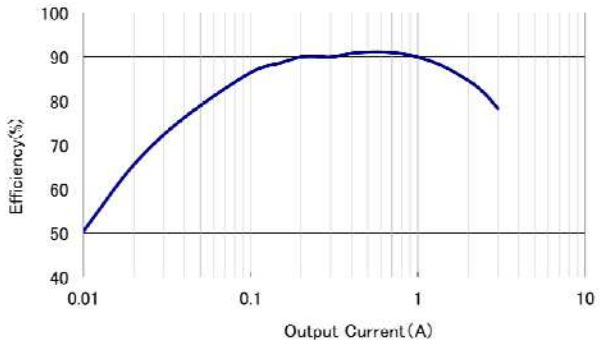
(Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} = VP_{IN2} = 5.0 V)

Efficiency vs. Output Current (ch1)

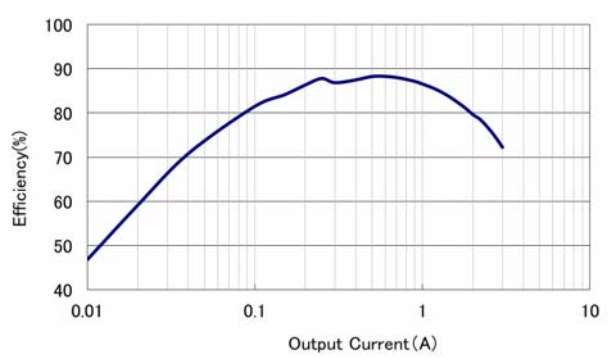
VOUT=3.3 V



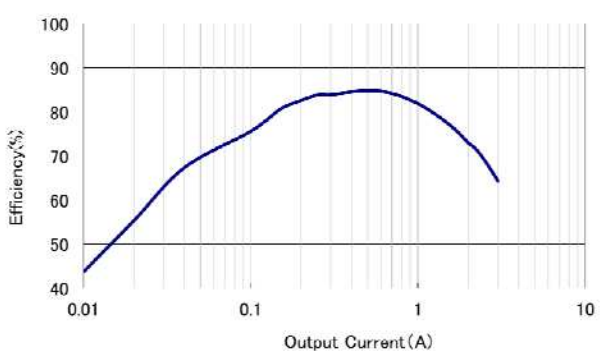
VOUT=2.5V



VOUT=1.8 V



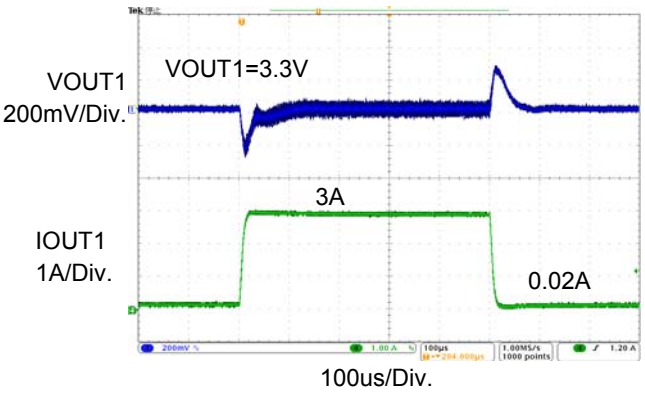
VOUT=1.2V



Load Step Transient Waveforms

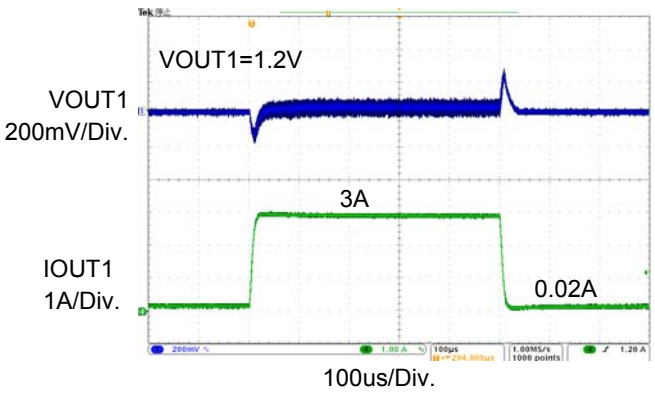
TA = 25°C, VIN = 5V, L1 = 2.2uH, CIN1 = CIN2 = 10uF, COUT1 = 20uF, COUT2 = 10uF

ch1



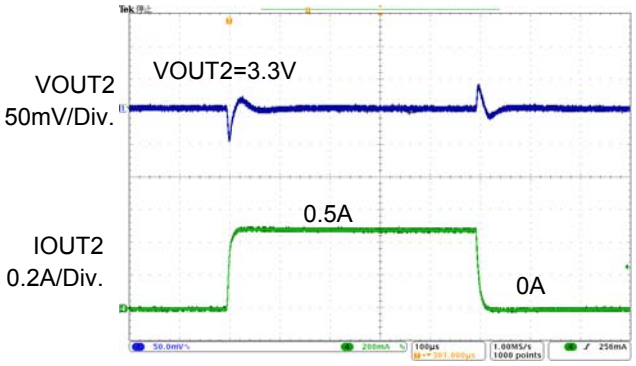
100us/Div.

ch1



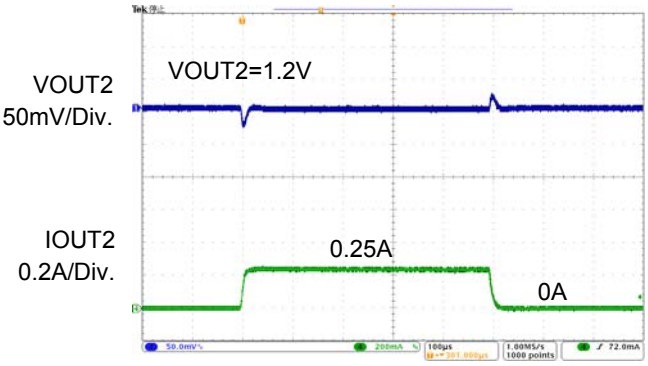
100us/Div.

ch2 Normal operation



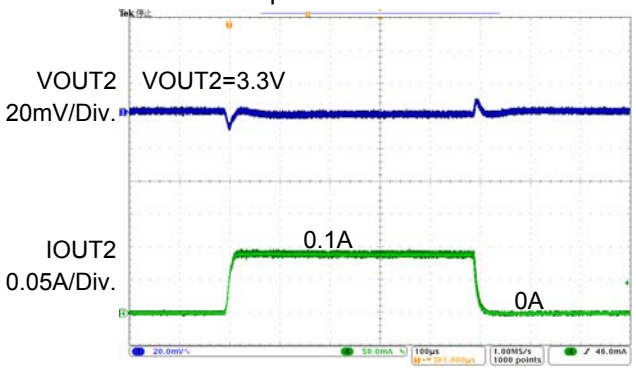
100us/Div.

ch2 Normal operation



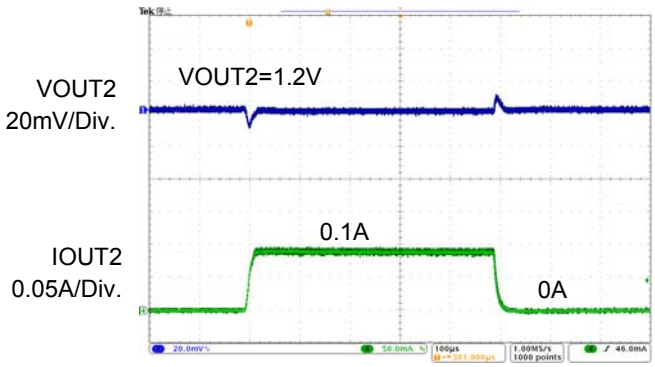
100us/Div.

ch2 Ultra low-power mode



100us/Div.

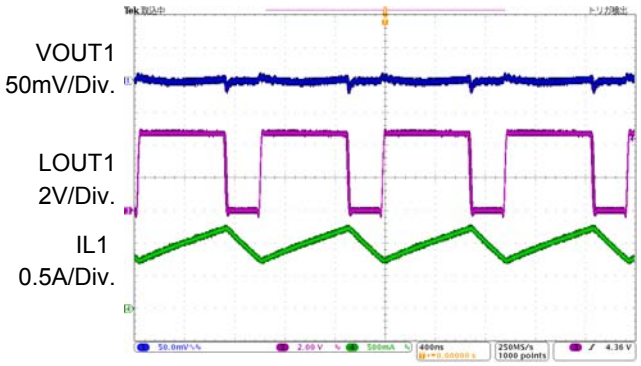
ch2 Ultra low-power mode



100us/Div.

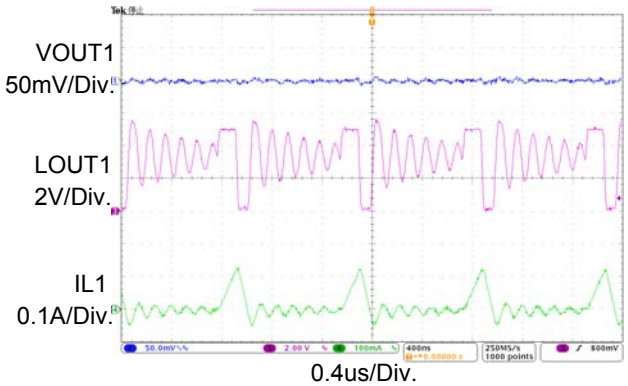
Ch1 Operation Waveforms

VOUT1=3.3V, IOUT1=1A



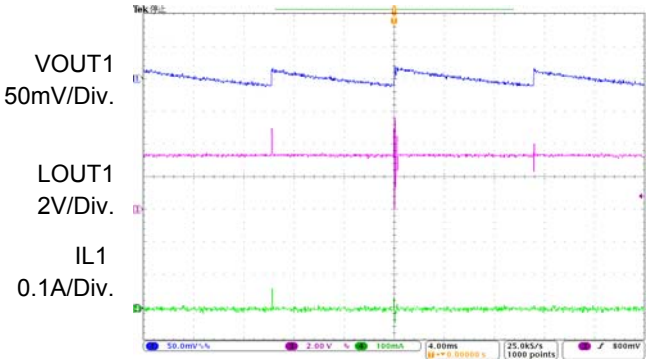
0.4us/Div.

VOUT1=3.3V, IOUT1=0.01A



0.4us/Div.

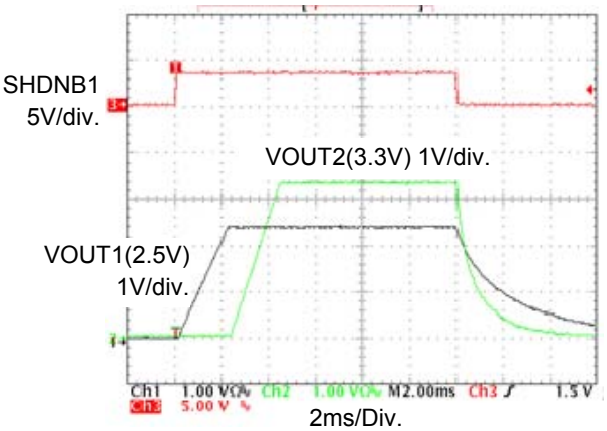
VOUT1=3.3V, IOUT1=0A



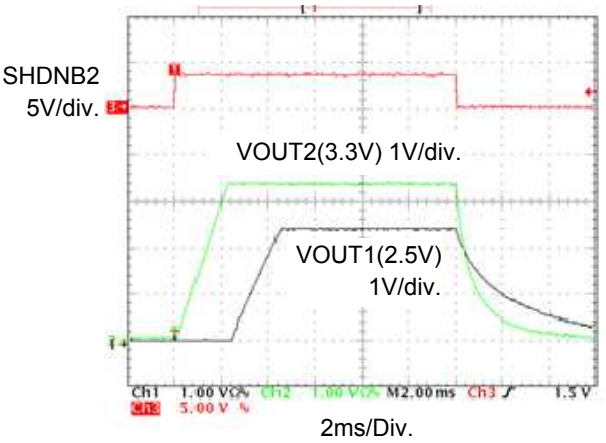
4ms/Div.

Start-up and Shutdown Waveforms

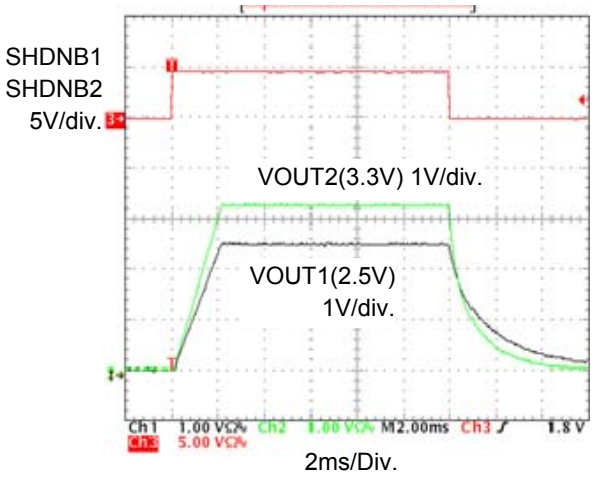
Only SHDNB1 ON



Only SHDNB2 ON

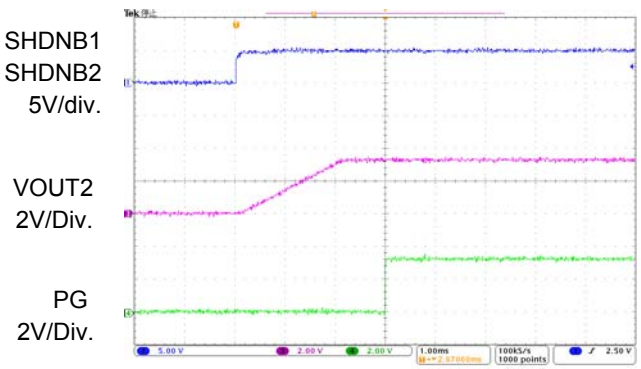


Both SHDNB1 and SHDNB2 ON at the same time



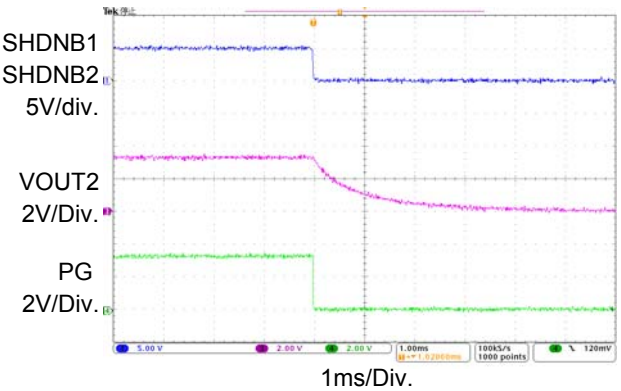
Power Good Waveform *PG pin is connected to ch2 output(3.3V)

Start-up



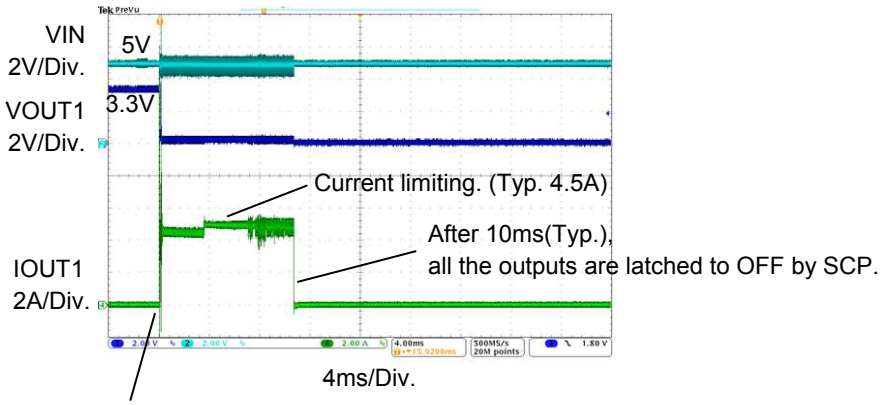
1ms/Div.

Shutdown



1ms/Div.

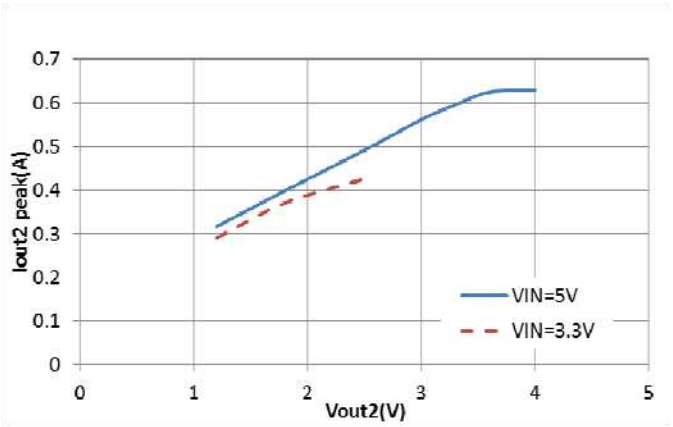
Short-circuit protection waveform



4ms/Div.

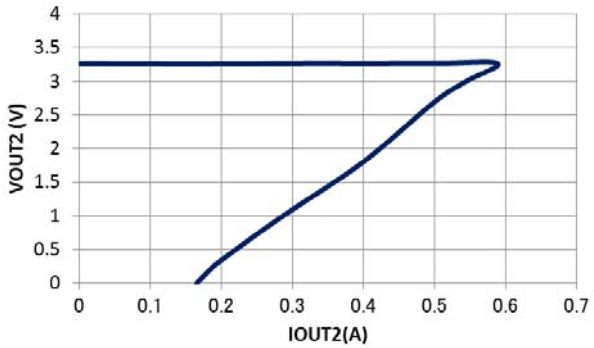
Ch1 output short-circuits.

Ch2(LDO) peak output current vs. output voltage (VIN=5.0V)

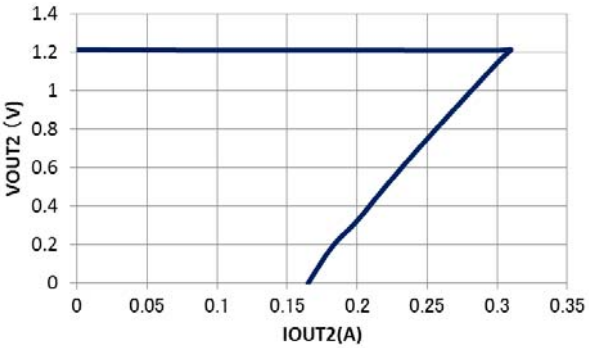


Ch2(LDO) output voltage vs. output current (VIN=5.0V)

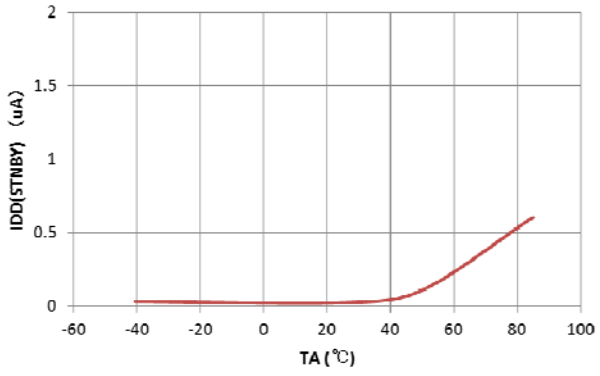
VOUT2=3.3V



VOUT2=1.2V

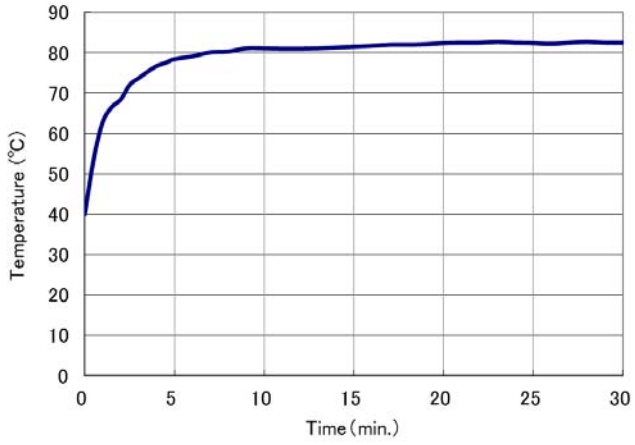


Standby current vs. Operating ambient temperature

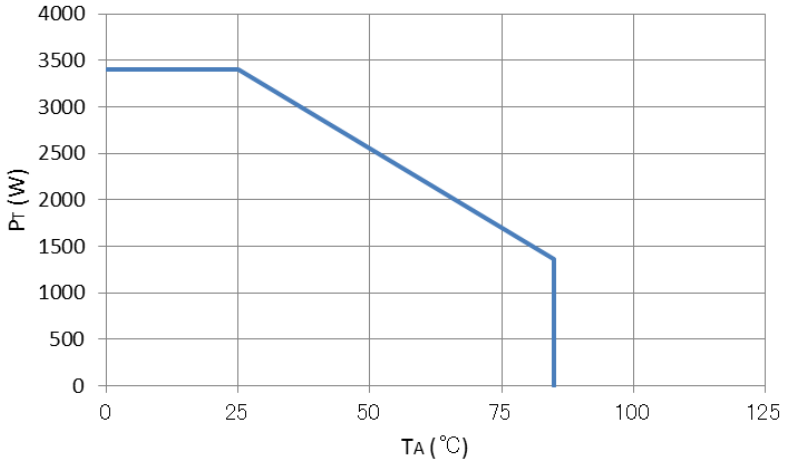


IC Surface Temperature vs. Time

Ch1 and ch2 operation (normal mode)
VIN=5V
ch1:3.3V, 2A ch2 : 1.8V, 0.3A
T_A = 25°C
Measured on Renesas Evaluation Board



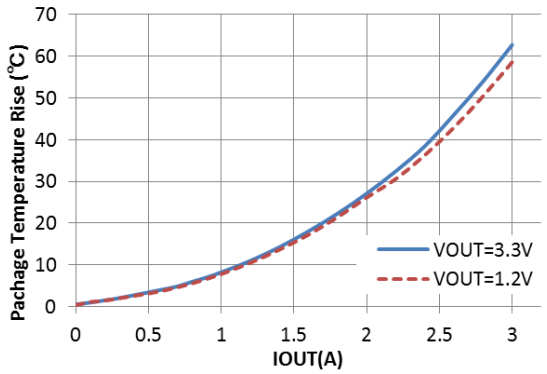
Temperature Derating Curve



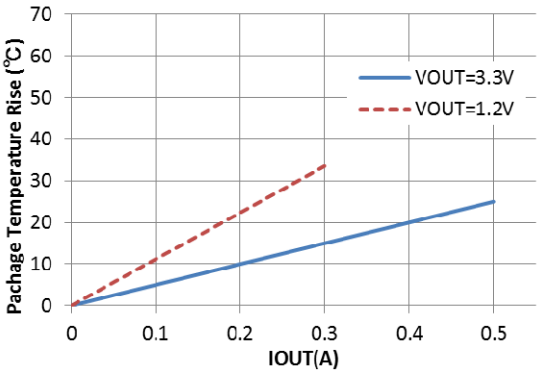
Pakage Tempereture Rise vs. IOUT

VIN=5.0V

Only ch1 operation



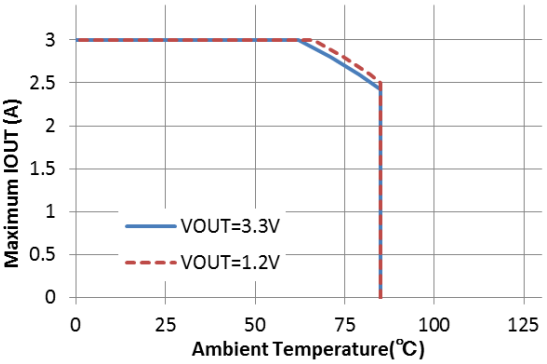
Only ch2 operation



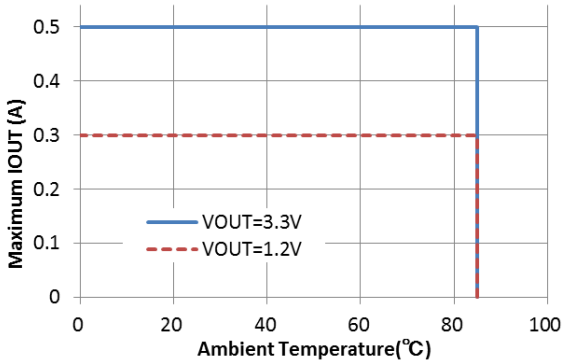
Maximum IOUT vs. Ambient Tempereture

VIN=5.0V

Only ch1 operation



Only ch2 operation



Note : When calculate the package temperature with both ch1 and ch2 operation, reference these data.

Control Block

SHDNB1, SHDNB2: ON/OFF Setting

SHDNB1	SHDNB2	ch1	ch2
L	L	OFF	OFF
H	L	Start-up in order of ch1 and ch2 Stop ch1 and ch2 at the same time	
L	H	Start-up in order of ch2 and ch1 Stop ch1 and ch2 at the same time	
H	H	Start-up ch1 and ch2 at the same time Stop ch1 and ch2 at the same time	

Note: L: Low level, H: High level
OFF: circuit stand-by, ON: circuit operation status
When both SHDNB1 and SHDNB2 are H, RAA23021x continues operation even if one of them is turned to L.
RAA23021x stops when both of them are turned L.

DSTB: IC Ultra Low-Power Mode Setting

DSTB	IC Operation
L	Normal operation
H	Ultra low-power mode operation (ch1: stop, ch2: operation)

Note: L: Low level, H: High level

Output Status

V_{REG} Pin Status

SHDNB1	SHDNB2	DSTB	V_{REG}
L	L	L or H	AGND
H	L	L	2.4 V
L	H		
H	H		
H	L	H	AGND
L	H		
H	H		

Note: L: Low level, H: High level

ch1, ch2 Output Pin Status

ch1 · ch2 Status	ch1	ch2
	LOUT1	OUT2
Stop	PGND (Discharge circuit: On)*	AGND (Discharge circuit: On)
Operation	Pulse (VP_{IN1} or PGND)	Set voltage

Note: Ch1 discharge circuit is “On” during ultra low-power mode.

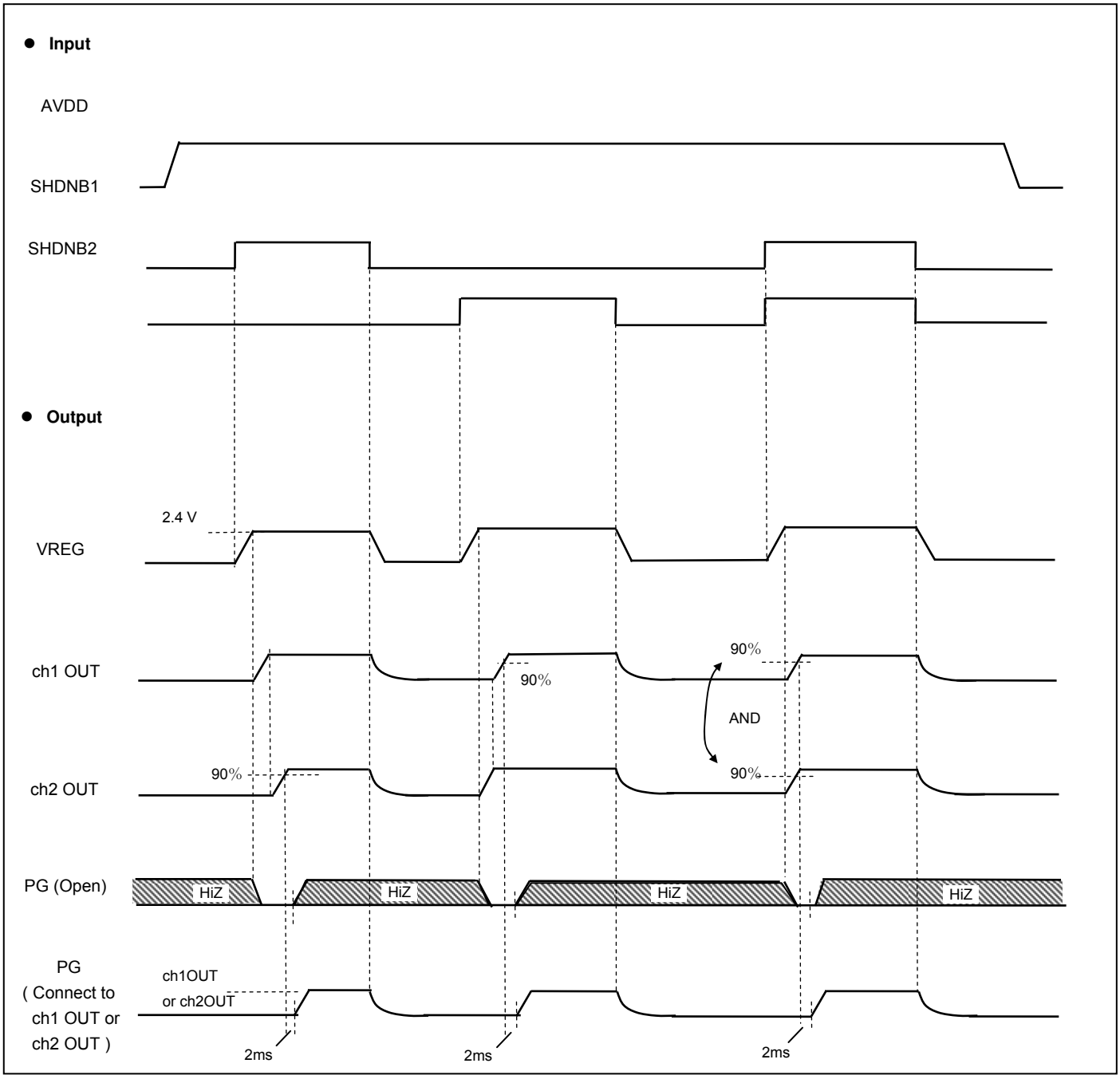
PG Pin Status (ch1, ch2 output detect)

IC Operation Status			PG Output Status
SHDNB Pin	DSTB Pin	ch1, ch2 Output Status	
SHDNB1 = L SHDNB2 = L	L or H	Stop	HiZ
SHDNB1 = H or SHDNB2 = H	L	ch1 or ch2 output voltage is under 90% of the set voltage	L
		ch1 and ch2 output voltage are over 90% of the set voltage	HiZ
	H	ch1: Stop ch2: Operation (Both output voltage is over 90% of setting voltage and under 90%)	HiZ

Note: L: Low level, H: High level, HiZ: High impedance

Caution: When both ch1 and ch2 output voltage start up over 90%, there is delay time (under 2ms) before PG pin becomes HiZ.
When using power good (PG pin), connect it to ch1 or ch2 output. Recommended value of pull-up resistor is 100kΩ.

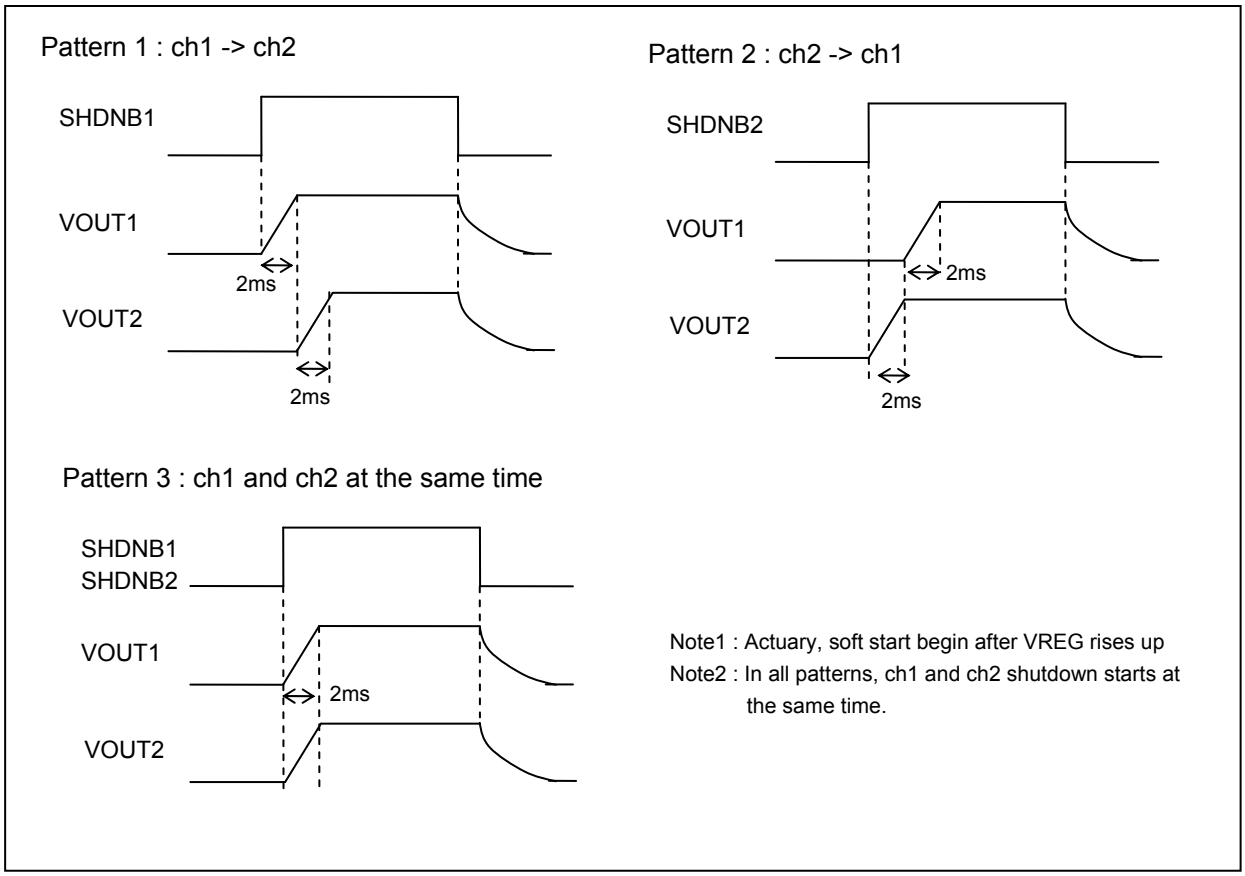
Timing Chart



Operation of Each Block (Overview)

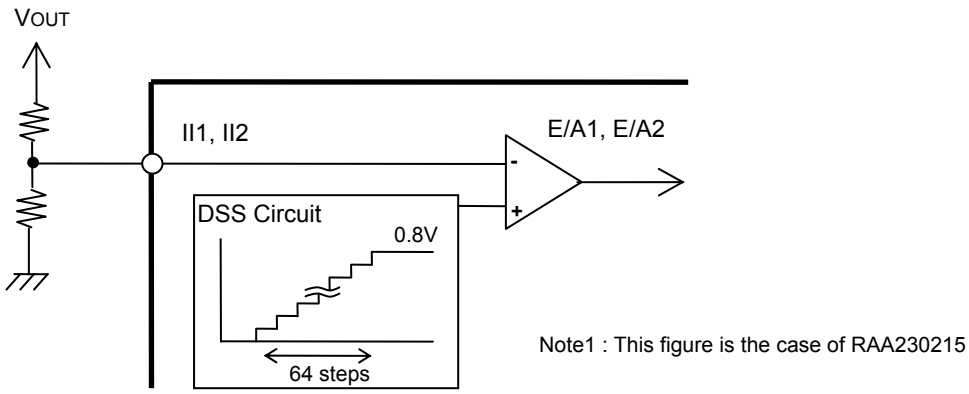
Rise up sequencer

The IC “rise up” sequence feature has 3 patterns described below. The internal “rise up” sequence capability does not need any additional external circuitry or components.

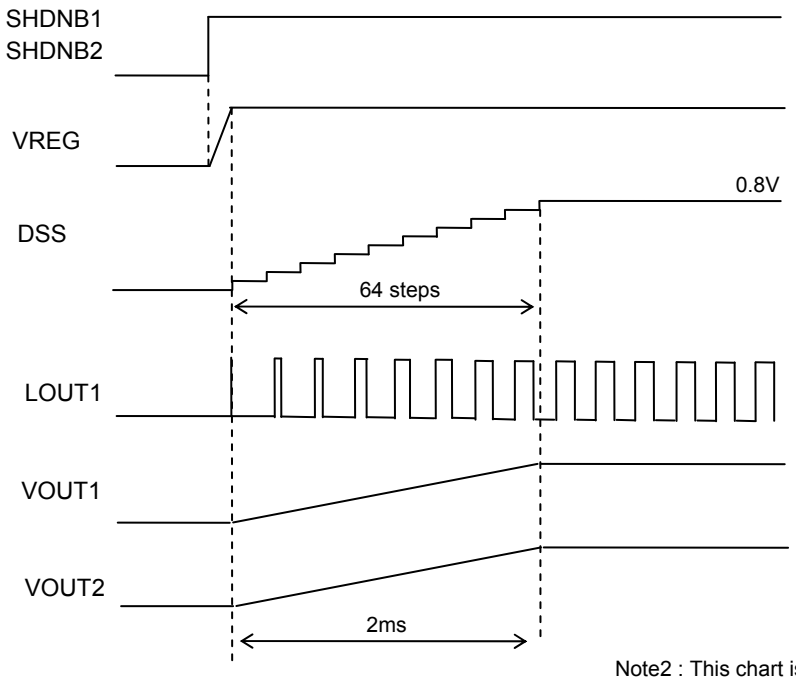


Soft start

To limit the startup inrush current and output voltage overshoot, a soft start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. The soft start time are fixed for both ch1 and ch2 are 2ms(Typ.) and no additional components are needed. Soft start feature gradually increases the error amplifier (E/A) input threshold voltage by using the voltage that is generated by the digital soft start (DSS) circuit in 64 steps.



Note1 : This figure is the case of RAA230215



Note2 : This chart is the case that ch1 and ch2 start at the same time

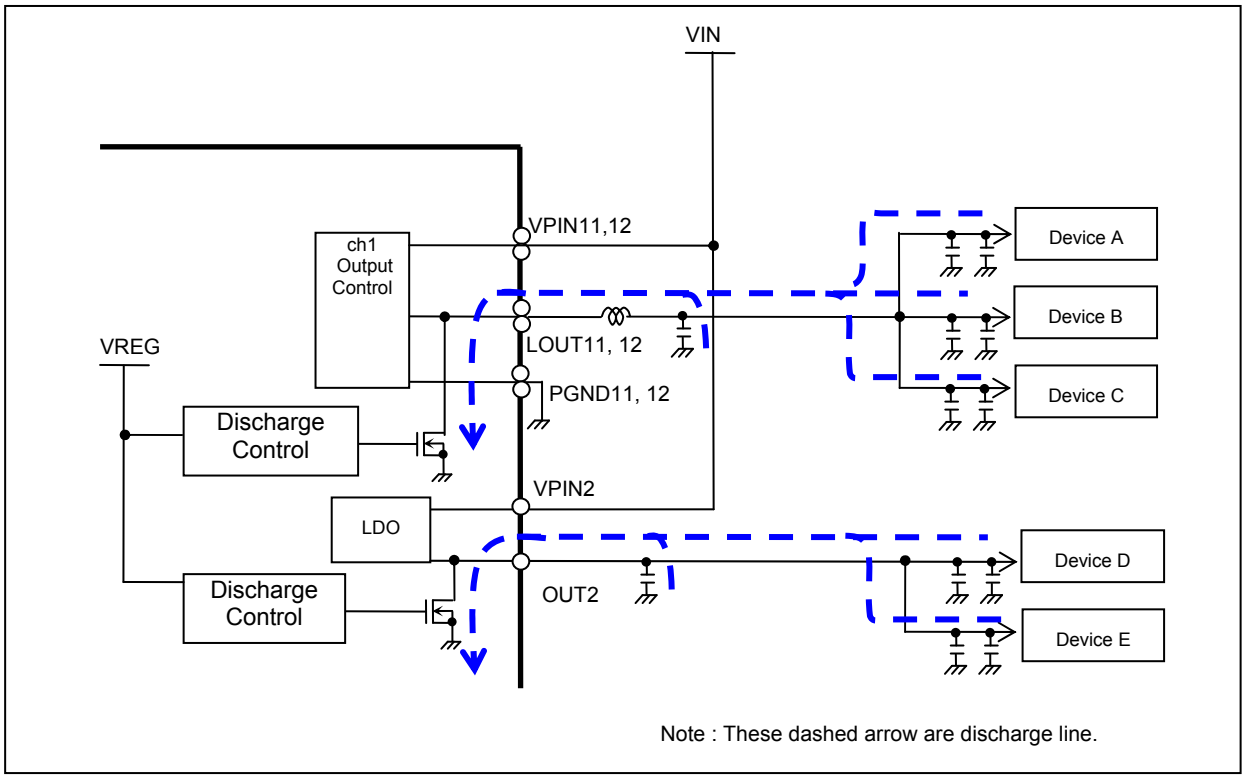
Note3 : DSS waveform cannot be observed from IC outside.

Discharge circuit

This IC has the discharge circuit for both ch1 and ch2. This enables a rapid discharge without an external MOSFET. When SHDNB pin is changed from high level to low, discharge switches of ch1 and ch2 turn on at the same time, and they discharge all capacitors which are connected to each output through LOUT1 and OUT2 pin.

When AVDD pin voltage becomes low level, discharge switches become off because there are no voltage to keep them on. The control voltage of discharge switches is VREG, and the discharge time of VREG capacitor is over 100ms when AVDD voltage fall down, so even if SHDNB pin is connected to AVDD pin, the output voltage of ch1 and ch2 can be discharged because VREG voltage level can keep the discharge switches on.

About calculation of discharge time, see page 30.



Power Good

Power Good (PG) is an open-drain output that requires a pull − up resistor (Recommended value = 100kΩ). PG releases when the both ch1 and ch2 FB voltage and thus the output voltage rises above 90% of nominal regulation point. The PG goes low when the FB voltage falls below 90% of the regulation point. When both SHDNB pins become low level, PG pin become high impedance (HiZ) because VREG is used for PG control and it fall down at this time. So, if PG is connected to AVDD, its status keep high level. PG pin must be connected to ch1 or ch2 output.

This function can be used for sequence signal for other devices.

Protection Circuit View

Protection Circuit	Function	Operation Status		Reset
		Common Circuit (V_{REG}, OSC, etc.)	Output	
Short-circuit protection (SCP) *Only ch1	Detect ch1 output voltage dropping because of short-circuit, etc. (Timer latch type)	Operation	All the output are latched to OFF	Change SHDNB1 pin and SHDNB2 pin from high to low or Drop AV_{DD} pin input voltage under the operation stop voltage (2.8 V)
Thermal shutdown circuit (TSD)	Detect increase of IC internal temperature (Over 150°C) (Timer latch type)	Operation	All the output are latched to OFF	
Over current protection (OCP) *Only ch2	Detect ch2 over current	Operation	ch2 output is down (ch1 continues operation)	Release over current status (Under the output short-circuit current: 100 mA)
Under voltage lockout circuit (UVLO)	Detect dropping of AV_{DD} (IC power supply)	Operation[*1]	All the outputs are stop	Up AV_{DD} pin input voltage over the operation start voltage (2.9 V)

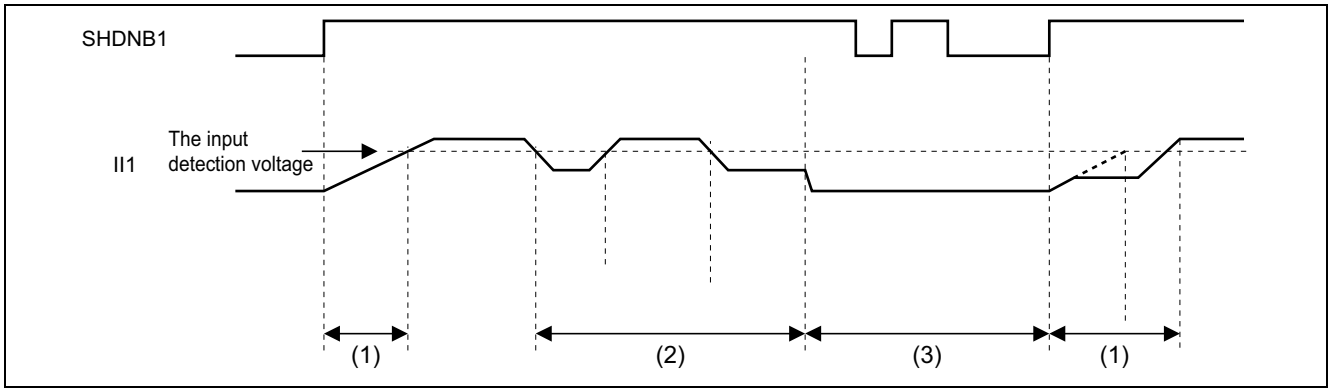
Note: The common circuit stops if AVDD is lower than VREG.
When ultra low-power mode, these protection circuits DO NOT operate.

Short-Circuit Protection Circuit (ch1)

When the voltage of ch1 drops, the voltage of the II1 pin also drops. If it falls below the input detection voltage of the short-circuit protection circuit (under 75% of output voltage), the timer circuit starts operating. And after 10 ms, all the outputs are latched to OFF. At this time, common circuits (such as the internal power supply block, and oscillator, etc.) continue operating.

When the short-circuit protection circuit is operating, to reset the latch circuit, either change the level of the SHDNB1 pin and SHDNB2 pin from high to low or drop the level of the power supply voltage (AV_{DD}) to the level below the operation stop voltage of the under voltage lockout circuit (2.8 V).

- Timing Chart (when ch1 is short circuited)



(1) At starting
- A short-circuit will not be detected while the ch1 is undergoing a soft start (that is, short-circuit protection is not triggered). If a short circuit occurs while ch1 is starting, short-circuit protection will start after the soft start time elapses following startup.
- If a short-circuit occurs in a channel that is operating while another channel is being soft-started, short-circuit protection will start immediately.

(2) Short-circuit protection operation
- If a short circuit is detected in ch1 (ch1 II pin voltage is lower than the input detection voltage except soft-stare period), the timer circuit starts operating. And after 10 ms, all the outputs are latched to OFF.
- Common circuits (such as the internal power supply block, and oscillator, etc.) continue operating.

(3) Cancelling short-circuit protection
- To reset the latch circuit, either change the level of the SHDNB1 pin and SHDNB2 pin from high to low, or drop the level of the power supply voltage (AV_{DD}) to the operation stop voltage of the under voltage lockout circuit (2.8 V).

Thermal Shutdown Circuit (Timer Latch Type)

After overheating has been detected (shutdown temperature: 150°C or higher), the timer circuit starts operating (as same as SCP). And after 10 ms, all the outputs are latched to OFF. Common circuits (such as the internal power supply block, and oscillator, etc.) continue operating.

When the thermal shutdown circuit is operating, either change the level of the SHDNB1 pin and SHDNB2 pin from high to low, or drop the level of the power supply voltage (AV_{DD}) to the operation stop voltage of the under voltage lockout circuit (2.8 V).

When ultra low-power mode, this circuits DOES NOT operate.

Under Voltage Lockout Circuit (Auto Recovery Type)

(1) Under voltage lockout operation
When the power supply voltage (AV_{DD}) falls to the operation stop voltage (2.8 V), output from all channels stops. Common circuits (such as the internal power supply block, and oscillator, etc.) continue operating.
(2) Restoring output
Once AV_{DD} voltage is restored to the operation start voltage (2.9 V), the under voltage lockout operation is canceled and output automatically resumes. The output voltage cannot be restored while the under voltage lockout circuit is operating, not even by manipulating the SHDNB pin.
When ultra low-power mode, this circuits DOES NOT operate.

Current Limiting

Ch1 operates under the current control mode. If an overcurrent occurs, the current is limited on a pulse-by-pulse basis. If the current sensor detects an overcurrent, the current is limited and the switching operation of the Power MOSFET in the output stage stops until the next cycle.

When the ch1 current is limited, the output voltage drops. If the ch1 II pin voltage falls below the input detection voltage, the short-circuit protection circuit starts operating.

Reference data (Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} = 5.0 V)

Item		Symbol	Min	Typ	Max	unit	Measurement condition
Current limit value	ch1 Current limet 1	I_{LIM1_1}	—	4.5	—	A	ch1OUT 3.3V
	ch1 Current limet 2	I_{LIM1_2}	—	4.5	—	A	ch1OUT 1.2V

Note: These data are for reference and not guaranteed as specifications.

Reverse Current Protection (ch1)

Ch1 have a reverse current protection circuit. When the bottom of inductor current is under ground, low-side N-ch MOSFET of output block is stopped, and ch1 operate as diode rectification. So, consumption current at light load can be reduced.

Over Current Protection (ch2)

Ch2 have a fold back type current protection circuit. If over current occur, protection operation is started and load current is limited (output short-circuit current: 100 mA).
Peak output current depend on output voltage. When VPIN2=5V and VOUT2=3.3V,.it is over 550mA.

When ultra low-power mode, this circuits DOES NOT operate.