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ML620Q150A Series User's Manual

16-bit Microcontroller

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Preface

This manual describes the operation of the hardware of the 16-bit microcontroller ML620Q150A Series.

The following manuals are also available. Read them as necessary.

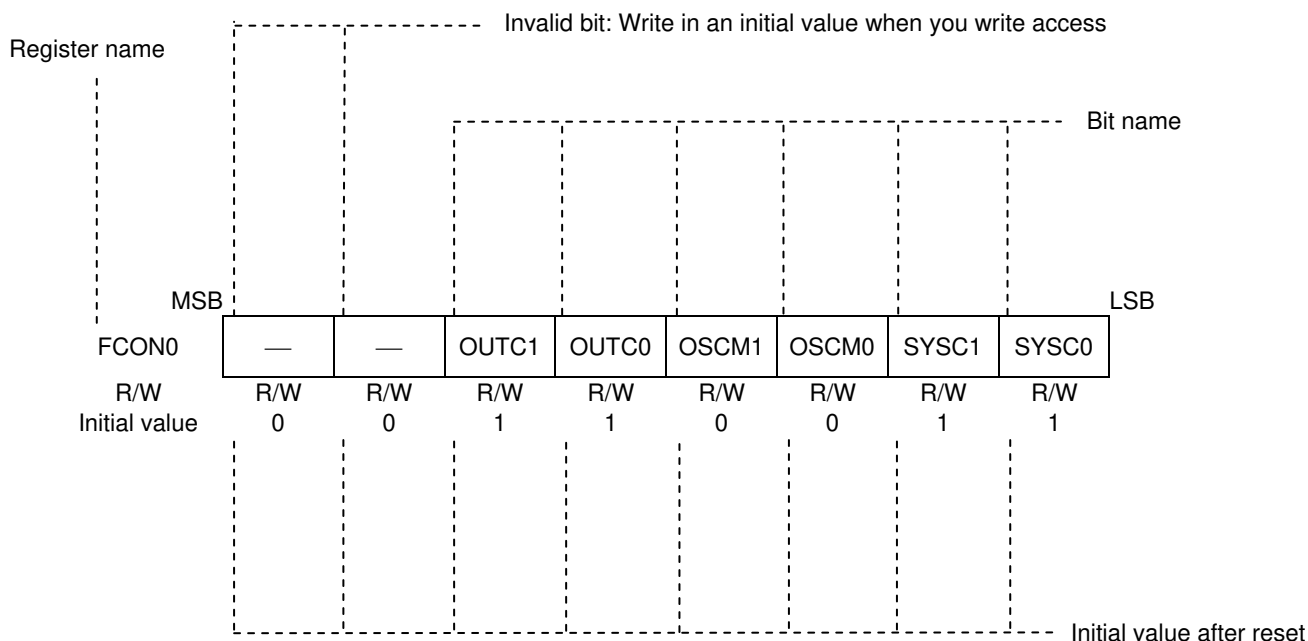
- nX-U16/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U16/100 Core.
- MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.
- CCU8 User's Manual
Description on the method of operating the compiler.
- CCU8 Programming Guide
Description on the method of programming.
- CCU8 Language Reference
Description on the language specifications.
- DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.
- IDEU8 User's Manual
Description on the integrated development environment IDEU8.
- uEASE User's Manual
Description on the on-chip debug tool uEASE.
- uEASE connection Manual
Description about the connection between uEASE.
- FWuEASE Flash Writer Host Program User's Manual
Description on the Flash Writer host program.

Notation

Classification	Notation	Description
◆ Numeric value	xxh, xxH xxb	Indicates a hexadecimal number. x: Any value in the range of 0 to F Indicates a binary number; “b” may be omitted. x: A value 0 or 1
◆ Unit	word, W byte, B nibble, N mega-, M kilo-, K kilo-, k milli-, m micro-, μ nano-, n second, s (lower case)	1 word = 16 bits 1 byte = 8 bits 1 nibble = 4 bits 10^6 $2^{10} = 1024$ $10^3 = 1000$ 10^{-3} 10^{-6} 10^{-9} second
◆ Terminology	“H” level, “1” level “L” level, “0” level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics. Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

◆ Register description

R/W: Indicates that Read/Write attribute. “R” indicates that data can be read and “W” indicates that data can be written. “R/W” indicates that data can be read or written.



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Chapter 1 Overview

1. Overview

1.1 Features

This LSI is a high-performance 16-bit CMOS microcontroller into which rich peripheral circuits, such as 10-bit A/D converter, timer, PWM, synchronous serial port, UART, I2C bus interface (master), Low level detect circuit, are incorporated around 16-bit CPU nX-U16/100.

The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. and, this LSI has a data flash-memory fill area by a software which can be written in. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

- CPU
 - 16-bit RISC CPU (CPU name: nX-U16/100)
 - Instruction system: 16-bit instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-Chip debug function
 - Minimum instruction execution time
 - Approx 30.5 s (at 32.768kHz system clock)
 - Approx 0.122s (at 8.192MHz system clock)

- Internal memory
 - Flash-memory

Product	Program area	Rewrite cycle
ML620Q151A/ML620Q154A/ML620Q157A	32-Kbyte* (16K × 16-bit)	100
ML620Q152A/ML620Q155A/ML620Q158A	48-Kbyte* (24K × 16-bit)	
ML620Q153A/ML620Q156A/ML620Q159A	64-Kbyte* (32K × 16-bit)	

* including unusable 1KByte TEST area

Internal 2-Kbyte Data Flash (1-Kbyte × 2) Rewrite cycle: 10,000 times

- SRAM: Internal 2-Kbyte RAM (2-Kbyte × 8 -bits)

- Interrupt controller
 - 2 non-maskable interrupt sources (Internal source: BACK-UP CLOCK, WDT)
 - maskable interrupt

Product	Interrupt source
ML620Q151A/ML620Q154A/ML620Q157A	27 (Internal source: 20, External source: 7)
ML620Q152A/ML620Q155A/ML620Q158A	28 (Internal source: 20, External source: 8)
ML620Q153A/ML620Q156A/ML620Q159A	28 (Internal source: 20, External source: 8)

- 4 steps of interrupt level, and a mask function

- Time base counter
 - Low-speed time base counter × 1 channel
- Watchdog timer
 - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
 - Free running
 - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s @32.768kHz)
- Timers
 - 8 bits x 2ch (16-bits configuration available x 1ch)
 - 16 bits x 4ch

- PWM
 - 16 bits x 4ch
 - The auto reload timer mode / PWM mode
 - Timer start-stop function by the software and an external trigger.
 - A pulse width can be measured using an external-trigger input.
 - An external event can be selected as the counter clock.
 - Complement synchronous PWM
- Synchronous serial port
 - 1ch
 - Master/slave selectable
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
- UART
 - Full-duplex x 1ch (Half-duplex x 2ch)
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- I2C bus interface
 - Master function only
 - Fast mode (400kbit/s), Standard mode (100kbit/s)
- Successive approximation type A/D converter
 - 10-bit A/D converter
 - Input: 12ch (Maximum)
 - Conversion time: 43us, 13.5 s per channel (conversion-time is selectable)
- Analog Comparator
 - 1ch
 - Edge for the interrupt and sampling function is selectable.
- General-purpose ports (including multiple functions)
 - Input-only ports

Product	Input-only ports (including multiple functions)	
	When not using the crystal resonator	When using the crystal resonator
ML620Q151A/ML620Q152A/ML620Q153A	6ch	5ch
ML620Q154A/ML620Q155A/ML620Q156A	7ch	6ch
ML620Q157A/ML620Q158A/ML620Q159A	7ch	6ch

- Output-only ports : 4ch
- Input/output ports

Product	Input/output ports (including multiple functions)	
	When not using the crystal resonator	When using the crystal resonator
ML620Q151A/ML620Q152A/ML620Q153A	31ch	30ch
ML620Q154A/ML620Q155A/ML620Q156A	34ch	33ch
ML620Q157A/ML620Q158A/ML620Q159A	46ch	45ch

- Reset
 - Reset through the RESET_N pin
 - Power-on reset generation when powered on
 - Reset by the watchdog timer (WDT) overflow
 - Reset by the Low Level Detector (LLD)
- LLD(Low Level Detector) function
 - Threshold voltages: 4values (1.9V/2.55V/3.7V/4.2V)
 - A threshold voltage is selected as Code-Option.
 - LLD is a ready as a supply-voltage supervisory reset.
 - Reset or an interrupt output is selectable as Code-Option.

- Clock
 - Low-speed clock (This LSI can not guarantee the operation without low-speed clock)
 - Crystal oscillation (32.768 kHz) or Built-in RC oscillation (32.768kHz)
 - Crystal oscillation or Built-in RC oscillation is selectable as Code-Option.
 - High-speed clock
 - Built-in RC oscillation (2.097MHz) or Built-in PLL oscillation (8.192MHz)
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
 - Block control function: Operation of an intact functional block circuit is powered down. (register reset and clock stop)

- Package

Product	Package
ML620Q151A/ML620Q152A/ML620Q153A	48pinTQFP (P-TQFP48-0707-0.50-QK)
ML620Q154A/ML620Q155A/ML620Q156A	52pinTQFP (P-TQFP52-1010-0.65-TK)
ML620Q157A/ML620Q158A/ML620Q159A	64pinQFP (P-QFP64-1414-0.80-UK)

- Guaranteed operating range
 - Operating temperature: -40°C to $+105^{\circ}\text{C}$
 - Operating voltage: $V_{DD} = 1.8\text{V}$ to 5.5V

The difference point of this LSI is shown below.

function	ML620Q151A/152A/153A	ML620Q154A/155A/156A	ML620Q157A/158A/159A
Shipment	48pinTQFP	52pinTQFP	64pinQFP
flash capacity (program area)	32Kbyte(ML620Q151A) 48Kbyte(ML620Q152A) 52Kbyte(ML620Q153A)	32Kbyte(ML620Q154A) 48Kbyte(ML620Q155A) 52Kbyte(ML620Q156A)	32Kbyte(ML620Q157A) 48Kbyte(ML620Q158A) 52Kbyte(ML620Q159A)
maskable interrupt	27	28	28
Input-only port (At the case of crystal unused)	6	7	7
P05 port	–	Available	Available
Input/output port (At the case of crystal unused)	31	34	46
P36,P53,P64 ports	–	Available	Available
P37 port	–	–	Available
P50~P52 ports	–	–	Available
P65~P67 ports	–	–	Available
P70~P74 ports	–	–	Available

– :none

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML620Q151A/ML620Q152A/ML620Q153A(TQFP48)

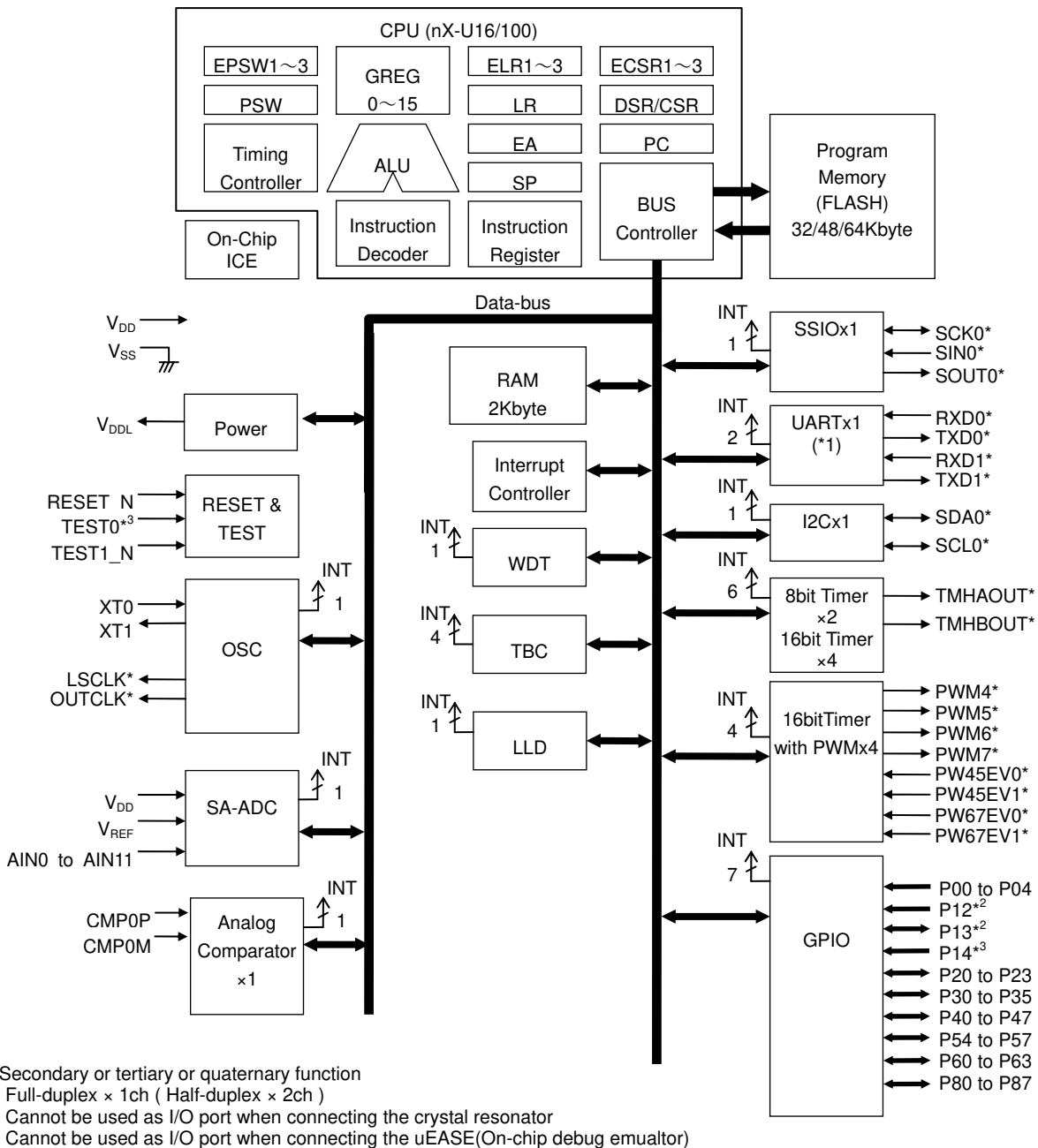


Figure 1-1 Block Diagram of ML620Q151A/ML620Q152A/ML620Q153A(TQFP48)

1.2.2 Block Diagram of ML620Q154A/ML620Q155A/ML620Q156A(TQFP52)

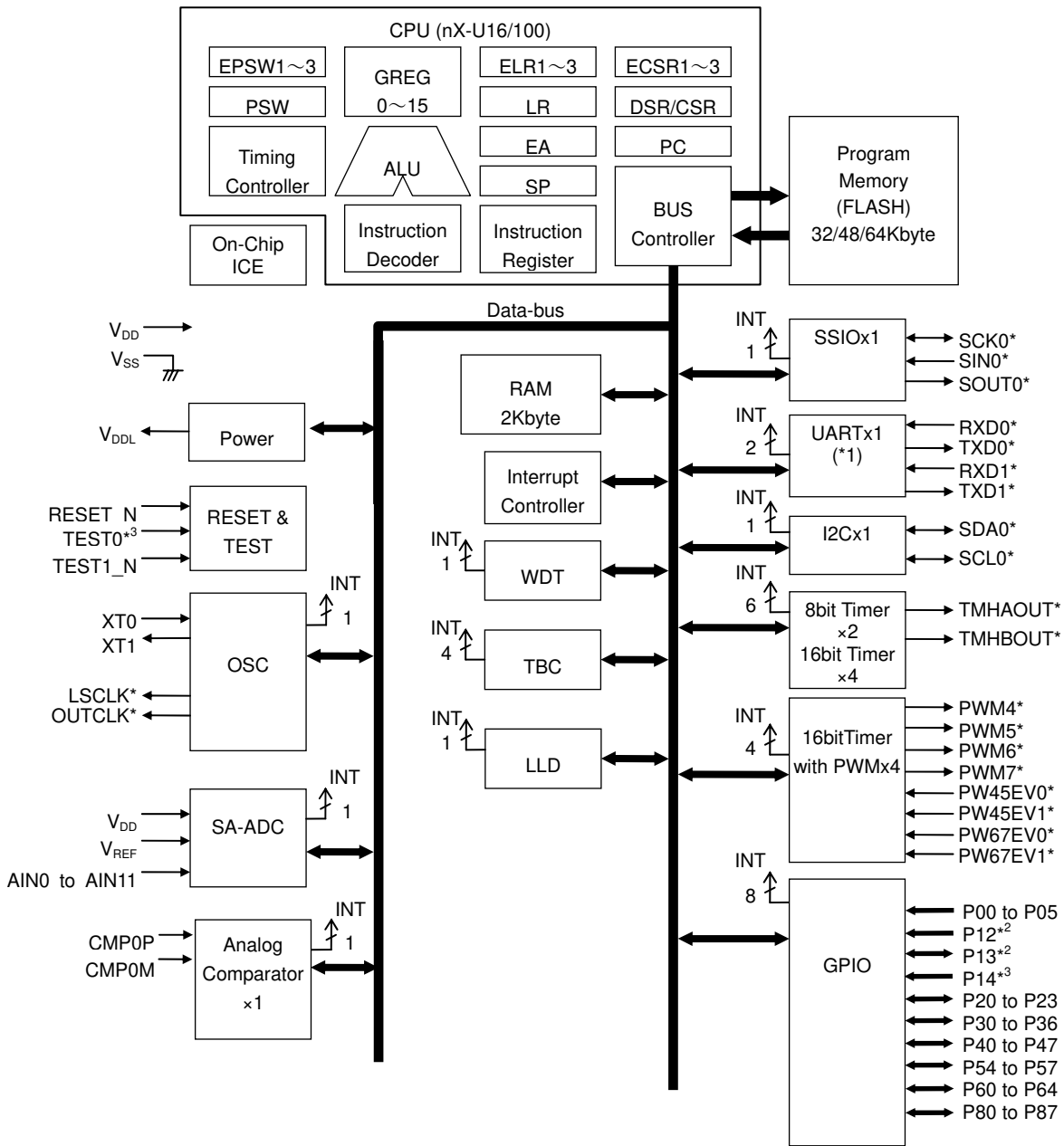


Figure 1-2 Block Diagram of ML620Q154A/ML620Q155A/ML620Q156A(TQFP52)

1.2.3 Block Diagram of ML620Q157A/ML620Q158A/ML620Q159A(QFP64)

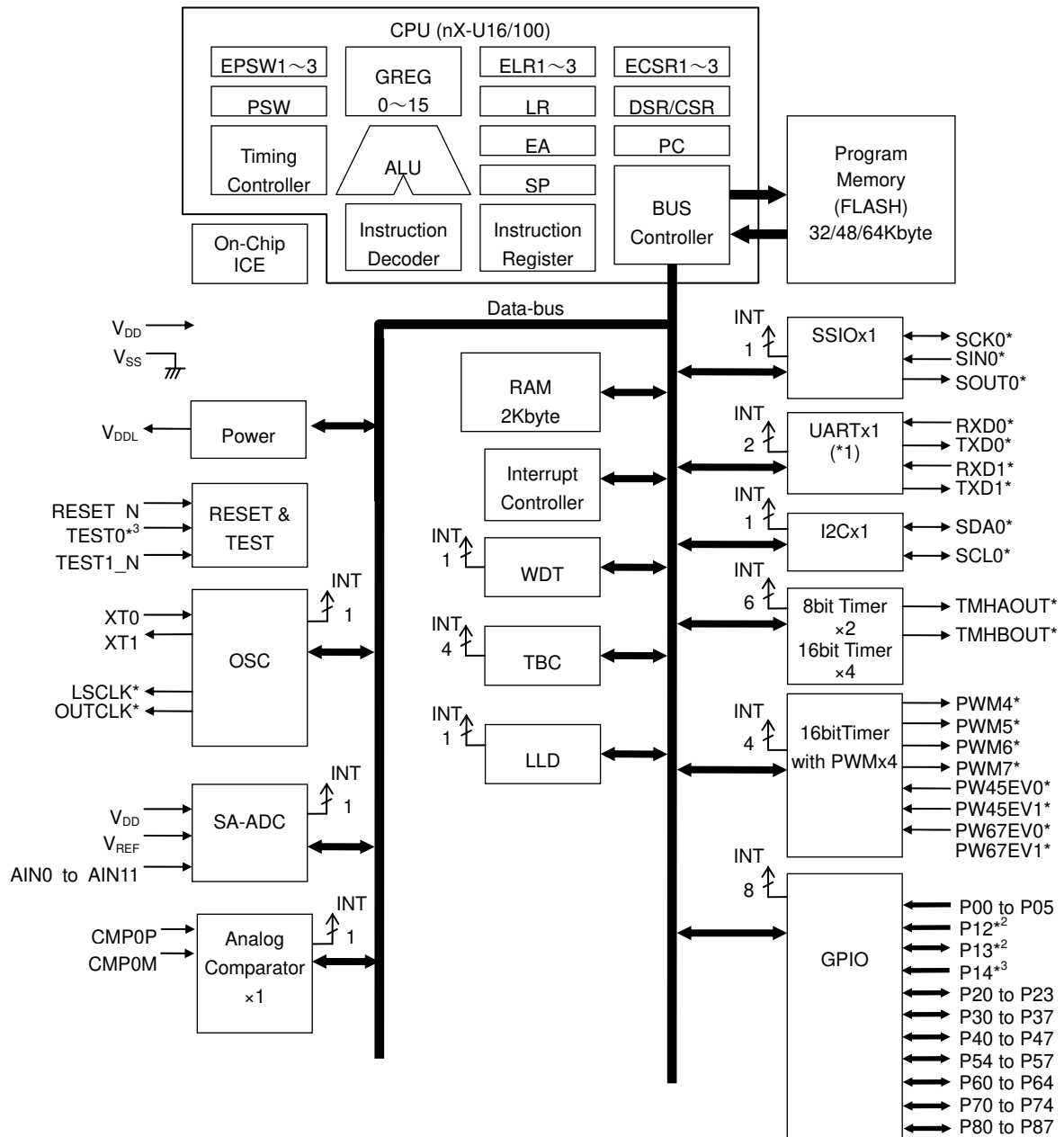


Figure 1-3 Block Diagram of ML620Q157A/ML620Q158A/ML620Q159A(QFP64)

1.3 Pins

1.3.1 Pin Layout

1.3.1.1 Pin Layout of ML620Q151A/ML620Q152A/ML620Q153A TQFP48 package product

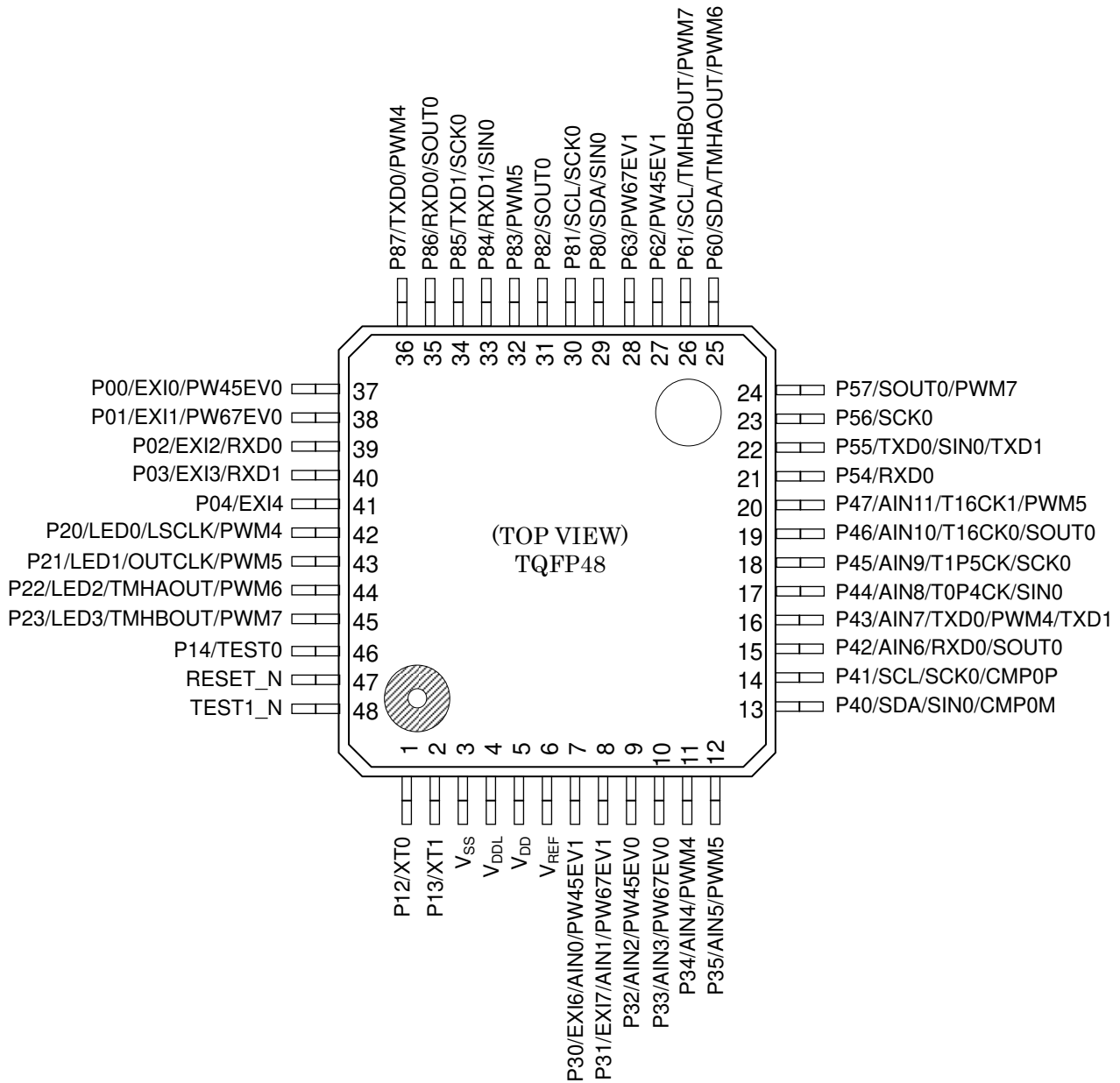


Figure 1-4 Pin Layout of ML620Q151A/ML620Q152A/ML620Q153A TQFP48 Package

1.3.1.2 Pin Layout of ML620Q154A/ML620Q155A/ML620Q156A TQFP52 package product

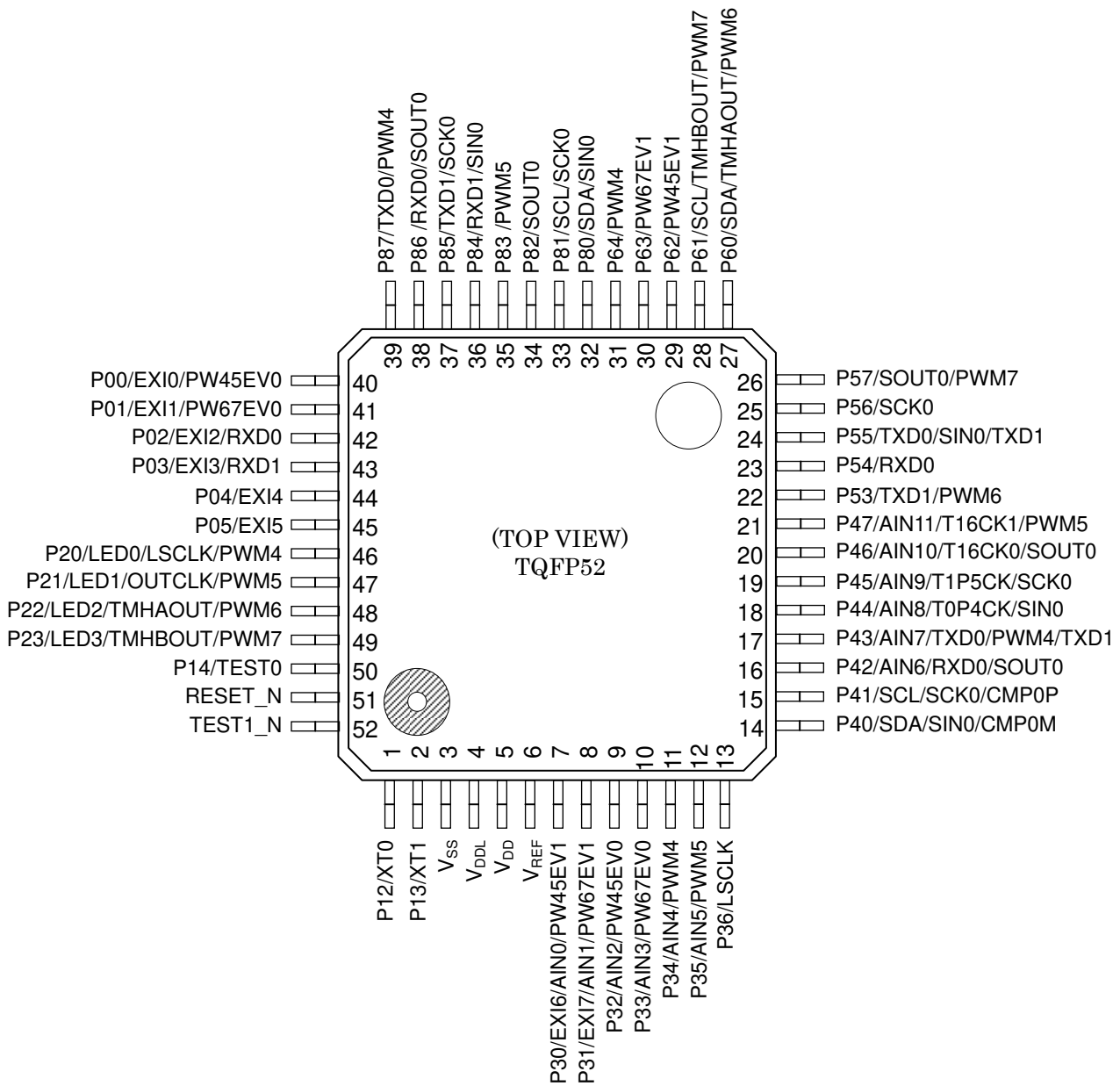


Figure 1-5 Pin Layout of ML620Q154A/ML620Q155A/ML620Q156A TQFP52 Package