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FEUL620Q504H-01

ML620Q503H/Q504H
User's Manual

Issue Date: Aug.31, 2015

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Preface

This manual describes the operation of the hardware of the 16-bit microcontroller ML620Q503H/Q504H.

The following manuals are also available. Read them as necessary.

■ nX-U16/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U16/100 Core.

■ MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

■ CCU8 User's Manual
Description on the method of operating the compiler.

■ CCU8 Programming Guide
Description on the method of programming.

■ CCU8 Language Reference
Description on the language specifications.

■ DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.

■ IDEU8 User's Manual
Description on the integrated development environment IDEU8.

■ uEASE User's Manual
Description on the on-chip debug tool uEASE.

■ uEASE connection Manual
Description about the connection between uEASE and ML620Q503H/Q504H.

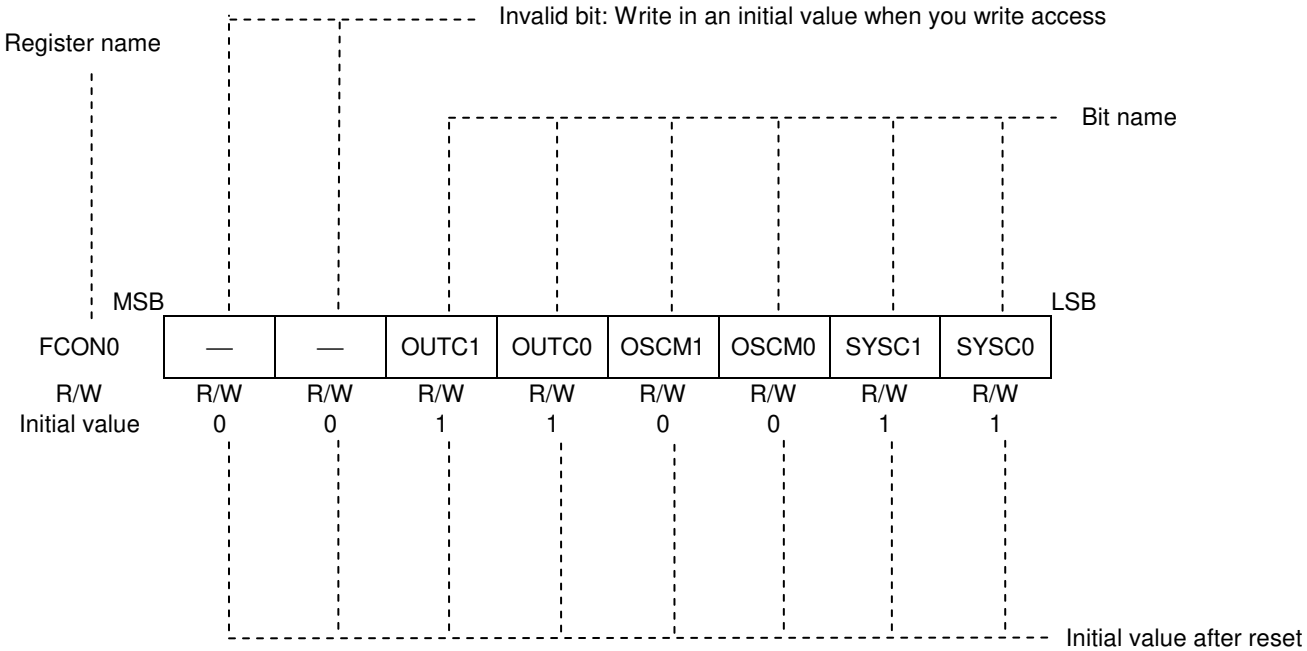
■ FWuEASE Flash Writer Host Program User's Manual
Description on the Flash Writer host program.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.



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Chapter 1

Overview

1. Overview

1.1 Features

This LSI family is a high-performance 16-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface (master), supply voltage level detect circuit, RC oscillation type A/D converter, and successive approximation type A/D converter are incorporated around 16-bit CPU nX-U16/100.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) is most suitable for battery-driven applications. And, this LSI has a data flash-memory fill area by a software which can be written in.
The on-chip debug function that is installed enables program debugging and programming.

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Build-in On-Chip debug function
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    62.5ns (@16 MHz system clock)

- Built-in coprocessor for multiplication, division, and multiply-accumulate operations
  - Signed or unsigned operation setting
  - Multiplication: 16bit × 16bit (operation time 4 cycles)
  - Division: 32bit / 16bit (operation time 8 cycles)
  - Division: 32bit / 32bit (operation time 16 cycles)
  - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time 4 cycles)
  - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time 4 cycles)

- Internal memory
  - Supports ISP function (re-writing the program memory area by software)
  - Number of segments

Product name	Flash memory		SRAM
	Program area*	Data area	
ML620Q503H	32KB (16K×16bit)	2KB(1K×16bit)	2KB(1K×16bit)
ML620Q504H	64KB (32K×16bit)	2KB(1K×16bit)	6KB(3K×16bit)

*: including 1KB of unusable test area

- Interrupt controller (INTC)
  - 1 non-maskable interrupt sources (Internal source: 1)
  - 37 maskable interrupt sources (Internal sources: 29, External sources: 8)
  - Software interrupt (SWI): maximum 64 sources
  - External interrupts and comparator allow edge selection and sampling selection
  - Priority level (4-level) can be set for each interrupt

- Time base counter (TBC)
  - Low-speed time base counter × 1 channel

- Timers (TMR)
  – 8 bits × 8 channels
    (Timer0-7: 16-bit × 4 configuration available by using Timer0-1 or Timer2-3, Timer4-5, Timer6-7)
  – Selection of one shot timer mode is possible
  – External clock can be selected as timer clock.

- Function Timers (FTM)
  – 16-bit × 4 channels
  – Equipped with the timer/capture/PWM functions using a 16-bit counter
  – Timer start/stop function by software/event trigger(external pin or other timer)
  – External pin can be selected as counter clock
  – Capture function (the measurement such as the pulse width is possible using external trigger input)
  – Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output.

- Watchdog timer (WDT)
  – Non-maskable interrupt and reset
  – Free running
  – Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)

- Synchronous serial port (SSIOF/ SSIO)
  – without FIFOs (SSIO) : 1 channel
  – with 4-byte transmits and receives FIFOs (SSIOF) : 1 channel
  – Master/slave are selectable
  – LSB first/MSB first are selectable
  – 8-bit length/16-bit length are selectable
  – Phase/Polarity of clock are selectable
  – supports slave-select signal (only SSIOF)

- UART (UARTF/ UART)
  – without FIFOs (UART) : 1ch
  – with 4-byte transmits and receives FIFOs (UARTF) : 1ch
  – Full duplex buffer system
  – Communication speed: Settable within the range of 2400bps to 115200bps.
  – Programmable interface (data length, parity, stop bits are selectable)

- I^2C bus interface (I^2C)
  – Master function × 2 channel
  – Fast mode (400 kbps), standard mode (100 kbps)

- General-purpose ports (PORT)
  – Input port x 2, Input/output port × 36 channels

- Melody driver (MELODY)
  – Tempo: 15 types
  – Scale: 29 types (Melody sound frequency: 508 Hz to 10.922 kHz)
  – Tone length: 63 types
  – Buzzer output mode (4 output modes, 8 buzzer frequencies, 7duty levels at 4.096kHz/15 duty levels at other buzzer frequencies)

- RC oscillation type A/D converter (RC-ADC)
  – Time division × 2 channels
  – 24-bit counter

- Successive approximation type A/D converter (SA-ADC)
  - Input × 12 channels
  - 12-bit A/D converter
  - Starting by trigger of Timer/FTM function.
  - Capacitive touch sense function

- Analog Comparator (CMP)
  - Input × 2 ch
  - Common mode input voltage: 0.2V to V_{DD} - 0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection are selectable

- Voltage Level Supervisor (VLS)
  - Threshold voltages: selectable from 13 levels
  - interrupt or reset generate are selectable

- Low Level Detector(LLD)
  - Judgment Voltage: 1.8V±0.2V
  - Usable as low level detection reset

- Reset
  - Reset by the RESET_N pin
  - Reset by power-on detection
  - Reset by overflow of watchdog timer (WDT)
  - Reset by Voltage Level Supervisor(VLS)
  - Reset by Low Level Detector(LLD)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
    - Crystal oscillation (32.768 kHz)
    - External clock input (30kHz to 36kHz)
    - Built-in RC oscillation (32.768kHz)
  - High-speed clock:
    - Crystal/Ceramic oscillation (16 MHz)
    - External clock input (2MHz to 16 MHz)
    - Built-in RC oscillation (16MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
  - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits can keep in operating states.
  - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8,1/16,1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - Die *Please contact our responsible sales person for the pad layout information.
  - 48-pin plastic TQFP
    Tray
    ML620Q503H-xxxTBWAAL
    ML620Q504H-xxxTBWAAL

    Tape and Reel
    ML620Q503H-xxxTBWABL
    ML620Q504H-xxxTBWABL

- Guaranteed operating range
  - Operating temperature (ambient) : –40°C to +85°C
  - Operating voltage: V_{DD} = 1.8V to 5.5V

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML620Q503H/Q504H

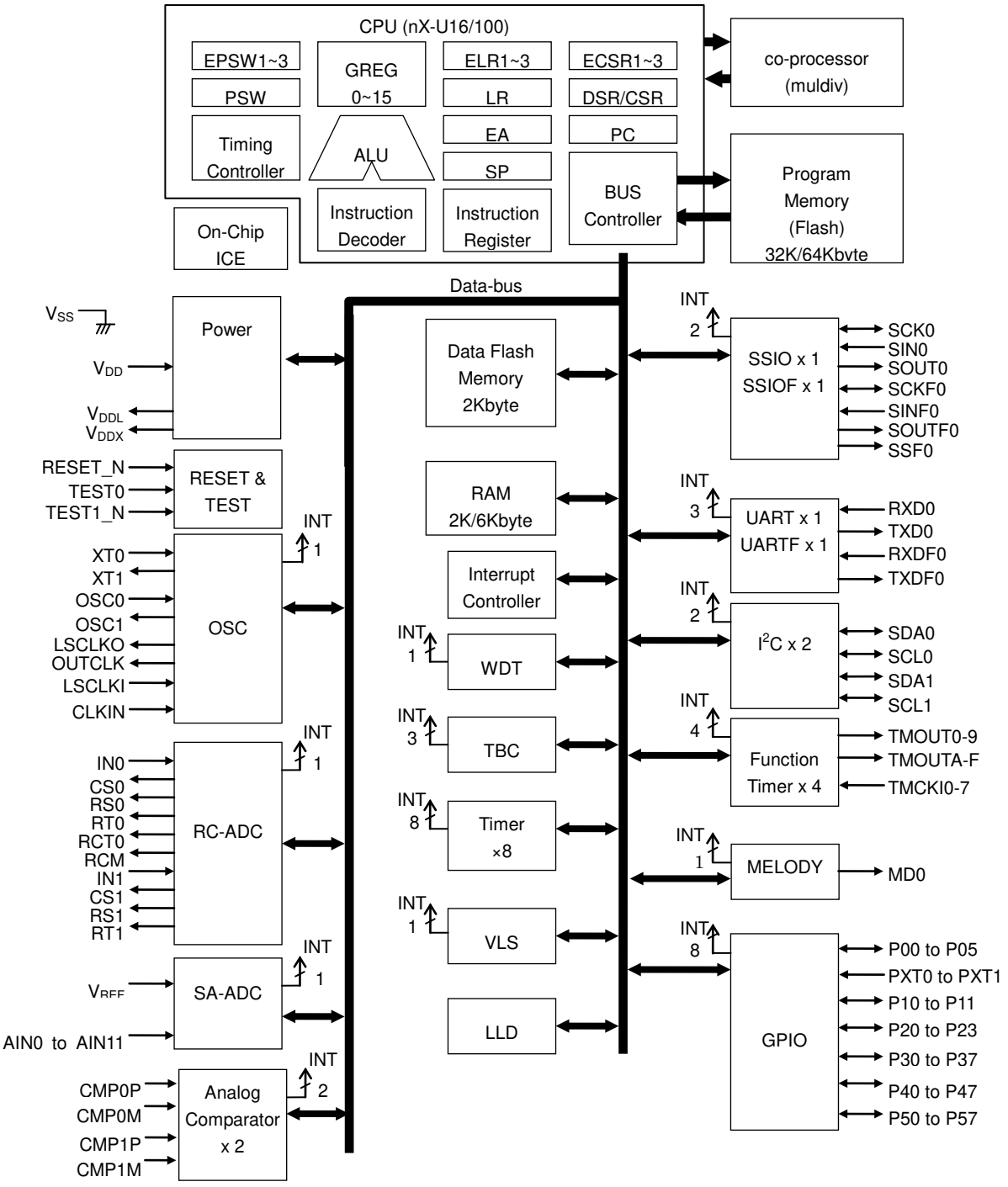
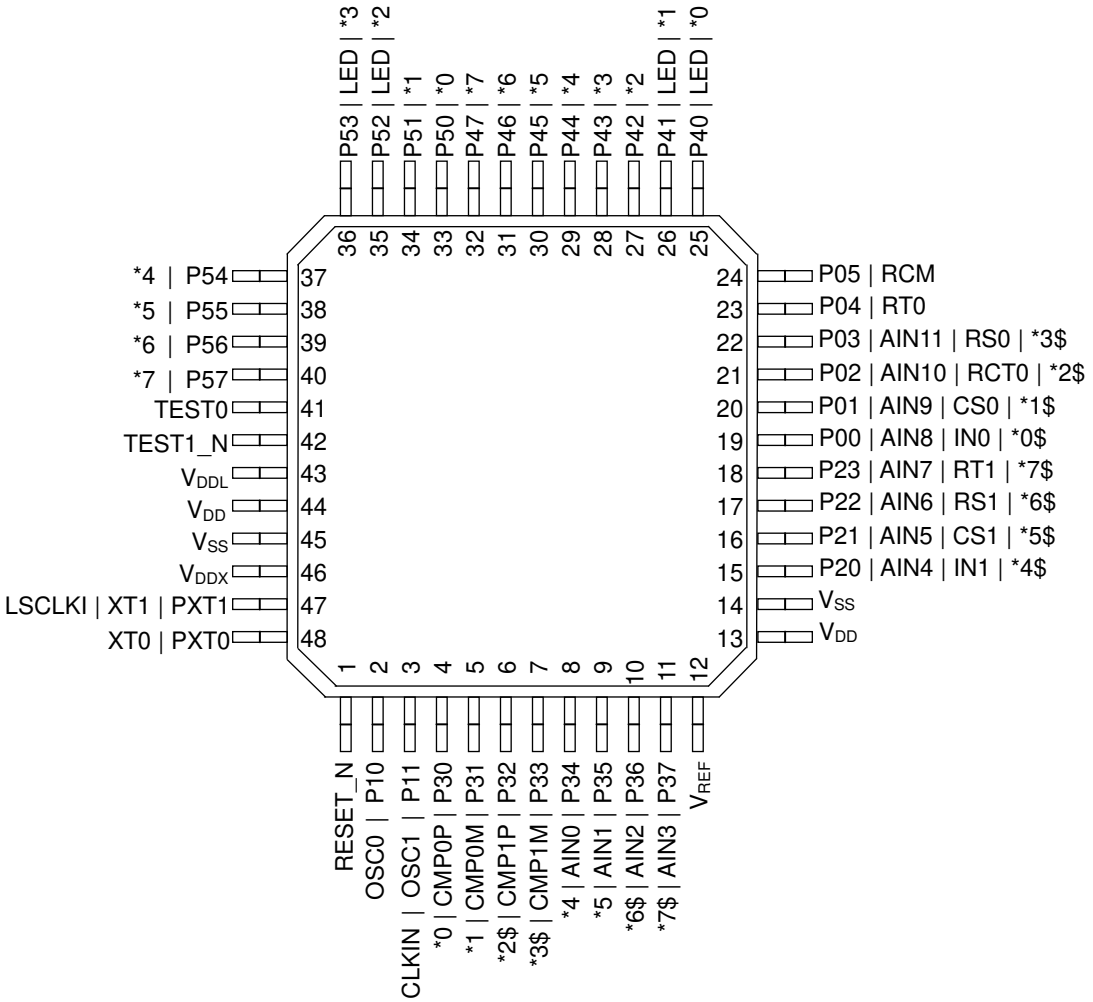


Figure 1-1 Block Diagram of ML620Q503H/Q504H

1.3 Pins

1.3.1 Pin Layout

1.3.1.1 Pin Layout of ML620Q503H/Q504H TQFP Package



External interrupt input pin(EXI) can be assigned to P00-P05, PXT0-1, P20-P57.
*0 to *7 and *0$ to *7$ has following functions. But 0-7 has limited function. Please refer to the pin list.

*0 : SDA0, SOUT0, RXD0	*4 : SDA1, SOUTF0, RXDF0
*1 : SCL0, SIN0 , TXD0	*5 : SCL1, SINF0, TXDF0
*2 : SCK0, TMOUT ,TMCKI	*6 : LSCLKO,SCKF0, TMOUT, TMCKI
*3 : MD0, TMOUT , TMCKI	*7 : OUTCLK,SSF0, TMOUT, TMCKI
*0$: SOUT0, RXD0	*4$: SOUTF0, RXDF0
*1$: SIN0, TXD0	*5$: SINF0, TXDF0
*2$: SCK0, TMOUT	*6$: SCKF0, TMOUT
*3$: MD0(P33 only), TMOUT	*7$: SSF0, TMOUT

Figure 1-2 Pin Layout of ML620Q503H/Q504H TQFP Package

1.3.2 List of Pins

1.3.2.1 List of Pins of ML620Q503H/Q504H TQFP Package

PKG Pin No.	1st Function				2nd/3rd/4th Function								
	Pin name	I/O	Reset State	Function	pin name	I/O	function	pin name	I/O	function	pin name	I/O	function
14, 45	V_{SS}	–	–	Negative power supply pin	–	–	–	–	–	–	–	–	–
13, 44	V_{DD}	–	–	Positive power supply pin	–	–	–	–	–	–	–	–	–
43	V_{DDL}	–	–	Power supply pin for internal circuit (internally generated)	–	–	–	–	–	–	–	–	–
46	V_{DDX}	–	–	Power supply pin for internal circuit (internally generated)	–	–	–	–	–	–	–	–	–
12	V_{REF}	–	–	Reference power supply pin of SA-ADC	–	–	–	–	–	–	–	–	–
1	RESET_N	I	Pull-up Input	Reset input pin	–	–	–	–	–	–	–	–	–
42	TEST1_N	I	Pull-up Input	Input pin for testing	–	–	–	–	–	–	–	–	–
41	TEST0	I/O	Pull-down Input	Input/output pin for testing	–	–	–	–	–	–	–	–	–
48	PXT0/ EXII0/ XT0	I	Input disable	Input port/ External interrupt/ Low-speed oscillation port	–	–	–	–	–	–	–	–	–
47	PXT1/ EXI1/ XT1/ LSCLKI	I/O	Hi-Z output	Input-Output port/ External interrupt/ Low-speed oscillation port Low-speed external clock input	–	–	–	–	–	–	–	–	–
19	P00/ EXI00/ AIN8	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	IN0	I	RC-ADC oscillation input	SOUT0	O	SSIO data output	RXD0	I	UART data input
20	P01/ EXI01/ AIN9	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	CS0	O	RC-ADC reference capacitance connection pin	SIN0	I	SSIO data input	TXD0	O	UART data output
21	P02/ EXI02/ AIN10	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	RCT0	O	RCADC resistor/capacitor sensor connection pin	SCK0	I/O	SSIO clock input/output	TMOUT0	O	FTM output
22	P03/ EXI03/ AIN11	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	RS0	O	RC-ADC reference resistor connection pin	–	–	–	TMOUT1	O	FTM output
23	P04/ EXI04	I/O	Hi-Z output	Input-Output port/ External interrupt	RT0	O	RC-ADC measurement resistor sensor connection pin	–	–	–	–	–	–
24	P05/ EXI05	I/O	Hi-Z output	Input-Output port/ External interrupt	RCM	O	RC-ADC oscillation monitor	–	–	–	–	–	–
2	P10/ OSC0	I/O	Hi-Z output	Input-Output port/ High-speed oscillation port	–	–	–	–	–	–	–	–	–
3	P11/ OSC1/ CLKIN	I/O	Hi-Z output	Input-Output port/ High-speed oscillation port High-speed external clock input	–	–	–	–	–	–	–	–	–
15	P20/ EXI20/ AIN4	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	IN1	I	RC-ADC oscillation input	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
16	P21/ EXI21/ AIN5	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	CS1	O	RC-ADC reference capacitance connection pin	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
17	P22/ EXI22/ AIN6	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	RS1	O	RC-ADC reference resistor connection pin	SCKF0	I/O	SSIOF clock input/output	TMOUT2	O	FTM output
18	P23/ EXI23/ AIN7	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	RT1	O	RC-ADC measurement resistor sensor connection pin	SSF0	I/O	SSIOF select input/output	TMOUT3	O	FTM output
4	P30/ EXI30/ CMP0P	I/O	Hi-Z output	Input-Output port/ External interrupt/ Comparator plus input	SDA0	I/O	I^2C data input/output	SOUT0	O	SSIO data output	RXD0	I	UART data input

PKG Pin No.	1st Function				2nd/3rd/4th Function								
	Pin name	I/O	Reset State	Function	pin name	I/O	function	pin name	I/O	function	pin name	I/O	function
5	P31/ EXI31/ CMP0 M	I/O	Hi-Z output	Input-Output port/ External interrupt/ Comparator minus input	SCL0	O	I²C clock output	SIN0	I	SSIO data input	TXD0	O	UART data output
6	P32/ EXI32/ CMP1 P	I/O	Hi-Z output	Input-Output port/ External interrupt/ Comparator plus input	–	–	–	SCK0	I/O	SSIO clock input/output	TMOUT4	O	FTM output
7	P33/ EXI33/ CMP1 M	I/O	Hi-Z output	Input-Output port/ External interrupt/ Comparator minus input	MD0	O	Melody/Buzzer output	–	–	–	TMOUT5	O	FTM output
8	P34/ EXI34/ AIN0	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	SDA1	I/O	I²C data input/output	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
9	P35/ EXI35/ AIN1	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	SCL1	O	I²C clock output	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
10	P36/ EXI36/ AIN2	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	–	–	–	SCKF0	I/O	SSIOF clock input/output	TMOUT6	O	FTM output
11	P37/ EXI37/ AIN3	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	–	–	–	SSF0	I/O	SSIOF select input/output	TMOUT7	O	FTM output
25	P40/ EXI40/ LED	I/O	Hi-Z output	Input-Output port/ External interrupt/ LED output	SDA0	I/O	I²C data input/output	SOUT0	O	SSIO data output	RXD0	I	UART data input
26	P41/ EXI41/ LED	I/O	Hi-Z output	Input-Output port/ External interrupt/ LED output	SCL0	O	I²C clock output	SIN0	I	SSIO data input	TXD0	O	UART data output
27	P42/ EXI42/ TMCKI 0	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	–	–	–	SCK0	I/O	SSIO clock input/output	TMOUT8	O	FTM output
28	P43/ EXI43/ TMCKI 1	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	MD0	O	Melody/Buzzer output	–	–	–	TMOUT9	O	FTM output
29	P44/ EXI44	I/O	Hi-Z output	Input-Output port/ External interrupt	SDA1	I/O	I²C data input/output	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
30	P45/ EXI45	I/O	Hi-Z output	Input-Output port/ External interrupt	SCL1	O	I²C clock output	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
31	P46/ EXI46/ TMCKI 2	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	LSCLKO	O	Low-speed clock output	SCKF0	I/O	SSIOF clock input/output	TMOUTA	O	FTM output
32	P47/ EXI47/ TMCKI 3	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	OUTCLK	O	High-speed clock output	SSF0	I/O	SSIOF select input/output	TMOUTB	O	FTM output
33	P50/ EXI50	I/O	Hi-Z output	Input-Output port/ External interrupt	SDA0	I/O	I²C data input/output	SOUT0	O	SSIO data output	RXD0	I	UART data input
34	P51/ EXI51	I/O	Hi-Z output	Input-Output port/ External interrupt	SCL0	O	I²C clock output	SIN0	I	SSIO data input	TXD0	O	UART data output
35	P52/ EXI52/ TMCKI 4/ LED	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input/ LED output	–	–	–	SCK0	I/O	SSIO clock input/output	TMOUTC	O	FTM output
36	P53/ EXI53/ TMCKI 5/ LED	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input/ LED output	MD0	O	Melody/Buzzer output	–	–	–	TMOUTD	O	FTM output
37	P54/ EXI54	I/O	Hi-Z output	Input-Output port/ External interrupt	SDA1	I/O	I²C data input/output	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
38	P55/ EXI55	I/O	Hi-Z output	Input-Output port/ External interrupt	SCL1	O	I²C clock output	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
39	P56/ EXI56/ TMCKI 6	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	LSCLKO	O	Low-speed clock output	SCKF0	I/O	SSIOF clock input/output	TMOUTE	O	FTM output