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Parallel NOR Flash Embedded Memory

JR28F032M29EWXX; PZ28F032M29EWXX; JS28F064M29EWXX
PC28F064M29EWXX; JR28F064M29EWXX; PZ28F064M29EWXX
JS28F128M29EWXX; PC28F128M29EWXX; RC28F128M29EWXX

Features

- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65–3.6V (I/O buffers)
- Asynchronous random or page read
  - Page size: 8 words or 16 bytes
  - Page access: 25ns
  - Random access (V_{CCQ} = 2.7–3.6V): 60ns (BGA); 70ns (TSOP)
- Buffer program: 256-word MAX program buffer
- Program time
  - 0.56µs per byte (1.8 MB/s TYP when using 256-word buffer size in buffer program without V_{PPH})
  - 0.31µs per byte (3.2 MB/s TYP when using 256-word buffer size in buffer program with V_{PPH})
- Memory organization
  - 32Mb: 64 main blocks, 64KB each, or eight 8KB boot blocks (top or bottom) and 63 main blocks, 64KB each
  - 64Mb: 128 main blocks, 64KB each, or eight 8KB boot blocks (top or bottom) and 127 main blocks, 64 KB each
  - 128Mb: 128 main blocks, 128KB each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/erase suspend and resume capability
  - READ operation on another block during a PROGRAM SUSPEND operation
  - READ or PROGRAM operation on one block during an ERASE SUSPEND operation on another block
- BLANK CHECK operation to verify an erased block
- Unlock bypass, block erase, chip erase, and write to buffer capability
  - Fast buffered/batch programming
  - Fast block and chip erase
- V_{PP}/WP# pin protection
  - V_{PPH} voltage on V_{PP} to accelerate programming performance
  - Protects highest/lowest block (H/L uniform) or top/bottom two blocks (T/B boot)
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
  - Password access
- Extended memory block
  - 128-word (256-byte) block for permanent secure identification
  - Program or lock implemented at the factory or by the customer
- Low-power consumption: Standby mode
- JESD47H-compliant
  - 100,000 minimum ERASE cycles per block
  - Data retention: 20 years (TYP)
- 65nm single-bit cell process technology
- Packages (JEDEC-standard)
  - 56-pin TSOP (128Mb, 64Mb)
  - 48-pin TSOP (64Mb, 32Mb)
  - 64-ball FBGA (128Mb, 64Mb)
  - 48-ball BGA (64Mb, 32Mb)
- Green packages available
  - RoHS-compliant
  - Halogen-free
- Operating temperature
  - Ambient: –40°C to +85°C

Part Numbering Information

This product is available with the prelocked extended memory block. Devices are shipped from the factory with memory content bits erased to 1. For a list of available options, such as packages or high/low protection, or for further information, contact your Micron sales representative.

Table 1: Part Number Information

Part Number Category	Category Details
Package	JS = 56-pin TSOP, 14mm x 20mm, lead-free, halogen-free, RoHS-compliant
	PC = 64-ball Fortified BGA, 11mm x 13mm, lead-free, halogen-free, RoHS-compliant
	RC = 64-ball Fortified BGA, 11mm x 13mm, leaded
	JR = 48-pin TSOP, 12mm x 20mm, lead-free, halogen-free, RoHS-compliant
	PZ = 48-ball BGA, 6mm x 8mm, lead-free, halogen-free, RoHS-compliant
Product designator	28F = Parallel NOR interface
Density	128 = 128Mb
	064 = 64Mb
	032 = 32Mb
Device type	M29EW = Embedded Flash memory (3V core, page read)
Device function	H = Highest block protected by V_{PP}/WP#; uniform block
	L = Lowest block protected by V_{PP}/WP#; uniform block
	B = Bottom boot; bottom two blocks protected by V_{PP}/WP#
	T = Top boot; top two blocks protected by V_{PP}/WP#
Features	A/B/F/X or an asterisk (*) = Combination of features, including packing media, security features, and specific customer request information

Valid M29EW Part Number Combinations

Table 2: Standard Part Numbers by Density, Medium, and Package

Density	Medium	Package				
		JS	PC	RC	JR	PZ
32Mb	Tray	–	–	–	JR28F032M29EWHA	PZ28F032M29EWHA
					JR28F032M29EWLA	PZ28F032M29EWLA
					JR28F032M29EWBA	PZ28F032M29EWBA
					JR28F032M29EWTA	PZ28F032M29EWTA
	Tape and reel	–	–	–	JR28F032M29EWBB	PZ28F032M29EWBB
					JR28F032M29EWTB	

Table 2: Standard Part Numbers by Density, Medium, and Package (Continued)

Density	Medium	Package				
		JS	PC	RC	JR	PZ
64Mb	Tray	JS28F064M29EWHA	PC28F064M29EWHA	–	JR28F064M29EWHA	PZ28F064M29EWHA
		JS28F064M29EWLA	PC28F064M29EWLA		JR28F064M29EWLA	PZ28F064M29EWLA
		JS28F064M29EWBA	PC28F064M29EWBA		JR28F064M29EWBA	PZ28F064M29EWBA
		JS28F064M29EWTA	PC28F064M29EWTA		JR28F064M29EWTA	PZ28F064M29EWTA
	Tape and reel	JS28F064M29EWLB	–	–	JR28F064M29EWHB	PZ28F064M29EWBB
					JR28F064M29EWLB	
					JR28F064M29EWTB	
128Mb	Tray	JS28F128M29EWHF	PC28F128M29EWHF	RC28F128M29EWHF	–	–
		JS28F128M29EWLA	PC28F128M29EWLA	RC28F128M29EWLA		
	Tape and reel	–	–	–	–	–

Table 3: Part Numbers with Security Features by Density, Medium, and Package

Density	Medium	Package	
		PC	PZ
64Mb	Tray	PC28F064M29EWHX	PZ28F064M29EWHX
		PC28F064M29EWLX	PZ28F064M29EWLX
		PC28F064M29EWBX	PZ28F064M29EWBX
		PC28F064M29EWTX	PZ28F064M29EWTX
	Tape and Reel	PC28F064M29EWTY	–
128Mb	Tray	PC28F128M29EWHX	–
		PC28F128M29EWLX	
	Tape and Reel	–	–

Note: 1. This data sheet covers only standard parts. For security parts, contact your local Micron sales representative.

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General Description

The M29EW is an asynchronous, parallel NOR Flash memory device manufactured on 65nm single-bit cell (SBC) technology. READ, ERASE, and PROGRAM operations are performed using a single low-voltage supply. Upon power-up, the device defaults to read array mode.

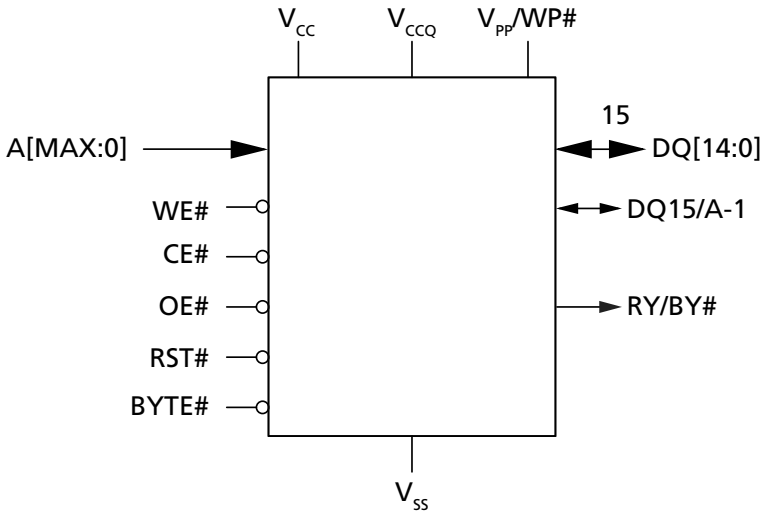
The main memory array is divided into uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

CE#, OE#, and WE# control the bus operation of the device and enable a simple connection to most microprocessors, often without additional logic.

The M29EW supports asynchronous random read and page read from all blocks of the array. It also features an internal program buffer that improves throughput by programming 256 words via one command sequence. The device contains a 128-word extended memory block which overlaps addresses with array block 0. The user can program this additional space and then protect it to permanently secure the contents. The device also features different levels of hardware and software protection to secure blocks from unwanted modification.

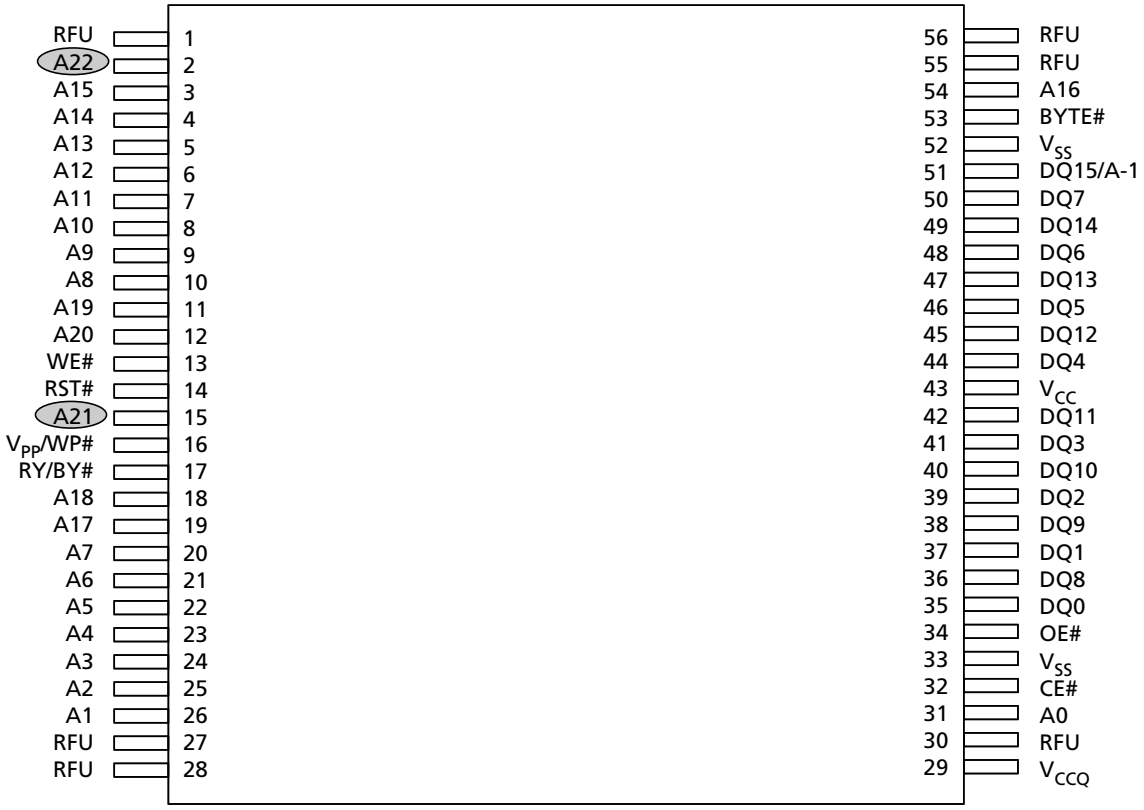
Refer to TN-13-30, System Design Considerations with Micron Flash Memory, for details on system design and V_{CC} and V_{CCQ} signals.

Figure 1: Logic Diagram



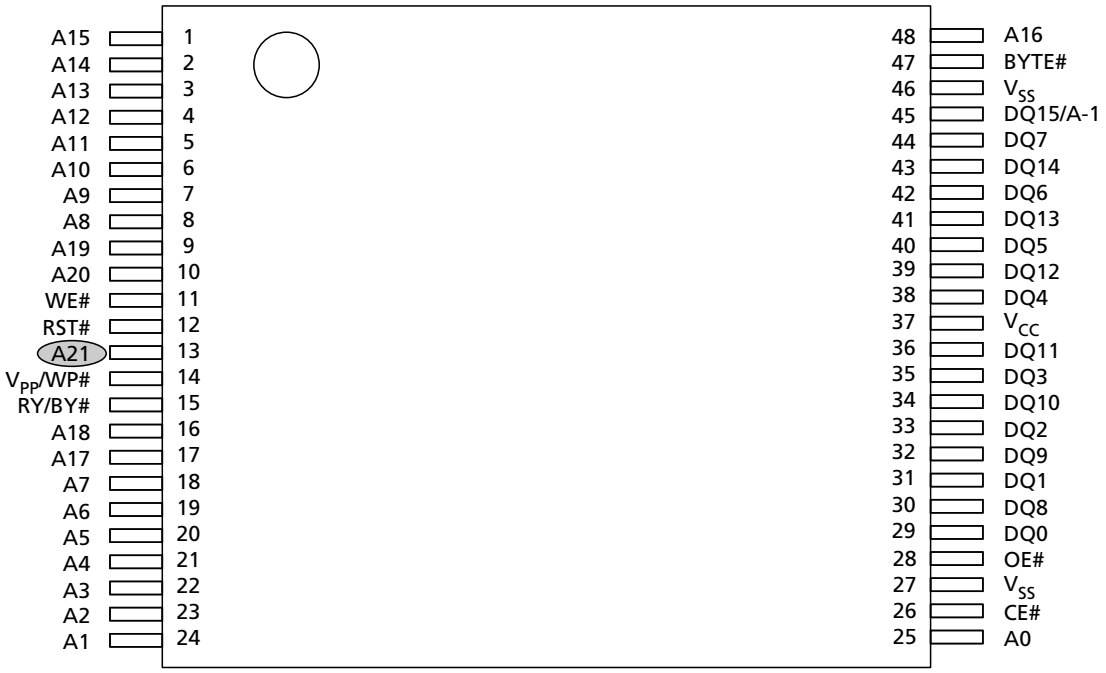
Signal Assignments

Figure 2: 56-Pin TSOP (Top View)



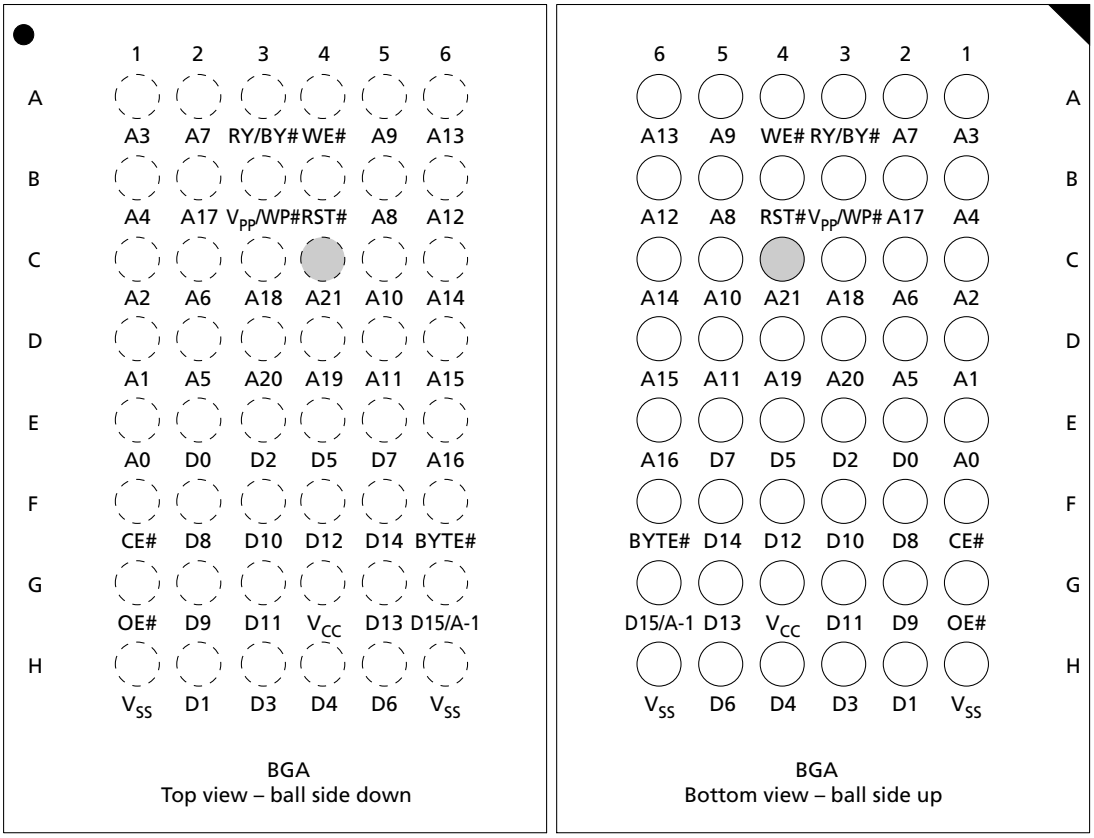
Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64Mb and above; otherwise, it is RFU.
3. A22 is valid for 128Mb and above; otherwise, it is RFU.
4. RFU = Reserved for future use.

Figure 3: 48-Pin TSOP (Top View)



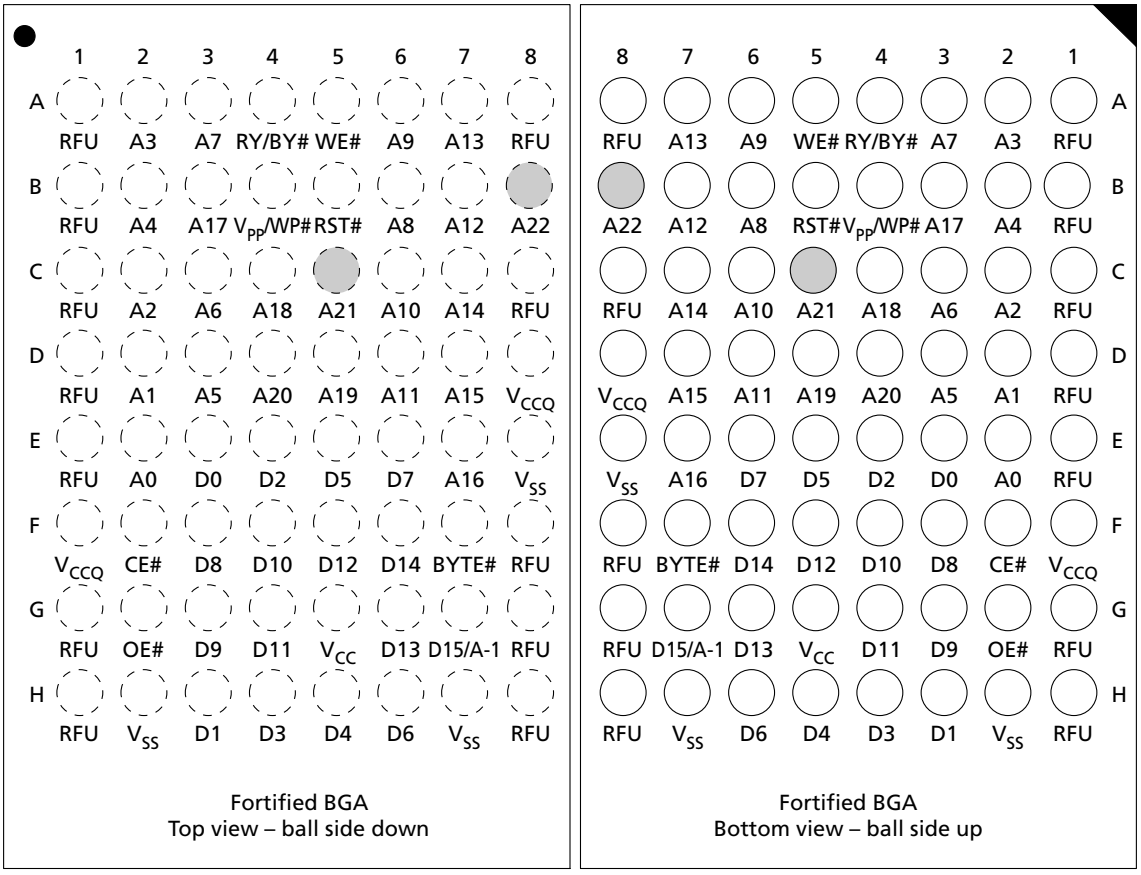
Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64Mb and above; otherwise, it is RFU.
3. For 48-Pin, there is no V_{CCQ} pin, V_{CC} also supply IO, it can only be 2.7V-3.6V
4. RFU = Reserved for future use.

Figure 4: 48-Ball BGA (Top and Bottom Views)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64Mb and above; otherwise, it is RFU.
3. For 48-Pin, there is no V_{CCQ} pin, V_{CC} also supply IO, it can only be 2.7V-3.6V
4. RFU = Reserved for future use.

Figure 5: 64-Ball Fortified BGA (Top and Bottom Views)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64Mb and above; otherwise, it is RFU.
3. A22 is valid for 128Mb and above; otherwise, it is RFU.
4. RFU = Reserved for future use.

Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 4: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby and data outputs are at High-Z.
OE#	Input	**Output enable:** Controls the bus READ operation.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the command interface.
V_{PP}/WP#	Input	**V_{PP}/Write Protect:** Provides WRITE PROTECT function and V_{PPH} function. These functions protect the lowest or highest block or top two blocks or bottom two blocks, enable the device to enter unlock bypass mode and accelerate program speed, respectively. (Refer to Hardware Protection, Bypass Operations, and Program Operations for details.) A 0.1µF capacitor should be connected between V_{PP}/WP# and V_{SS} to decouple the current surges from the power supply when V_{PPH} is applied. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operation when V_{PPH} is applied. (See DC Characteristics.)
BYTE#	Input	**Byte/word organization select:** Switches between x8 and x16 bus modes. When BYTE# is LOW, the device is in x8 mode; when HIGH, the device is in x16 mode.
RST#	Input	**Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}RHEL, whichever occurs last). See RESET AC Specifications for more details.
DQ[7:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine.
DQ[14:8]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During WRITE operations, these bits are not used. When reading the status register, these bits should be ignored.
DQ15/A-1	I/O	**Data I/O or address input:** When the device operates in x16 bus mode, this pin behaves as data I/O, together with DQ[14:8]. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Except where stated explicitly otherwise, DQ15 = data I/O (x16 mode); A-1 = address input (x8 mode).

Table 4: Signal Descriptions (Continued)

Name	Type	Description
RY/BY#	Output	**Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z. (See RESET AC Specifications for more details.) The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one (or more) of the devices is (are) busy. A 10K Ohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when V_{CC} <= V_{LKO}. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations. (See DC Characteristics.)
V_{CCQ}	Supply	**I/O supply voltage:** Provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

Memory Organization

Memory Configuration

The 32Mb device memory array (x8/x16) is divided into 63 main blocks (64KB each) and 8 top or bottom boot blocks (8KB each). It is also divided into 64 main uniform blocks (64KB each).

The 64Mb device memory array (x8/x16) is divided into 127 main blocks (64KB each) and 8 top or bottom boot blocks (8KB each). It is also divided into 128 main uniform blocks (64KB each).

The 128Mb device memory array (x8/x16) is divided into 128 main uniform blocks (128KB each).

Memory Map – 32Mb

Table 5: 32Mb Memory Map – x8 Top and Bottom Boot [70:0]

Block	Block Size	Address Range (x8 Top Boot)		Block	Block Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
70	8KB	003F E000	003F FFFF	70	64KB	003F 0000	003F FFFF
69		003F C000	003F DFFF	69		003E 0000	003E FFFF
68		003F A000	003F BFFF	68		003D 0000	003D FFFF
67		003F 8000	003F 9FFF	⋮	⋮	⋮	⋮
66		003F 6000	003F 7FFF	8	64KB	0001 0000	0001 FFFF
65		003F 4000	003F 5FFF	7	8KB	0000 E000	0000 FFFF
64		003F 2000	003F 3FFF	6		0000 C000	0000 DFFF
63		003F 0000	003F 1FFF	5		0000 A000	0000 BFFF
62	64KB	003E 0000	003E FFFF	4		0000 8000	0000 9FFF
⋮	⋮	⋮	⋮	3		0000 6000	0000 7FFF
2	64KB	0002 0000	0002 FFFF	2		0000 4000	0000 5FFF
1		0001 0000	0001 FFFF	1		0000 2000	0000 3FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 1FFF

Table 6: 32Mb Memory Map – x16 Top and Bottom Boot [70:0]

Block	Block Size	Address Range (x16 Top Boot)		Block	Block Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
70	4KW	001F F000	001F FFFF	70	32KW	001F 8000	001F FFFF
69		001F E000	001F EFFF	69		001F 0000	001F 7FFF
68		001F D000	001F DFFF	68		001E 8000	001E FFFF
67		001F C000	001F CFFF	⋮	⋮	⋮	⋮
66		001F B000	001F BFFF	8	32KW	0000 8000	0000 FFFF
65		001F A000	001F AFFF	7	4KW	0000 7000	0000 7FFF
64		001F 9000	001F 9FFF	6		0000 6000	0000 6FFF
63		001F 8000	001F 8FFF	5		0000 5000	0000 5FFF
62	32KW	001F 0000	001F 7FFF	4		0000 4000	0000 4FFF
⋮	⋮	⋮	⋮	3		0000 3000	0000 3FFF
2	32KW	0001 0000	0001 7FFF	2		0000 2000	0000 2FFF
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

Table 7: 32Mb Memory Map – x8/x16 Uniform Blocks [63:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
63	64KB	03F 0000h	03F FFFFh	63	32KW	01F 8000h	01F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
0		000 0000h	000 FFFFh	0		000 0000h	000 7FFFh

Memory Map – 64Mb

Table 8: 64Mb Memory Map – x8 Top and Bottom Boot [134:0]

Block	Block Size	Address Range (x8 Top Boot)		Block	Block Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
134	8KB	007F E000	007F FFFF	134	64KB	007F 0000	007F FFFF
133		007F C000	007F DFFF	133		007E 0000	007E FFFF
132		007F A000	007F BFFF	132		007D 0000	007D FFFF
131		007F 8000	007F 9FFF	⋮	⋮	⋮	⋮
130		007F 6000	007F 7FFF	8	64KB	0001 0000	0001 FFFF
129		007F 4000	007F 5FFF	7	8KB	0000 E000	0000 FFFF
128		007F 2000	007F 3FFF	6		0000 C000	0000 DFFF
127		007F 0000	007F 1FFF	5		0000 A000	0000 BFFF
126	64KB	007E 0000	007E FFFF	4		0000 8000	0000 9FFF
⋮	⋮	⋮	⋮	3		0000 6000	0000 7FFF
2	64KB	0002 0000	0002 FFFF	2		0000 4000	0000 5FFF
1		0001 0000	0001 FFFF	1		0000 2000	0000 3FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 1FFF

Table 9: 64Mb Memory Map – x16 Top and Bottom Boot [134:0]

Block	Block Size	Address Range (x16 Top Boot)		Block	Block Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
134	4KW	003F F000	003F FFFF	134	32KW	003F 8000	003F FFFF
133		003F E000	003F EFFF	133		003F 0000	003F 7FFF
132		003F D000	003F DFFF	132		003E 8000	003E FFFF
131		003F C000	003F CFFF	⋮	⋮	⋮	⋮
130		003F B000	003F BFFF	8	32KW	0000 8000	0000 FFFF
129		003F A000	003F AFFF	7	4KW	0000 7000	0000 7FFF
128		003F 9000	003F 9FFF	6		0000 6000	0000 6FFF
127		003F 8000	003F 8FFF	5		0000 5000	0000 5FFF
126	32KW	003F 0000	003F 7FFF	4		0000 4000	0000 4FFF
⋮	⋮	⋮	⋮	3		0000 3000	0000 3FFF
2	32KW	0001 0000	0001 7FFF	2		0000 2000	0000 2FFF
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

Table 10: 64Mb Memory Map – x8/x16 Uniform Blocks [127:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
127	64KB	07F 0000h	07F FFFFh	127	32KW	03F 8000h	03F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
63		03F 0000h	03F FFFFh	63		01F 8000h	01F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
0		000 0000h	000 FFFFh	0		000 0000h	000 7FFFh

Memory Map – 128Mb

Table 11: 128Mb Memory Map – x8/x16 Uniform Blocks [127:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
127	128KB	0FE 0000h	0FF FFFFh	127	64KW	07F 0000h	07F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
63		07E 0000h	07F FFFFh	63		03F 0000h	03F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
0		000 0000h	001 FFFFh	0		000 0000h	000 FFFFh

Bus Operations

Table 12: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	8-Bit Mode			16-Bit Mode	
						A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	H	X	Byte address	High-Z	Data output	Word address	Data output
WRITE	L	H	L	H	H[3]	Command address	High-Z	Data input[4]	Command address	Data input[4]
STANDBY	H	X	X	H	H	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z	High-Z	X	High-Z
RESET	X	X	X	L	X	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitches of less than 3ns on CE#, WE#, and RST# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# is LOW, then the highest or the lowest block remains protected, or the top two blocks or the bottom two blocks, depending on line item.
4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 8 words (16 bytes) and is addressed by address inputs A[2:0] in x16 bus mode and A[2:0] plus DQ15/A-1 in x8 bus mode. The extended memory blocks and CFI area do not support page read mode.

A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. (See AC Characteristics for details about when the output becomes valid.)

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation. (See AC Characteristics for timing requirement details.)

Standby

Driving CE# HIGH in read mode causes the device to enter standby, and data I/Os to be High-Z. To reduce the supply current to the standby supply current (I_{CC2}), CE# must be held within V_{CC} ±0.3V. (See DC Characteristics.)

During PROGRAM or ERASE operations the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and the outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to the standby level, independently from CE#, OE#, or WE# inputs.

Registers

Status Register

Table 13: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory, or when a BLANK CHECK operation fails.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode. (See WRITE TO BUFFER PROGRAM command.)	

Notes:
1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE or BLANK CHECK operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM, ERASE, or BLANK CHECK operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.

5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.
6. When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.

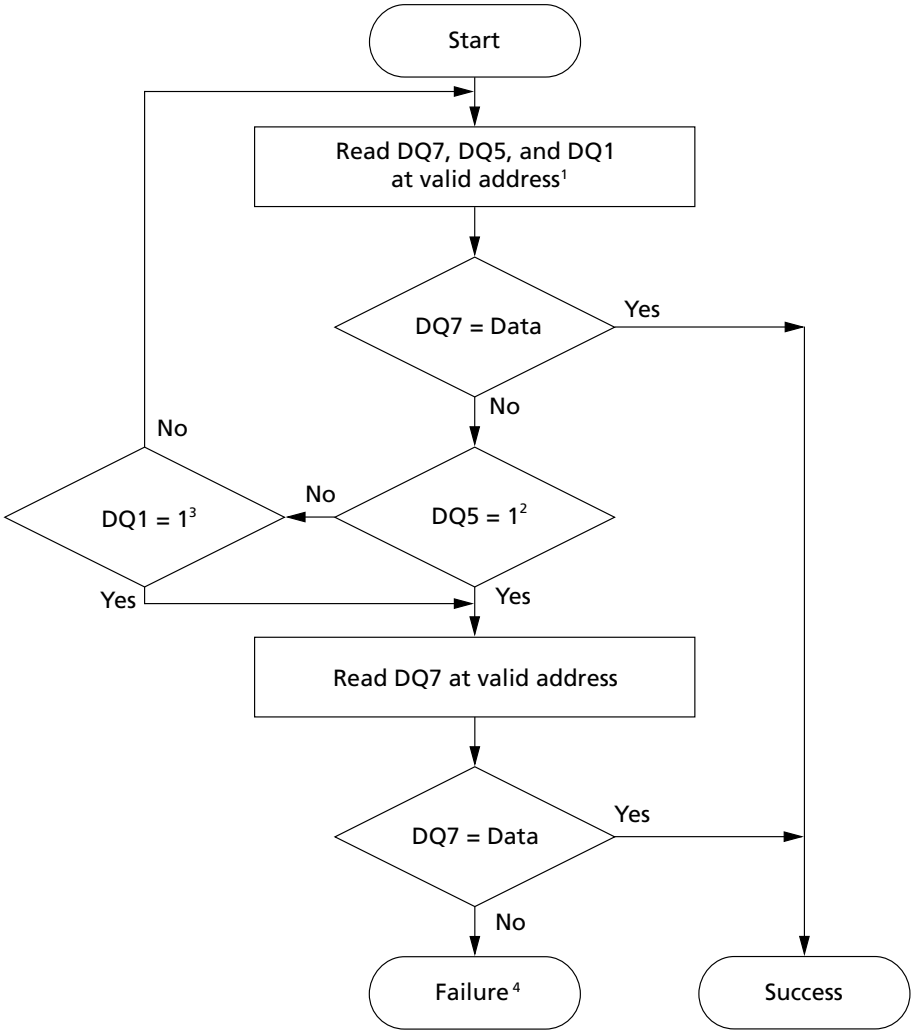
Table 14: Operations and Corresponding Bit Settings

Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	–	0	0	2
BLANK CHECK	Any address	1	Toggle	0	–	–	0	0	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	–	0	
	Non-erasing block	0	Toggle	0	0	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
PROGRAM SUSPEND	Programming block	Invalid operation						High-Z	
	Nonprogramming block	Outputs memory array data as if in read mode						High-Z	
ERASE SUSPEND	Erasing blk	1	No Toggle	0	–	Toggle	–	High-Z	
	Non-erasing blk	Outputs memory array data as if in read mode						High-Z	
PROGRAM during ERASE SUSPEND	Erasing block	DQ7#	Toggle	0	–	Toggle	–	0	2
	Non-erasing block	DQ7#	Toggle	0	–	No Toggle	–	0	2
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	High-Z	
PROGRAM Error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	2
ERASE Error	Erase success block	0	Toggle	1	1	No toggle	–	High-Z	
	Erase fail block	0	Toggle	1	1	Toggle	–	High-Z	
BLANK CHECK Error	Any address	1	Toggle	1	1	Toggle	–	High-Z	

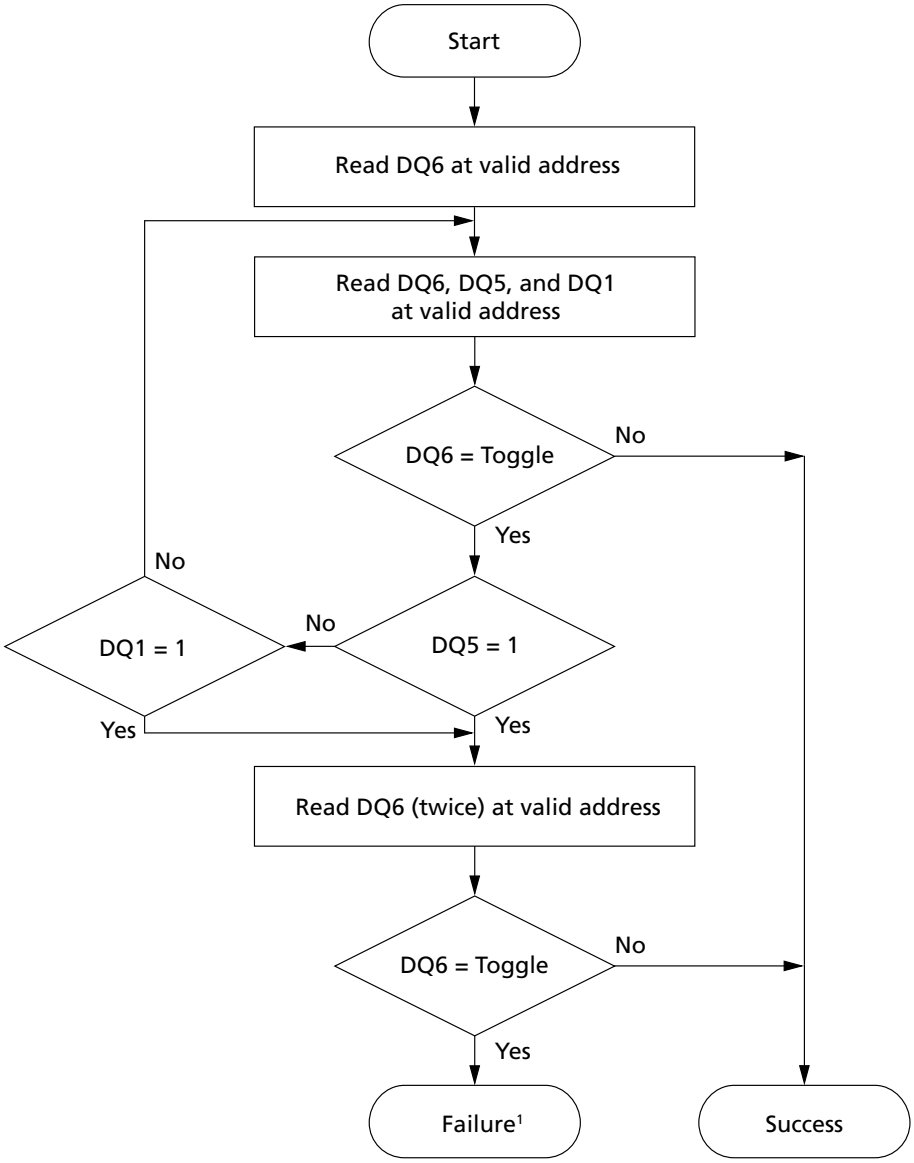
Notes: 1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.

Figure 6: Data Polling Flowchart



Notes:
1. Valid address is the address being programmed or an address within the block being erased or on which a BLANK CHECK operation has been executed.
2. The data polling process does not support the BLANK CHECK operation. The process represented in the Toggle Bit Flowchart figure can provide information on the BLANK CHECK operation.
3. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 7: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.