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Intel StrataFlash® Synchronous Memory (K3/K18)

28F640K3, 28F640K18, 28F128K3, 28F128K18, 28F256K3, 28F256K18 (x16)

Datasheet

Product Features

- **Performance**
  - —110/115/120 ns Initial Access Speed for 64/128/256 Mbit Densities
  - —25 ns Asynchronous Page-Mode Reads, 8 Words Wide
  - —13 ns Synchronous Burst-Mode Reads, 8 or 16 Words Wide
  - —32-Word Write Buffer
  - —Buffered Enhanced Factory Programming
- **Software**
  - —25 µs (typ.) Program and Erase Suspend Latency Time
  - —Flash Data Integrator (FDI), Common Flash Interface (CFI) Compatible
  - —Programmable WAIT Signal Polarity
- **Quality and Reliability**
  - —Operating Temperature: –40 °C to +85 °C
  - —100K Minimum Erase Cycles per Block
  - —0.18 µm ETOX™ VII Process
- **Architecture**
  - —Multi-Level Cell Technology: High Density at Low Cost
  - —Symmetrical 64 K-Word Blocks
  - —256 Mbit (256 Blocks)
  - —128 Mbit (128 Blocks)
  - —64 Mbit (64 Blocks)
  - —Ideal for “CODE + DATA” applications
- **Security**
  - —2-Kbit Protection Register
  - —Unique 64-bit Device Identifier
  - —Absolute Data Protection with V_{PEN} and WP#
  - —Individual and Instantaneous Block Locking, Unlocking and Lock-Down Capability
- **Packaging and Voltage**
  - —64-Ball Intel® Easy BGA Package (128-Mbit is also offered in a lead-free package)
  - —56-and 79-Ball Intel® VF BGA Package
  - —V_{CC} = 2.70 V to 3.60 V
  - —V_{CCQ} = 1.65 to 1.95 V/2.375 to 3.60 V

The Intel StrataFlash® Synchronous Memory (K3/K18) product line adds a high performance burst-mode interface and other additional features to the Intel StrataFlash® memory family of products. Just like its J3 counterpart, the K3/K18 device utilizes reliable and proven two-bit-per-cell technology to deliver 2x the memory in 1x the space, offering high density flash at low cost. This is Intel’s third generation MLC technology, manufactured on 0.18 µm lithography, making it the most widely used and proven MLC product family on the market.

K3/K18 is a 3-volt device (core), but it is available with 3-volt (K3) or 1.8-volt (K18) I/O voltages. These devices are ideal for mainstream applications requiring large storage space for both code and data storage. Advanced system designs will benefit from the high performance page and burst modes for direct execution from the flash memory. Available in densities from 64 Mbit to 256 Mbit (32 Mbyte), the K3/K18 device is the highest density NOR-based flash component available today, just as it was when Intel introduced the original device in 1997.

Notice: This document contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 290737-009
February 2005

Contents

Revision History

Date of Revision	Revision	Description
08/22/01	-001	Original Version
09/24/01	-002	Corrected Typographical Errors in 11.0 AC Characteristics section.
09/27/01	-003	Change VFBGA Package from 64 to 56 ball package. Add ordering info in Appendix E.
02/22/02	-004	Changes to ballouts per engineering review and editing/formatting updates.
06/17/02	-005	Changes to Iccr, elimination of Speed Bin 2, expansion of Vccq range.
06/11/03	-006	Corrections to Ordering Information, typcs, added Next-State Table, Appendix A info. Added table of Latency Count settings to Section 4.3.2.
12/01/03	-007	Update PDF presentation.
5/19/04	-008	Reformatted the document layout.
2/1/05	-009	Added lead-free information.

1.0 Introduction

This document contains information pertaining to the Intel StrataFlash® Synchronous Memory (K3/K18) device. The purpose of this document is to describe the features, operations and specifications of these devices.

1.1 Nomenclature

3 Volt core:	V_{CC} range of 2.7 V – 3.6 V
3 Volt I/O:	V_{CCQ} range of 2.375 V – 3.6 V
1.8 Volt I/O:	V_{CCQ} range of 1.65 V – 1.95 V
A_{MIN}:	For Easy BGA packages: A_{MIN} = A1 For VF BGA packages: A_{MIN} = A0
A_{MAX}:	For Easy BGA packages: 64 Mbit A_{MAX} = A22 128 Mbit A_{MAX} = A23 256 Mbit A_{MAX} = A24 For VF BGA packages: 64 Mbit A_{MAX} = A21 128 Mbit A_{MAX} = A22 256 Mbit A_{MAX} = A23
Block:	A group of flash cells that share common erase circuitry and erase simultaneously
Program:	To write data to the flash array
VPEN:	Refers to a signal or package connection name
V_{PEN}:	Refers to timing or voltage levels
CUI:	Command User Interface
OTP:	One Time Programmable
PR:	Protection Register
PLR:	Protection Lock Register
RFU:	Reserved for Future Use
SR:	Status Register
RCR:	Read Configuration Register
WSM:	Write State Machine
MLC:	Multi-Level Cell
Set:	Indicates a logic one (1)
Clear:	Indicates a logic zero (0)

1.2 Conventions

0x:	Hexadecimal prefix
0b:	Binary prefix
k (noun):	1,000
M (noun):	1,000,000
Byte:	8 bits
Word:	16 bits
Kword:	1,024 words
Kb:	1,024 bits
KB:	1,024 bytes
Mb:	1,048,576 bits
MB:	1,048,576 bytes
Brackets:	Square brackets ([]) will be used to designate group membership or to define a group of signals with similar function (i.e. A[21:1], SR[4,1] and D[15:0]).

2.0 Functional Overview

This section provides an overview of the K3/K18 device features and architecture.

The K3/K18 device product line adds a high performance burst-mode interface and other additional features to the Intel StrataFlash® memory family of products. Just like its J3 counterpart, the K3/K18 utilizes reliable and proven two-bit-per-cell technology to deliver 2x the memory in 1x the space, offering high density flash at low cost. This is the third generation of Intel's multi-level cell (MLC) technology, manufactured on 0.18 µm lithography, making it the most widely used and proven MLC product family on the market.

K3/K18 is a 3-volt device (core), but it is available with 3-volt (K3) or 1.8-volt (K18) I/O voltages. These devices are ideal for mainstream applications requiring large storage space for both code and data storage. Advanced system designs will benefit from the high performance page and burst modes for direct execution from the flash memory. Available in densities from 64 Mb to 256 Mbit (32 Mbyte), the K3/K18 device is the highest density NOR-based flash component available today, just as it was when Intel introduced the original device in 1997.

2.1 High Performance Page/Burst Modes

NOR-based flash is generally preferred over other architectures for its reliability and fast read speeds. Fast reads allow the application to execute code directly out of flash, rather than downloading to RAM for execution, saving the costs of redundant system memory and board space. The K3/K18 device sets the standard for fast read speeds by adding burst mode and utilizing an 8 word page mode. Burst mode increases throughput up to 76MB/s, effectively five times faster than asynchronous reads on standard flash memory, and supports performance up to 66 Mhz with zero wait states. Both page and burst modes also provide a high performance glueless interface to the Intel® StrongARM* SA-1110 CPU (and future Intel® XScale processors) and many other microprocessors.

2.2 Single Chip Solution

In addition to code execution, many applications also have data storage needs. K3/K18 memory provides a single-chip solution for combined code execution and data storage. A single-chip solution is easy to implement by utilizing a unique hardware and software combination: the K3/K18 device and Intel® Persistent Storage Manager (Intel® PSM). Intel® PSM is royalty free when used with Intel® Flash, is an installable file system and block device driver for Microsoft Windows* CE OS version 2.1 and later.

The Intel® PSM software is appropriate for any application using the Microsoft Windows CE operating system, including PC Companions, Set-Top Boxes, and other connected appliances and hand-held devices. Other operating system ports are also available. Intel® PSM is optimized for the Intel StrataFlash® Memory product line.

For wireless applications, Intel® Flash Data Integrator (Intel® FDI) Version 4 software provides the ability to manage data and files in Intel StrataFlash® Memory in an open architecture, including support for downloaded Java* applets, Bluetooth* file transfers, and voice recognition tags.

2.3 Packaging Options

The K3/K18 device is available in multiple packages: lead and lead-free Easy BGA and VF BGA, and Stacked Chip Scale Package (SCSP, stacking with SRAM or flash + flash). The 64-ball Easy BGA package provides SOP reliability and long-term footprint compatibility and cost in a chip scale package size. The VF BGA and SCSP offer small footprints for wireless applications.

Manufactured on the Intel 0.18-micron process technology, Intel StrataFlash® Memory offers unprecedented value and performance and reliability.

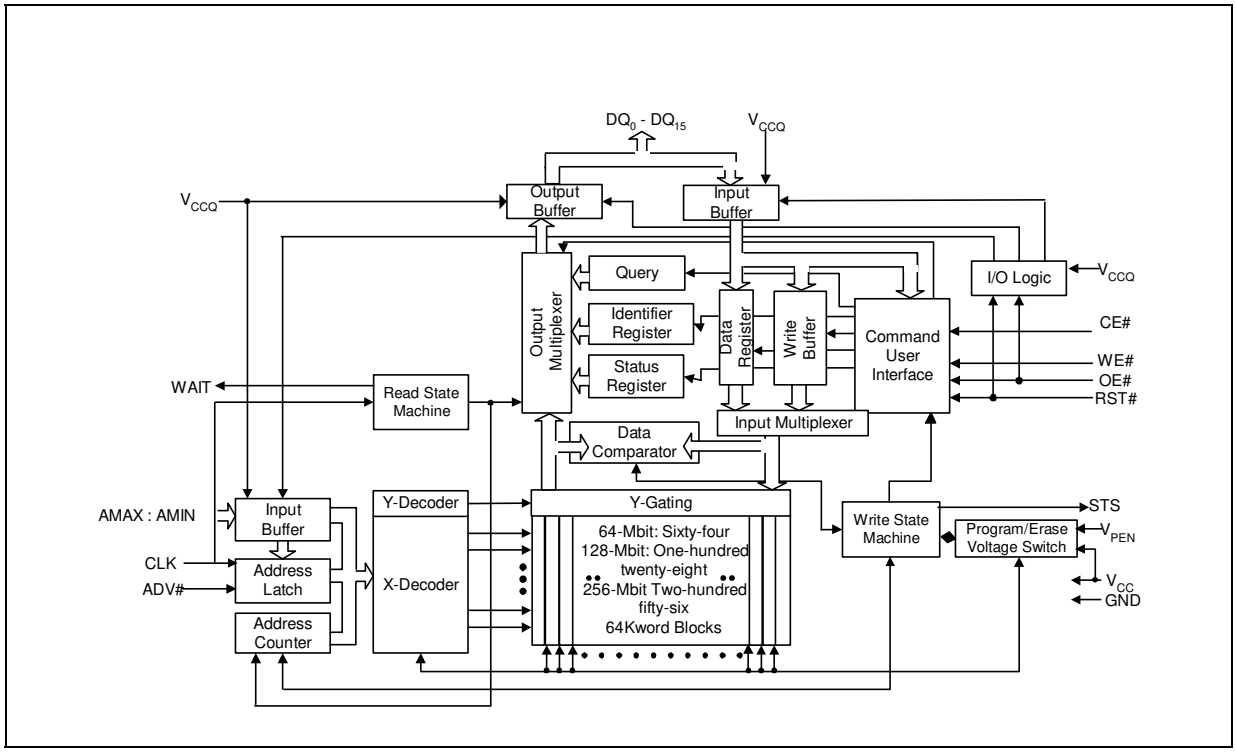
2.4 Product Highlights

High performance read modes: 8 or 16-word synchronous burst, 8-word page:

- 64 Mb: 110/25/13 ns (async/page/burst)
- 128 Mb: 115/25/13 ns (Offered in both lead and lead-free Easy BGA packages)
- 256 Mb:120/25/13 ns
- 2.7 V to 3.6 V Vcc operation
- 64-ball Easy BGA
- VF BGA packages and Stacked Chip Scale Package (SCSP)
- I/O V_{CCQ}: 2.375 V to 3.6 V (K3); 1.65 V to 1.95 V (K18)
- One-time-programmable protection registers (2Kbits)
- Program and Erase suspend capability
- Cost-effective multi-level cell architecture
- Royalty-free software support for most applications with Intel® PSM, Intel® FDI Version 4, or VFM
- Full extended operating temperature: -40° C to +85° C
- Proven reliability: 100,000 cycles, up to 20 years data retention

2.5 K3/K18 Block Diagram

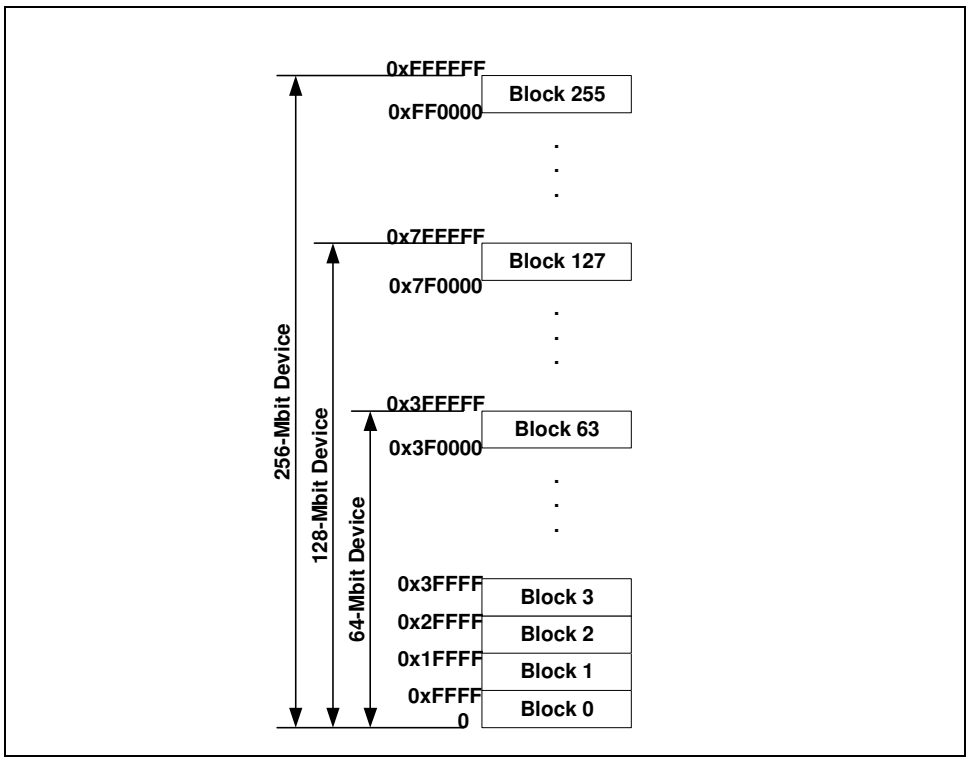
Figure 1. K3/K18 Device Memory Block Diagram



2.6 Memory Map

The K3/K18 device array is divided into symmetrical blocks that are 64-Kword in size. A 64 Mbit device contains 64 blocks, a 128 Mbit device contains 128 blocks and a 256 Mbit device contains 256 blocks. Flash cells within a block are organized by rows and columns. A block contains 512 rows by 128 words. The words on a row are divided into 16 eight-word groups. (See Figure 2.)

Figure 2. K3/K18 Device Memory Map



3.0 Package Information

3.1 Easy BGA Package

Figure 3. Easy BGA Package Drawing

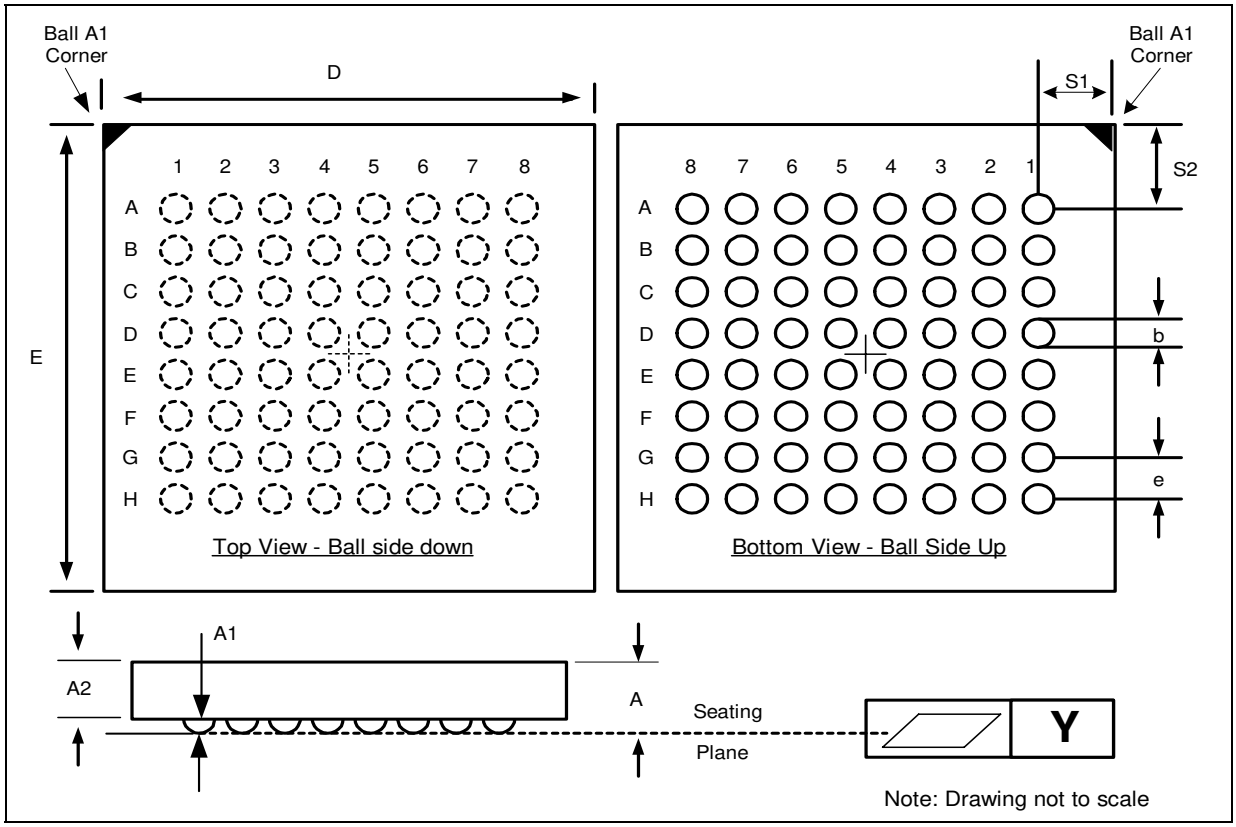


Table 1. Easy BGA Package Dimensions (Sheet 1 of 2)

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.200				0.0472
Ball Height	A1	0.250				0.0098		
Package Body Thickness	A2		0.780				0.0307	
Ball Width	b	0.330	0.430	0.530		0.0130	0.0169	0.0209
Package Body Width (64 Mb, 128 Mb, 256 Mb)	D	9.900	10.000	10.100	1	0.3898	0.3937	0.3976
Package Body Length (64 Mb, 128 Mb)	E	12.900	13.000	13.100	1	0.5079	0.5118	0.5157
Package Body Length (256 Mb)	E	14.900	15.000	15.100	1	0.5866	0.5906	0.5945
Pitch	[e]		1.000				0.0394	
Ball Count	N		64				64	

Table 1. Easy BGA Package Dimensions (Sheet 2 of 2)

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D (64/128/256 Mb)	S1	1.400	1.500	1.600	1	0.0551	0.0591	0.0630
Corner to Ball A1 Distance Along E (64/128 Mb)	S2	2.900	3.000	3.100	1	0.1142	0.1181	0.1220
Corner to Ball A1 Distance Along E (256 Mb)	S2	3.900	4.000	4.100	1	0.1535	0.1575	0.1614

3.2 VF BGA for 64 Mbit and 128 Mbit Package

Figure 4. VF BGA for 64 Mb and 128 Mb Package Drawing

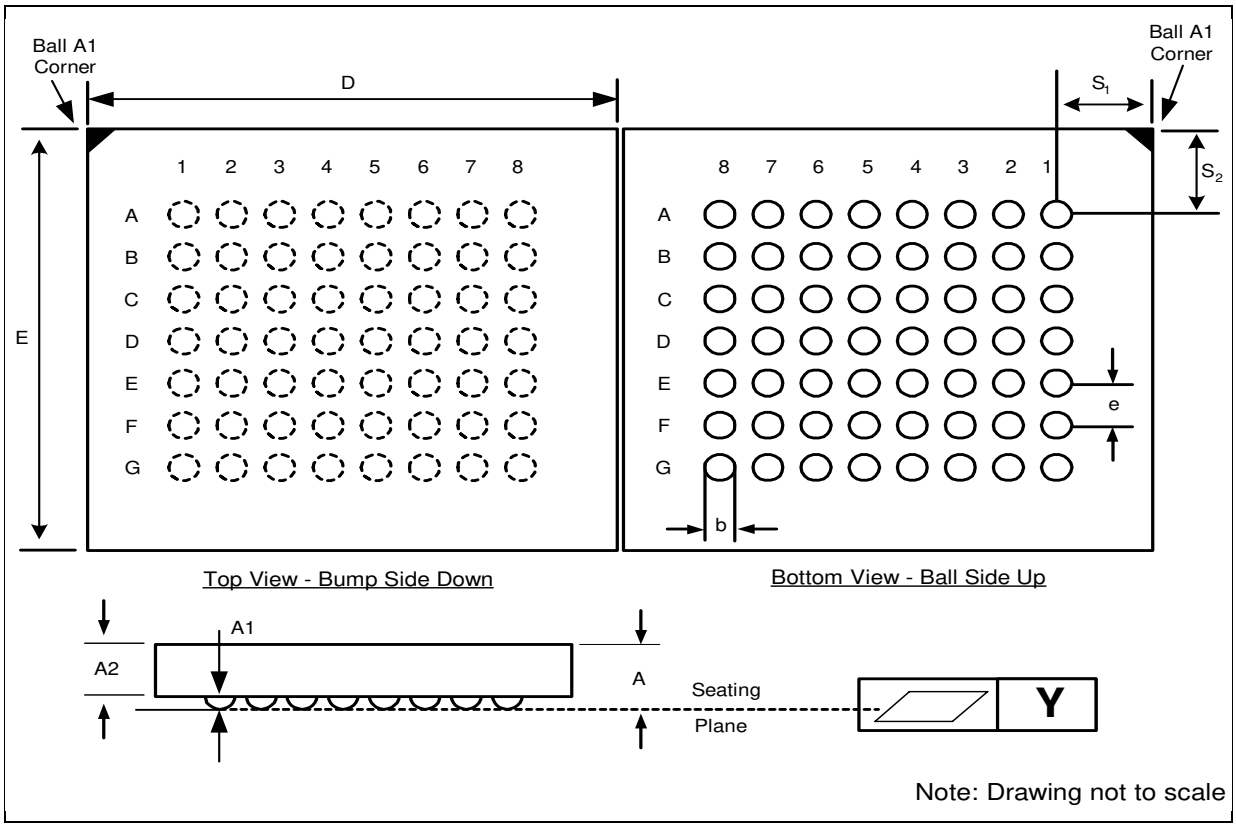


Table 2. VF BGA Package (64 Mb and 128 Mb) Dimensions (Sheet 1 of 2)

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.000				0.0394
Ball Height	A1	0.150				0.0059		
Package Body Thickness	A2		0.665				0.0262	

Table 2. VF BGA Package (64 Mb and 128 Mb) Dimensions (Sheet 2 of 2)

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Width (64 Mb)	D	7.600	7.700	7.800	1	0.2992	0.3031	0.3071
Package Body Width (128 Mb)	D	10.900	11.000	11.100	1	0.4291	0.4331	0.4370
Package Body Length (64 Mb, 128 Mb)	E	8.900	9.000	9.100	1	0.3504	0.3543	0.3583
Pitch	[e]		0.750				0.0295	
Ball (Lead) Count	N		56				56	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D (64 Mb)	S1	1.125	1.225	1.325	1	0.0443	0.0482	0.0522
Corner to Ball A1 Distance Along E (128 Mb)	S1	2.775	2.875	2.975	1	0.1093	0.1132	0.1171
Corner to Ball A1 Distance Along E (64 Mb, 128 Mb)	S2	2.150	2.250	2.350	1	0.0846	0.0886	0.0925

3.3 VF BGA for 256 Mbit Package

Figure 5. VF BGA Package 256 Mb Drawing

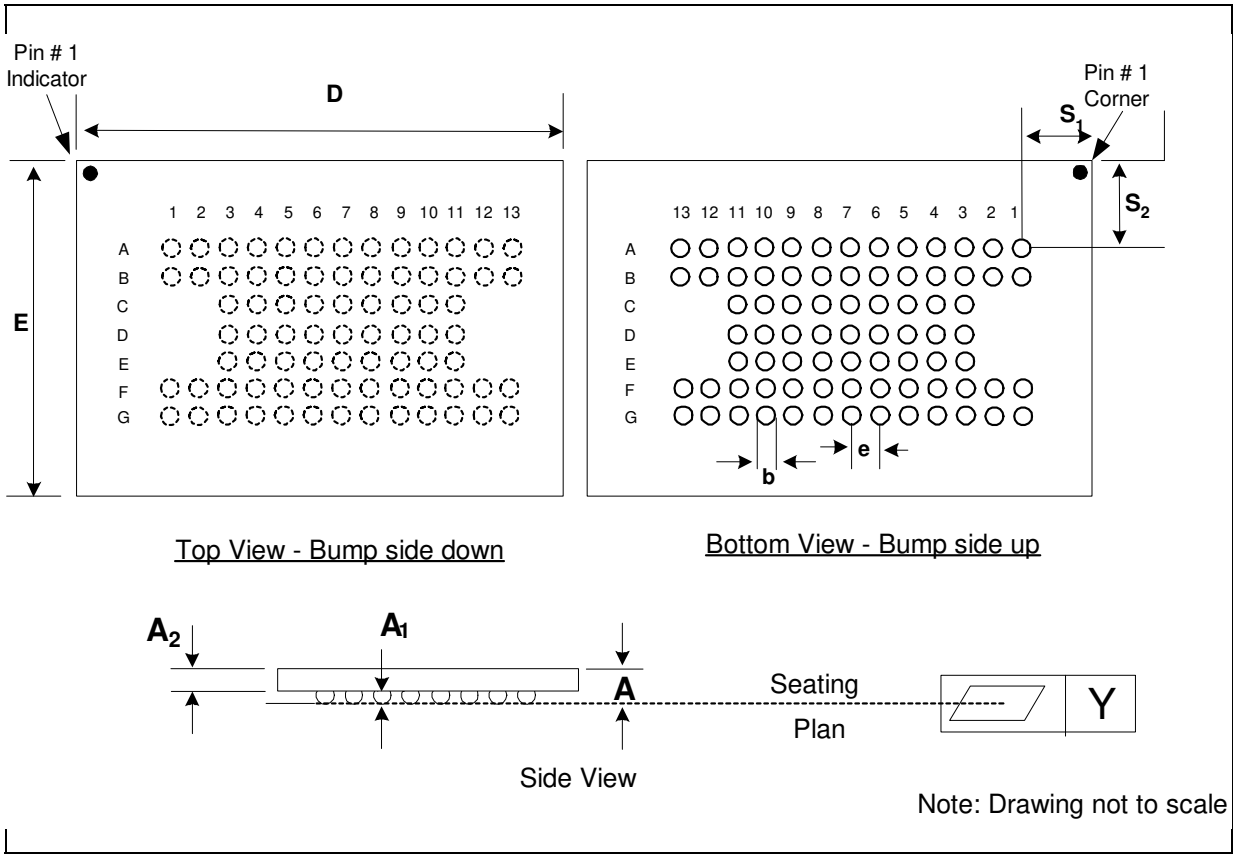


Table 3. VF BGA (256 Mb) Dimensions

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.000				0.0394
Ball Height	A1	0.150				0.0059		
Package Body Thickness	A2		0.665				0.0262	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Width	D	14.400	14.500	14.600	1	0.5669	0.5709	0.5748
Package Body Length	E	8.900	9.000	9.100	1	0.3504	0.3543	0.3583
Pitch	[e]		0.750				0.0295	
Ball (Lead) Count	N		79				79	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D	S1	2.650	2.750	2.850	1	0.1043	0.1083	0.1122
Corner to Ball A1 Distance Along E	S2	2.150	2.250	2.350	1	0.0846	0.0886	0.0925

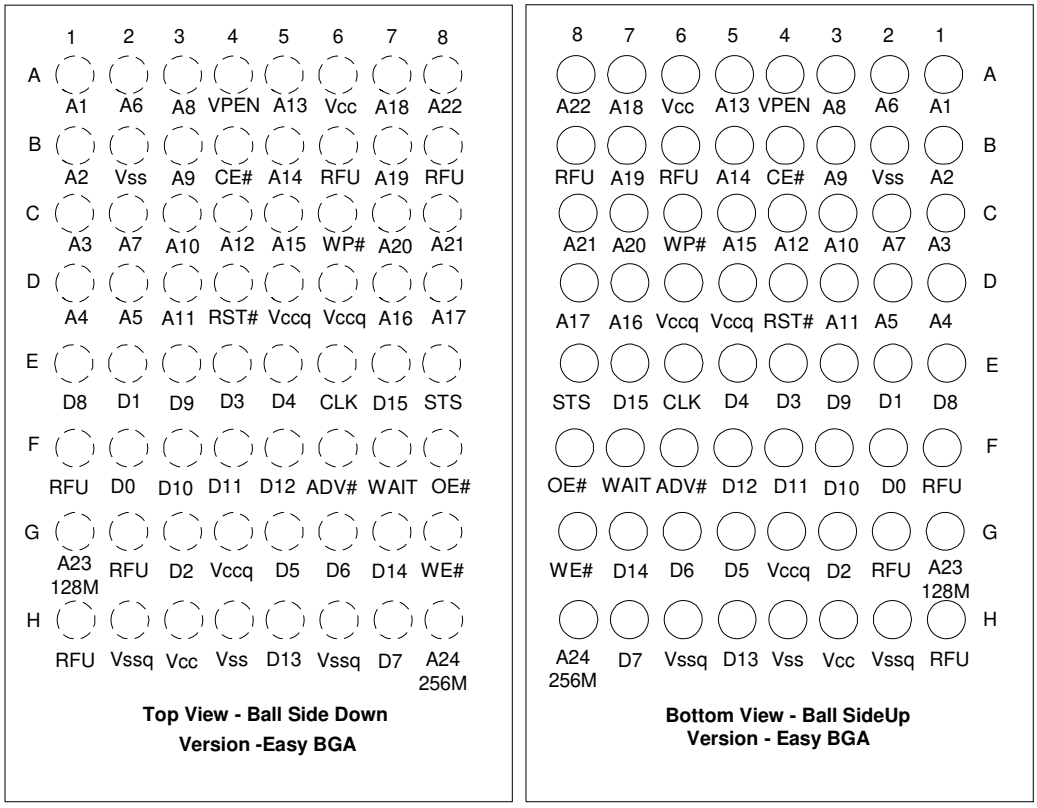
4.0 Ballout and Signal Description

The K3/K18 device is available in a 64-ball Easy BGA package for the 64-, 128-, and 256 Mbit densities. See Figure 6.

This device is also available in a 56-ball VF BGA package for the 64- and 128-Mbit densities and a 79-ball VF BGA package for the 256-Mbit density. See Figure 7 on page 18 and Figure 8 on page 19.

4.1 64-Ball Easy BGA Package for All Densities (1.0 mm Ball Pitch)

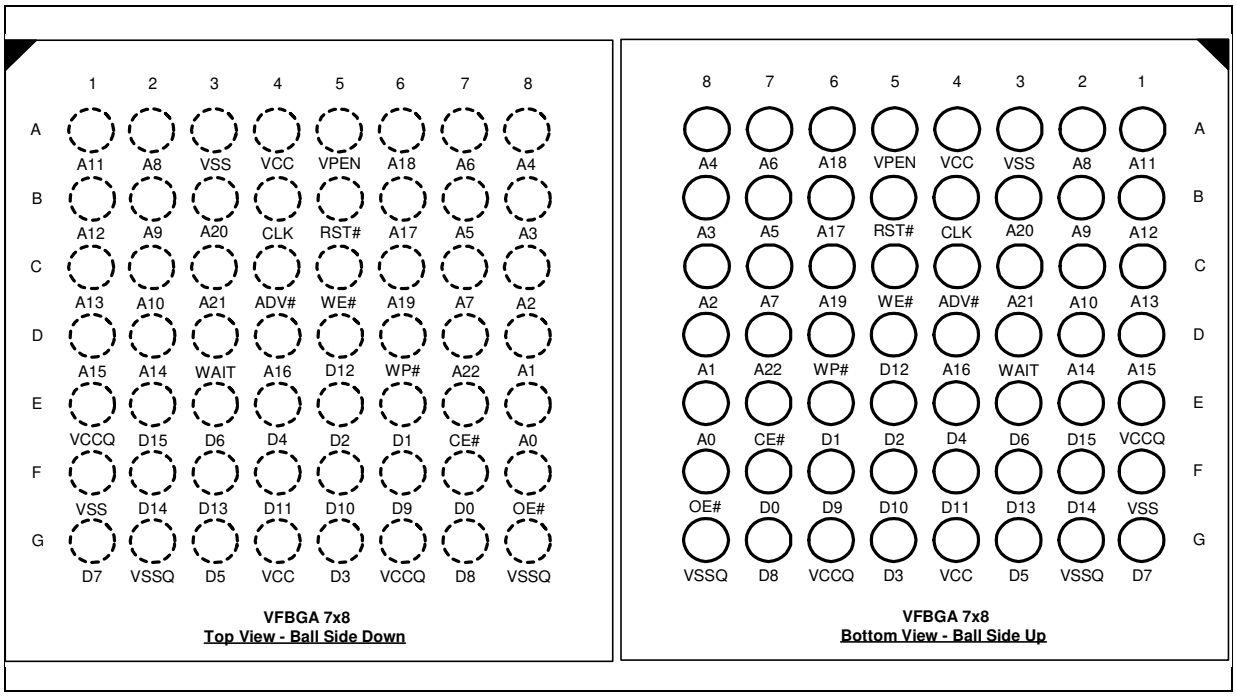
Figure 6. 64-Ball Easy BGA Package for All Available Densities (1.0 mm Ball Pitch)



NOTES:
1. Address A23 is valid only on 128-Mbit densities and above; otherwise, it is a no connect (NC).
2. Address A24 is valid only on 256-Mbit density; otherwise, it is a no connect (NC).

4.2 56-Ball VF BGA Package for 64- and 128-Mbit Density (0.75 mm Ball Pitch)

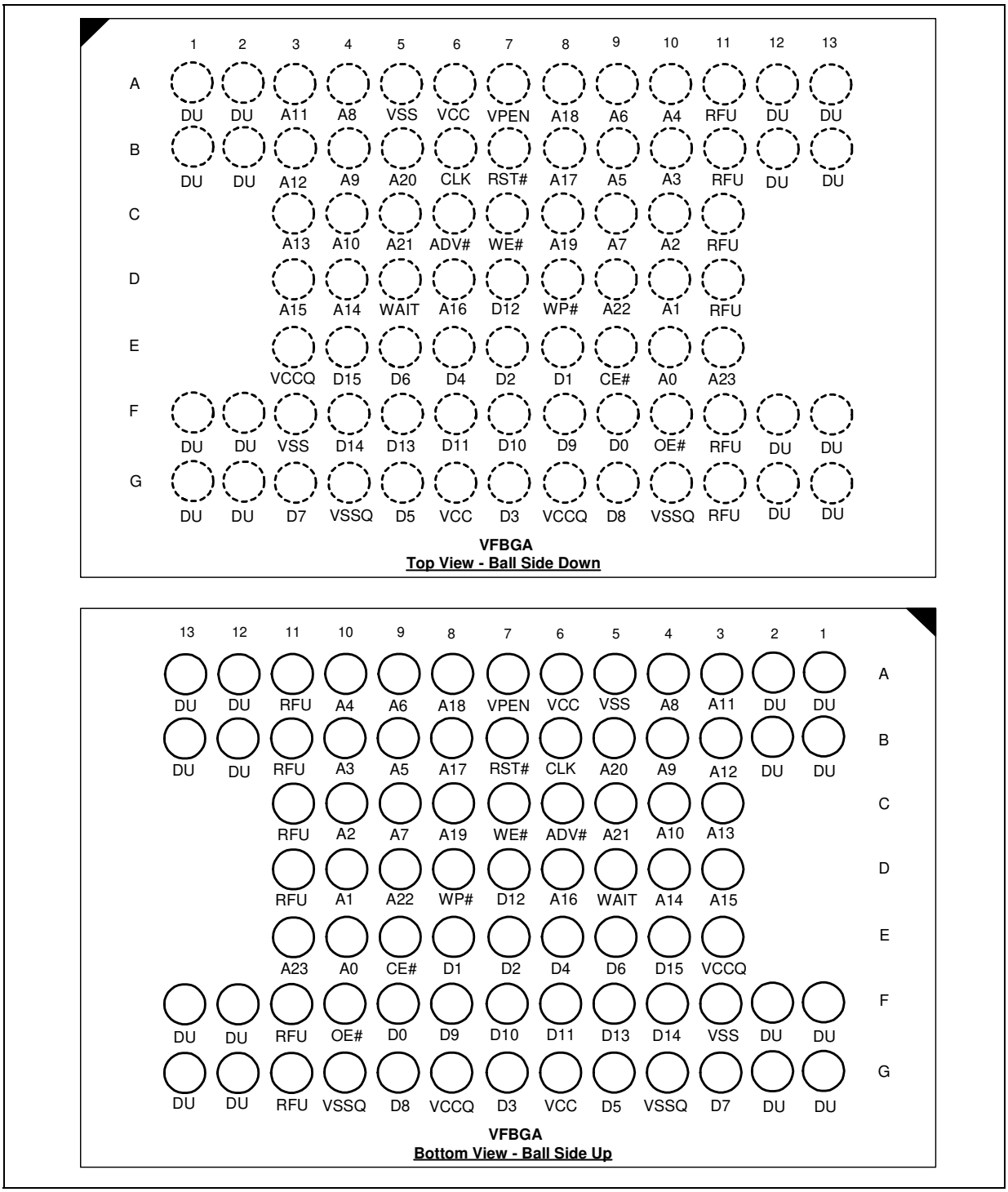
Figure 7. 56-Ball VF BGA Package 0.75 mm Ball Pitch (for 64- and 128-Mb Densities ONLY)



NOTE: Address A22 is only valid on 128-Mbit density; otherwise, it is a no connect (NC).

4.3 79-Ball VF BGA for 256-Mbit Density Package

Figure 8. 79-Ball VF BGA Package for 256-Mbit Density



4.4 Signal Descriptions

Table 4 describes the active signals used.

Table 4. Signal Descriptions

Sym	Type	Name and Function
A[A_{MAX}:A_{MIN}]	Input	**ADDRESS:** Device address. Address internally latched during read/write operations. See nomenclature Section 1.2 for A_{MAX} and A_{MIN} values.
D[15:0]	Input/ Output	**DATA I/O:** Inputs data and commands during write operations, outputs data during read operations. Float when CE# or OE# are de-asserted. Data is internally latched during write operations.
CE#	Input	**CHIP ENABLE:** Active-low; CE#-low selects the device. CE#-high deselects the device, places it in standby mode, and places data and WAIT outputs in a High-Z state.
OE#	Input	**OUTPUT ENABLE:** Active-low; OE#-low enables the device's output data drivers during read cycles. OE#-high places the data outputs in a High-Z state.
WE#	Input	**WRITE ENABLE:** Active-low; WE# controls writes to the flash device. Address and data are latched on the rising edge of WE#.
RST#	Input	**RESET:** Active-low; resets internal circuitry and inhibits write operations. This provides data protection during power transitions. RST#-high enables normal operation. Exit from reset places the device in asynchronous read-array mode.
WP#	Input	**WRITE PROTECT:** Active-low; WP#-low enables the lock-down mechanism. Blocks locked down cannot be unlocked with the unlock command. WP#-high overrides the lock-down function enabling blocks to be erased or programmed through software.
ADV#	Input	**ADDRESS VALID:** Active-low; during synchronous read operations, addresses are latched on the rising edge of ADV# or on the rising (or falling) edge of CLK, whichever occurs first.
VPEN	Input	**ERASE/PROGRAM/BLOCK LOCK ENABLE:** Controls device protection. When $V_{PEN} \leq V_{PENLK}$, flash contents are protected against Program and Erase.
CLK	Input	**CLOCK:** Synchronizes the device to the system's bus frequency in synchronous-read mode, and increments the internal address generator. During synchronous read operations, addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first. Connect this signal to VCC if the device will not be used in synchronous-read mode.
STS	Open Drain Output	**STATUS:** Indicates the status of the internal state machine. When configured in level mode (default mode), it acts as a RY/BY# pin. When configured in one of its pulse modes, it can indicate program and/or erase completion. For alternate configurations of the STATUS pin, see the configuration commands. STS is to be tied to V_{CCQ} with a pull-up resistor.
WAIT	Output	**WAIT:** Indicates invalid data in synchronous-read (burst) modes. WAIT is High-Z whenever CE# is de-asserted. WAIT is not gated by OE#.
VCC	Power	**CORE POWER SUPPLY:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \leq V_{LKO}$. Device operation at invalid V_{CC} voltages should not be attempted.
VCCQ	Power	**I/O POWER SUPPLY:** I/O Output-driver source voltage.
VSS	Power	**GROUND:** Ground reference for device core power supply. Connect to system ground.
VSSQ	Power	**I/O GROUND:** I/O Ground reference for device I/O power supply. Connect to system ground.
DU	—	**DO NOT USE:** Do not use this ball. This ball should not be connected to any power supplies, signals or other balls and must be left floating.
NC	—	**NO CONNECT:** No internal connection; can be driven or floated.
RFU	—	**RESERVED for FUTURE USE:** Balls designated as RFU are reserved by Intel for future device functionality and enhancement.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

The absolute maximum ratings are shown in Table 5.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Maximum Rating	Notes
Temperature under bias	–40 °C to +85 °C	
Storage temperature	–65 °C to +125 °C	
Voltage on any signal (except VCC and VCCQ)	–0.5 V to V_{CCQ} +0.5 V	1,2
VCC1 (K3) voltage	–0.2 V to +4.1 V	1
VCC2 (K18) voltage	-0.2 V to +3.8 V	
VCCQ1 (K3) voltage	–0.2 V to +4.1 V	1
VCCQ2 (K18) voltage	–0.2 V to +2.45 V	1
Output short circuit current	100 mA	3

NOTES:
1. Specified voltages are with respect to V_{SS}. Minimum DC voltage is –0.5 V on input/output signals and –0.2 V on V_{CC} and V_{CCQ}. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on V_{CC} is V_{CC} +0.5 V, which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns. Maximum DC voltage on input/output signals and V_{CCQ} is V_{CCQ} +0.5 V, which, during transitions, may overshoot to V_{CCQ} +2.0 V for periods <20 ns.
2. Program/erase voltage is normally 2.7 V–3.6 V.
3. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Symbol	Parameter	Min	Max	Units
T_A	Operating Temperature	–40	+85	°C
V_{CC1}	Core Voltage (K3)	2.70	3.60	V
V_{CC2}	Core Voltage (K18)	2.70	3.30	V
V_{CCQ1}	Vccq I/O Supply voltage (K3)	2.375	3.60	V
V_{CCQ2}	Vccq I/O Supply voltage (K18)	1.65	1.95	V
Block Erase Cycles	All Blocks, V_{CC} = 3 V	100,000		Cycles

6.0 Electrical Specifications

6.1 DC Current Characteristics

Table 6. DC Current Characteristics

V_{CC}				2.7 V – 3.3 V		2.7 V – 3.6 V			
V_{CCQ}				1.65 V– 1.95 V		2.375 V – 3.6 V			
Sym	**Parameter**		**Notes**	**Typ**	**Max**	**Typ**	**Max**	**Unit**	**Test Condition**
I_{LI}	Input Load Current		1		±1		±1	µA	$V_{CC} = V_{CCMAX}$, $V_{CCQ} = V_{CCQMAX}$, $V_{IN} = V_{CCQ}$ or GND
I_{LO}	Output Leakage Current		1		±10		±10	µA	$V_{CC} = V_{CCMAX}$, $V_{CCQ} = V_{CCQMAX}$, $V_{IN} = V_{CCQ}$ or GND
I_{CCS}	V_{CC} Standby	64 Mbit, 128 Mbit	1, 2, 3, 4	30	55	30	55	µA	CMOS Inputs, $V_{CC} = V_{CCMAX}$, $V_{CCQ} = V_{CCQMAX}$, Device is Disabled RST# = V_{CCQ}±0.2V/GND±0.2V
		256 Mbit		45	80	45	80	µA	
I_{CCR}	Average V_{CC} Read Current	Single Word Read	1, 3, 4, 5	10	73	10	78	mA	$V_{CC} = V_{CCMAX}$, $t_{ACC} = t_{AVQV}$
		Asynchronous Page Mode		16	28	18	30	mA	8 Word Read; $t_{ACC} = t_{AVQV}$, t_{APA} = 25 ns, $V_{CC} = V_{CCMAX}$
		Synchronous Burst		24	38	32	46	mA	Burst length = 8; f = 66 MHz(K3), 50 MHz(K18) $V_{CC} = V_{CCMAX}$ CE# = V_{IL}, OE# = V_{IH}, Inputs = V_{IH} or V_{IL}
				28	40	36	48	mA	Burst length = 16
I_{CCW}	V_{CC} Program Current		1, 4, 6, 7	50	80	40	70	mA	CMOS Inputs, $V_{PEN} = V_{CC}$
I_{CCE}	V_{CC} Block Erase Current		1, 4, 6, 7	50	80	40	70	mA	CMOS Inputs, $V_{PEN} = V_{CC}$
I_{CCWS}, I_{CCES}	V_{CC} Program Suspend or Block Erase Suspend Current		1, 4, 6, 7		20		10	mA	Device is enabled

NOTES:
1. All currents are RMS unless noted. Typical values at V_{CC} = 3 V, T_A = +25°C, best-case address pattern. Maximum values at V_{CC} = 3.6 V, worst-case address pattern.
2. Includes STS.
3. CMOS inputs/outputs are either $V_{CC} \pm 0.2$ V or $V_{SS} \pm 0.2$ V.
4. Current values are specified over a specific temperature range (–40°C to +85°C).
5. Sampled, not 100% tested.
6. I_{CCES}, I_{CCWS} are specified with device deselected. If device is read while in erase suspend/program suspend, current is I_{CCES} plus I_{CCR} or I_{CCWS} plus I_{CCR}.
7. $V_{PEN} < V_{PENLK}$ inhibits block erase, program and lock-bit operations. Don't use V_{PEN} outside its valid ranges.

Table 7. DC Voltage Characteristics

V_{CC}				2.7 V – 3.3 V		2.7 V – 3.6 V			
V_{CCQ}				1.65 V – 1.95 V		2.375 V – 3.6 V			
Sym	**Parameter**[1]		**Note**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Condition**
V_{IL}	Input Low Voltage	CMOS	7	0	0.4	0	0.4	V	
V_{IH}	Input High Voltage	CMOS	7	V_{CCQ} –0.4	V_{CCQ}	2.3	V_{CCQ}	V	
V_{OL}	Output Low Voltage	CMOS	2, 4		0.2		0.2	V	$V_{CC} = V_{CCMIN}$, $V_{CCQ} = V_{CCQMIN}$, $I_{OH} = 100\ \mu A$
V_{OH}	Output High Voltage	CMOS	2, 4	V_{CCQ} –0.2		V_{CCQ} –0.2		V	$V_{CC} = V_{CCMIN}$, $V_{CCQ} = V_{CCQMIN}$, $I_{OH} = -100\ \mu A$
V_{PENLK}	V_{PEN} Lock-Out during normal operations		3, 5		1.0		1.0	V	
V_{PENH}	V_{PEN} during Block Erase, Program or Lock-Bit operations		3, 5	1.65	1.95	2.7	3.6	V	
V_{LKO}	V_{CC} Lockout Voltage		3, 6	1.8		1.8		V	
V_{CCQLKO}	V_{CCQ} Lockout Voltage		3	1.0		1.0		V	

NOTES:
1. All currents are RMS unless noted. Typical values at typical V_{CC}, $T_A = +25°C$.
2. Includes STS.
3. Sampled, not 100% tested.
4. I_{CCES}, I_{CCWS} are specified with device deselected. If device is read while in erase suspend/program suspend, current is I_{CCES} plus I_{CCR} or I_{CCWS} plus I_{CCR}.
5. $V_{PEN} < V_{PENLK}$ inhibits block erase, program and lock-bit operations. Don't use V_{PEN} outside its valid ranges.
6. Block erases, programming and lock-bit configurations are inhibited when $V_{CC}<V_{LKO}$, and not guaranteed in the range between V_{LKOMIN} and V_{CCMIN}, and above V_{CCMAX}.
7. V_{IL} can undershoot to –0.4V and V_{IH} can overshoot to V_{CCQ} +0.4V for durations of 20 ns or less.

7.0 AC Characteristics

7.1 Read Operations

Table 8. AC Read Characteristics (Sheet 1 of 2)

VCC					2.7 V - 3.3 V		2.7 V - 3.6 V		
VCCQ					1.65 V - 1.95V		2.375 V - 3.6 V		
Num	**Sym**	**Parameter**[3]	**Density**	**Note**	**Min**	**Max**	**Min**	**Max**	**Unit**
Asynchronous Specifications									
R1	t_{AVAV}	Read cycle time	64 Mbit		110		110		ns
			128 Mbit		115		115		ns
			256 Mbit		120		120		ns
R2	t_{AVQV}	Address to output delay	64 Mbit	6		110		110	ns
			128 Mbit			115		115	ns
			256 Mbit			120		120	ns
R3	t_{ELQV}	CE# low to output delay	64 Mbit	3		110		110	ns
			128 Mbit			115		115	ns
			256 Mbit			120		120	ns
R4	t_{GLQV}	OE# low to output delay		3		30		25	ns
R5	t_{PHQV}	RST# high to output delay	64 Mbit			190		180	ns
			128 Mbit			220		210	ns
			256 Mbit			220		210	ns
R6	t_{ELQX}	CE# low to output in Low-Z			0		0		ns
R7	t_{GLQX}	OE# low to output in Low-Z		3	0		0		ns
R8	t_{EHQZ}	CE# high to output in High-Z		5		25		25	ns
R9	t_{GHQZ}	OE# high to output in High-Z		5		25		25	ns
R10	t_{OH}	Output hold from first occurring address, CE# or OE# change		5	0		0		ns
R11	t_{EHEL}	CE# high to CE# low		1	0		0		ns
R12	$t_{ELTL/H}$	CE# low to WAIT low				30		25	ns
R13	t_{EHTZ}	CE# high to WAIT High-Z				30		25	ns
Latching Specifications									
R101	t_{AVVH}	Address setup to ADV# high			9		7		ns
R102	t_{ELVH}	CE# low to ADV# high			9		7		ns
R103	t_{VLQV}	ADV# low to output delay	64 Mbit			110		110	ns
			128 Mbit			115		115	ns
			256 Mbit			120		120	ns

Table 8. AC Read Characteristics (Sheet 2 of 2)

VCC					2.7 V - 3.3 V		2.7 V - 3.6 V		
VCCQ					1.65 V - 1.95V		2.375 V - 3.6 V		
Num	**Sym**	**Parameter[3]**	**Density**	**Note**	**Min**	**Max**	**Min**	**Max**	**Unit**
R104	t_{VLVH}	ADV# pulse width low			12		10		ns
R105	t_{VHVL}	ADV# pulse width high			12		10		ns
R106	t_{VHAX}	Address hold from ADV# high		4	10		8		ns
R108	t_{APA}	Page address access		6		30		25	ns
Clock Specifications									
R200	f_{CLK}	CLK frequency				50		66	MHz
R201	t_{CLK}	CLK period		7	20		15		ns
R202	$t_{CH/L}$	CLK high/low time		7	7		4.5		ns
R203	t_{CHCL}	CLK fall/rise time		7		3		3	ns
Synchronous Specifications									
R301	t_{AVCH}	Address valid setup to CLK			9		7		ns
R302	t_{VLCH}	ADV# low setup to CLK			9		7		ns
R303	t_{ELCH}	CE# low setup to CLK			9		7		ns
R304	t_{CHQV}	CLK to output delay		7		15		13	ns
R305	t_{CHQX}	Output hold from CLK			3		3		ns
R306	t_{CHAX}	Address hold from CLK		4	10		8		ns
R307	$t_{CHTL/H}$	CLK to WAIT delay		7, 8		15		13	ns
R312	t_{CHVL}	CLK to ADV# low			3		3		ns

NOTES:
1. CE# high between synchronous reads = 15 ns. Data bus read voltage is ≤ V_{CCQ1}.
2. See Figure 17, "AC Input/Output Reference Waveform" on page 32 for timing measurements and maximum allowable input slew rate.
3. OE# may be delayed up to t_{ELQV}-t_{GLQV} after CE# low without impact on t_{ELQV}.
4. Address hold in synchronous burst-mode is t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
5. Sampled, not 100% tested.
6. For devices configured to standard word read mode, R108(t_{APA}) will equal R2(t_{AVQV}).
7. The clock duty cycle should be 50% (approx.).
8. Applies only to subsequent synchronous reads.