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SEMTECH

RClamp3552T
Low Voltage RailClamp®
2-Line ESD Protection

PROTECTION PRODUCTS

Description

RClamp®3552T is a low voltage RailClamp which can provide ESD protection to IEC 61000-4-2 on highspeed ports. It is manufactured using Semtech's proprietary low voltage technology, designed to minimize both the ESD peak clamping and TLP clampingvoltage. These devices "snap-back" to a low on-state voltage when the breakdown voltage of the device is exceeded. This has the advantage of lowering the overall ESD clamping voltage. When the device is in the on-state, the dynamic resistance is typically 0.30 Ohms, further minimizing the ESD clamping. Maximum capacitance is only 0.40pF allowing the RClamp3552T to be used in applications operating in excess of 6GHz without appreciable signal attenuation. Each device will protect two lines operating at 3.5 volts.

RClamp3552T is in a 3-pin SLP1006N3T package. It measures 1.0 x 0.6 mm with a nominal height of only 0.4mm. The leads are finished with lead-free NiPdAu.

The combination of low peak ESD clamping, low dynamic resistance, and low capacitance makes this device suitable for applications such as USB 3.0, LVDS, audio, and V-By-One interfaces.

Features

- High ESD withstand Voltage: +/-17kV (Contact) & +/-20kV(Air) per IEC 61000-4-2
- Very small PCB area: 0.6 mm^2
- Protects up to two data lines
- Low ESD clamping voltage
- Working voltage: 3.5 V
- Low capacitance: 0.40pF Maximum
- Low dynamic resistance: 0.30 Ohms Typical
- Solid-state silicon-avalanche technology

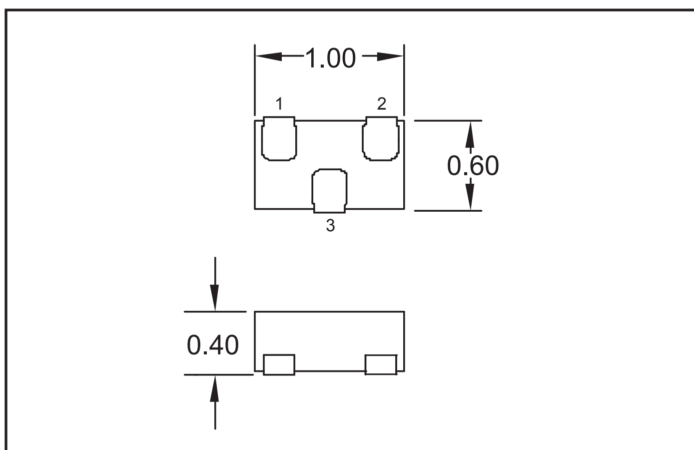
Mechanical Characteristics

- SLP1006N3T package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 1.0 x 0.6 x 0.40 mm
- Lead Finish: NiPdAu
- Molding compound flammability rating: UL 94V-0
- Marking: Marking code + dot matrix date code
- Packaging: Tape and Reel

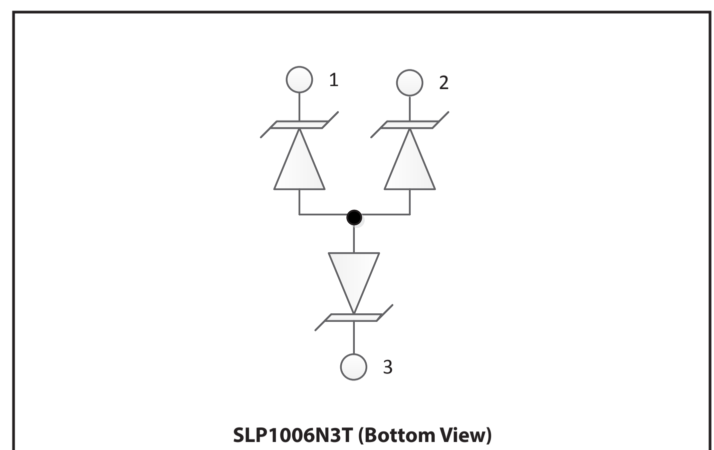
Applications

- USB 3.0
- V-By-One
- LVDS
- MIPI/MDDI
- MyDP
- Audio Ports

Package Dimension



Schematic & Pin Configuration



SLP1006N3T (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20μs)	I_{PP}	4	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±20 ±17	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 1 or 2 to Pin3				3.5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 10μA, Pin 1 or 2 to Pin3		7.5	8.8	9.8	V
Reverse Leakage Current	I_R	V_{RWM} = 3.5V, Pin 1 or 2 to Pin3			0.01	0.05	μA
Clamping Voltage	V_C	t_p = 8/20μs, Pin 1 or 2 to Pin3	I_{PP} = 1A		3.5	5	V
			I_{PP} = 4A		5	6.5	
ESD Clamping Voltage[2]	V_C	t_p = 0.2/100ns, Pin 1 or 2 to Pin3	I_{PP} = 16A		9.5		V
			I_{PP} = -16A		-9.5		
Dynamic Resistance[2,3] (Positive)	R_{DYN}	t_p = 0.2/100ns, Pin 1 or 2 to Pin3			0.30		Ω
Dynamic Resistance[2,3] (Negative)	R_{DYN}	t_p = 0.2/100ns, Pin 1 or 2 to Pin3			0.30		
Junction Capacitance	C_J	V_R = 0V, f = 1MHz, Pin 1 or 2 to Pin3			0.30	0.40	pF

Notes

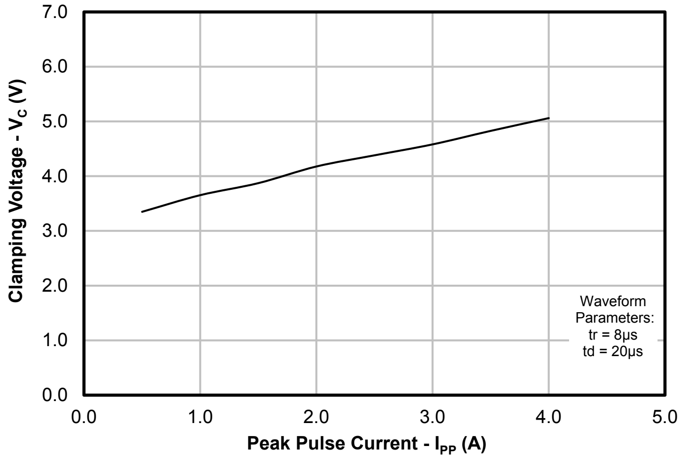
1) Measured with a 40dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.

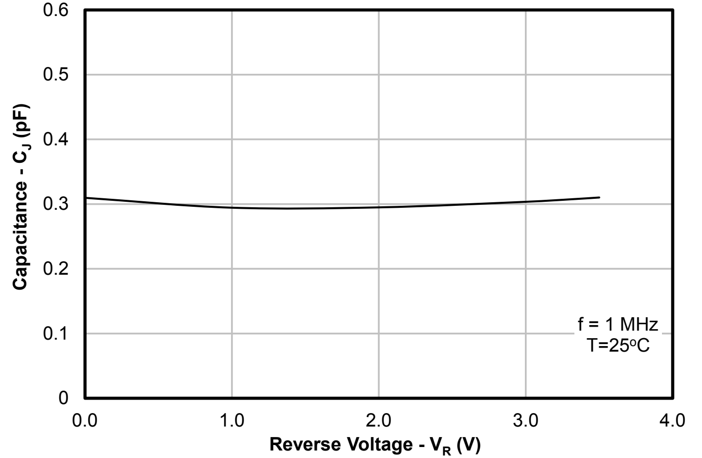
3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

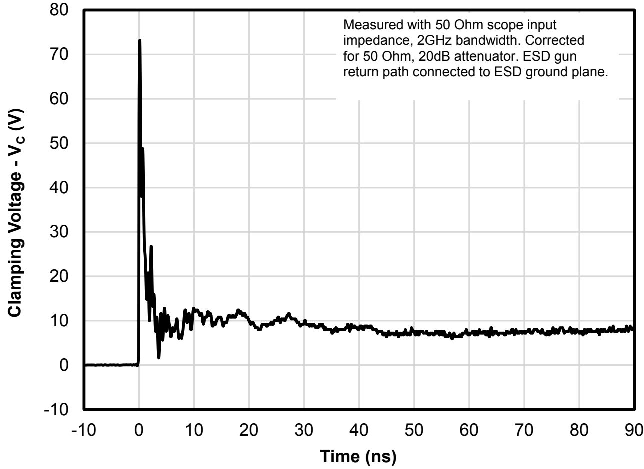
Clamping Voltage vs. Peak Pulse Current (tp=8/20μs) (Between any I/O and Ground)



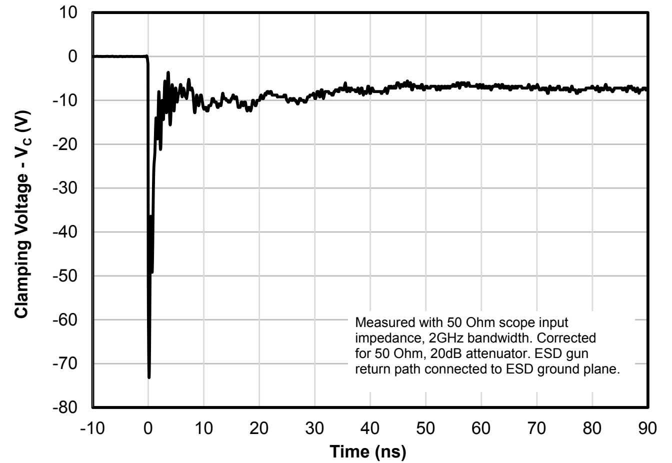
Junction Capacitance vs. Reverse Voltage (Between any I/O and Ground)



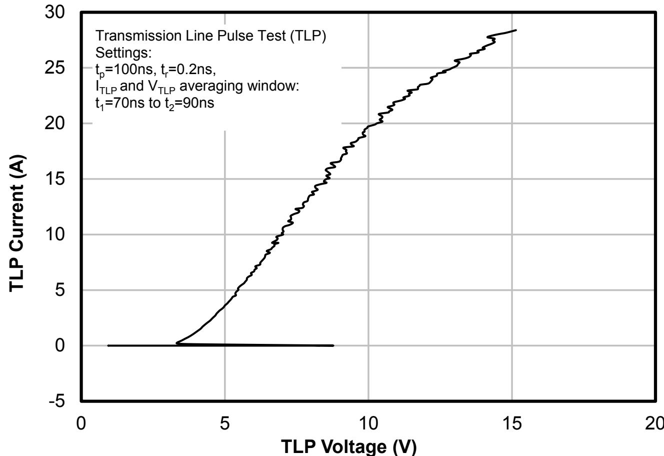
ESD Clamping (+8kV Contact per IEC 61000-4-2) (Between any I/O and Ground)



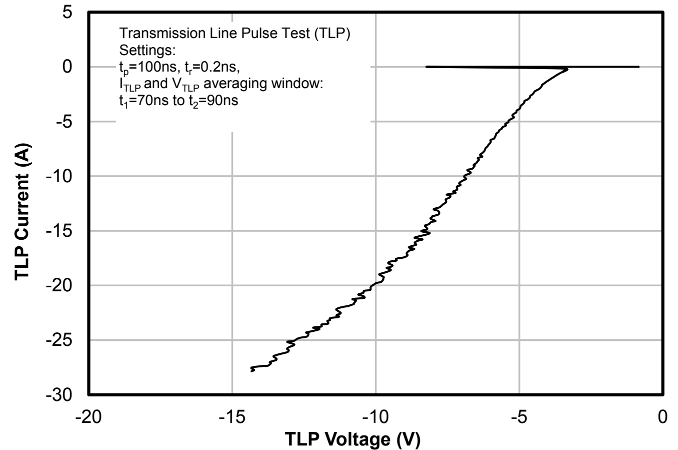
ESD Clamping (-8kV Contact per IEC 61000-4-2) (Between any I/O and Ground)



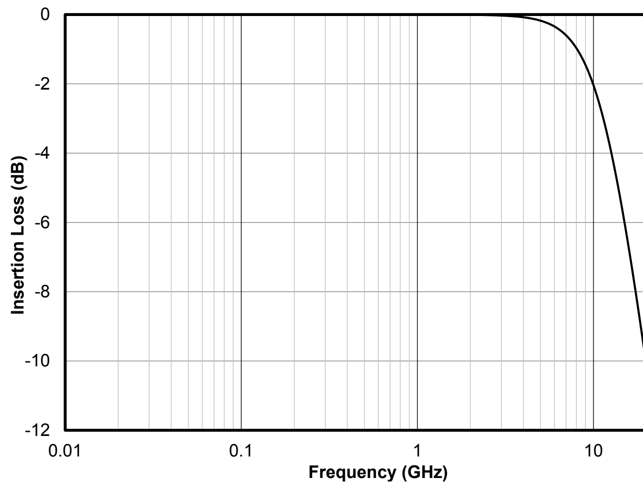
TLP Characteristic (Positive)

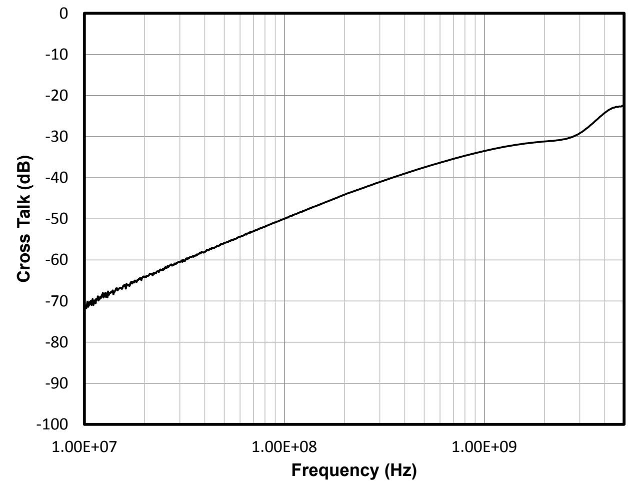


TLP Characteristic (Negative)



Typical Characteristics (Continued)



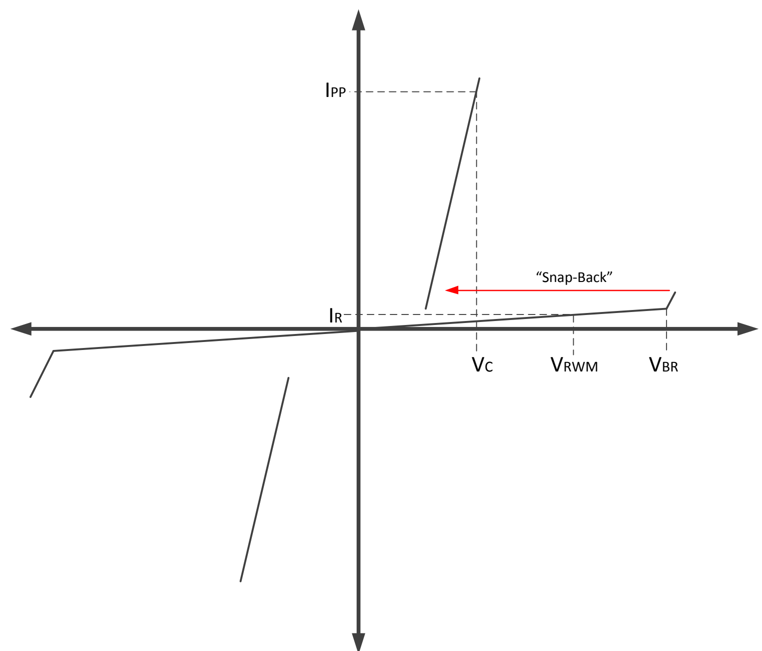


Applications Information

Device Operation

This device utilizes a multi-junction structure that is designed to switch to a low voltage state when triggered by ESD, EOS, or other transient events. During normal operation, the device will present a high impedance to the circuit for voltage up to the working voltage (V_{RWM}) of the device. When the voltage across the device terminals exceeds the breakdown voltage(V_{BR}), avalanche breakdown occurs in the blocking junction causing the device to "snap-back" or switch to a low impedance on-state. This has the advantage of lowering the overall clamping voltage (V_C) as ESD peak pulse current (I_{PP}) flows through the device. Once the current subsides, the device will return to a highimpedance off-state. Since this device is bidirectional, it will behave the same way for positive or negative polarity transient events.

Symbol	Parameter
V_{RWM}	Maximum Working Voltage
V_{TRIG}	Trigger Voltage
V_C	Clamping Voltage
I_R	Reverse Leakage Current
I_{PP}	Peak Pulse Currrent



Characterisitic Curve

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 2. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended. Assuming a 100um thick stencil, the aperture dimensions shown will yield an area ratio of approximately 0.75.

Recommended Mounting Pattern

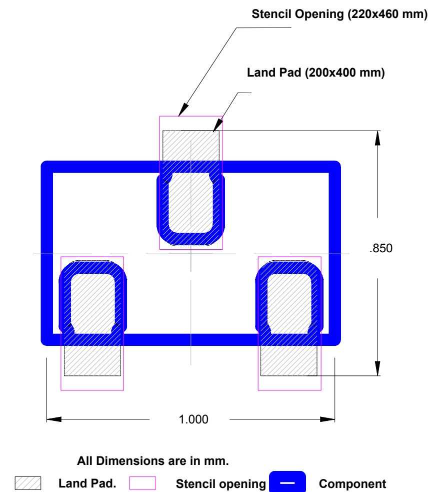
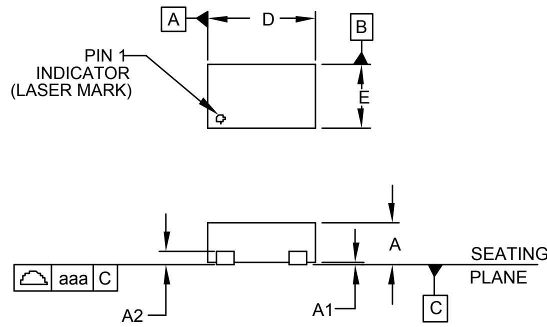
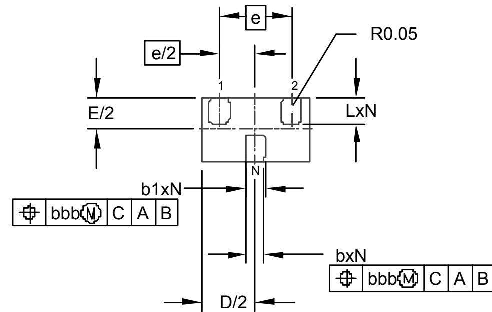


Table 2 - Recommended Assembly Guidelines	
Assembly Parameter	**Recommendation**
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular
Solder Stencil Thickness	0.100mm (0.004”)
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - SLP1006N3T

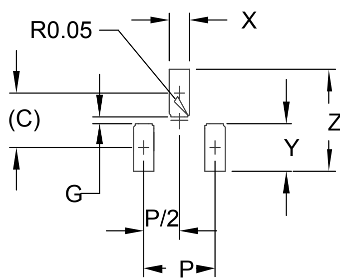


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.37	0.40	0.43
A1	0.00	0.02	0.05
A2		(0.13)	
b	0.145	0.17	0.195
b1	0.175	0.20	0.225
D	0.90	1.00	1.10
E	0.50	0.60	0.70
e		0.68 BSC	
L	0.225	0.25	0.275
N		3	
aaa		0.08	
bbb		0.10	



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

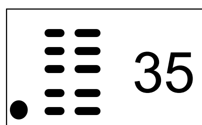
Land Pattern - SLP1006N3T



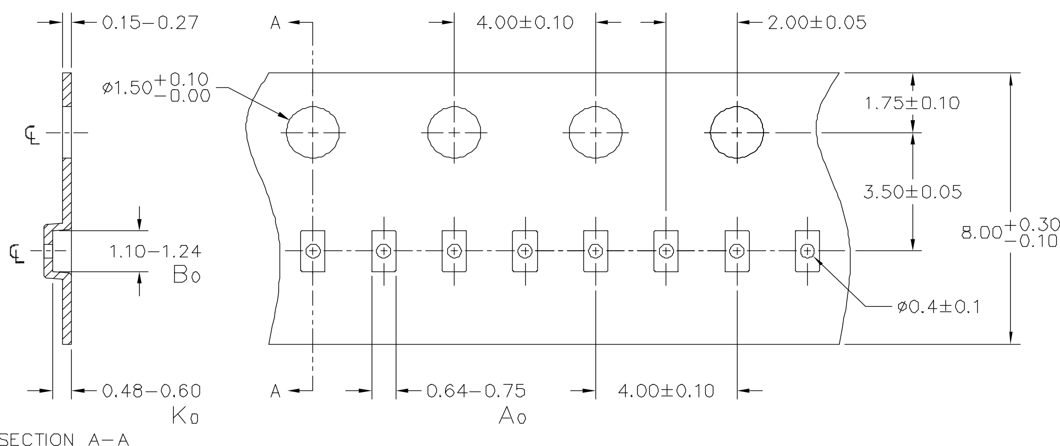
DIM	MILLIMETERS
C	(0.45)
G	0.05
P	0.68
X	0.20
Y	0.40
Z	0.85

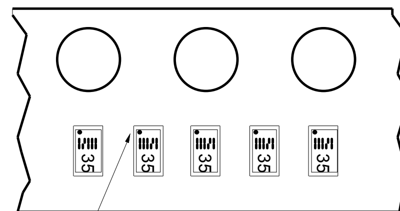
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Tape and Reel Specification





Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp3552T.TNT	10,000	7"

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