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RD3-2650

DP1.2 to HDMI1.4 converter

Reference board user guide

Rev. B

MegaChips

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1. Purpose and scope

This user guide provides set up instructions and the description of the STDP2650 reference board targeted for DP to HDMI conversion applications.

2. Description

The STDP2650 is MegaChips' latest generation DisplayPort converter series product that features a DisplayPort1.2 compliant receiver and an HDMI1.4 compliant transmitter, capable of handling high resolution video up to 4K2K 30Hz / FHD120Hz and audio up to 7.1CH.

The STDP2650 RD3 board is intended for the product evaluation and testing. The board contains a standard DP input connector, a standard HDMI output connector, and a micro USB connector for powering. It also includes an SPI flash for storing the firmware, a UART connector for debugging and in-system programming purpose (firmware download), and an I2C slave interface to configure the device from an external host controller (optional).

## 2.1. Board picture

Figure 1.   Board picture
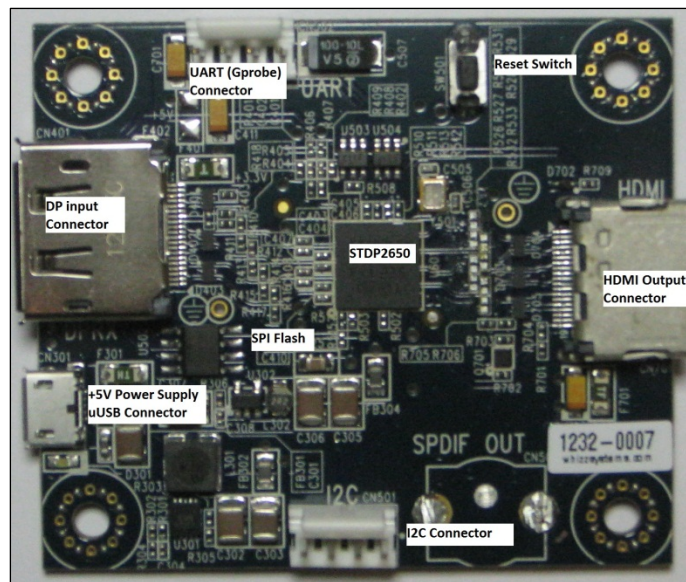
2.2. Set up instructions

The picture below is a typical connection diagram showing a notebook with DisplayPort output driving a TV/monitor using an STDP2650 RD board.

1.   Connect the DP output from the notebook to the DP input of the STDP2650 RD board using a standard DP cable.

2. Connect the HDMI output of the STDP2650 RD board to the HDMI input of the TV or the LCD monitor.

3. Power up the RD board by plugging in the micro USB cable (supplied with board) from an external USB source (ex: one of the USB ports from the notebook).

4. Use an HDMI TV or monitor that has audio output for testing the audio conversion through the STDP2650 RD board as well.

5. Once the connection is established and the board is powered, an image should appear on the screen within 2-3 seconds.

Figure 2.   Connection set up
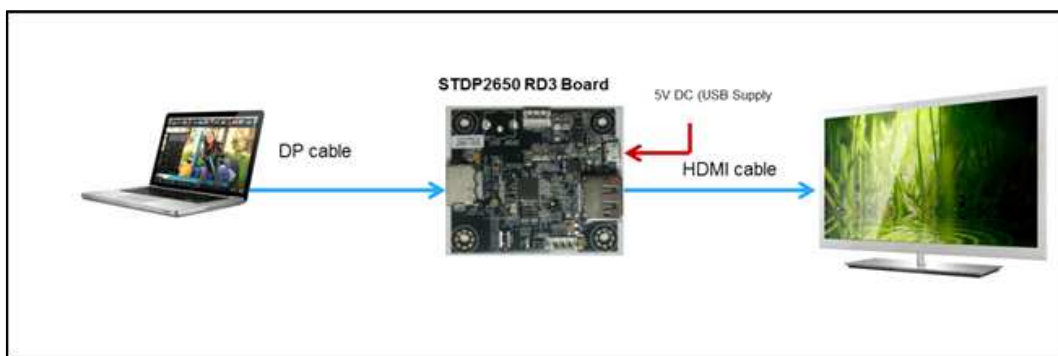
2.3. Diagnosis

If the image does not come up, follow the steps below for diagnosis.

Note: The diagnosis requires MegaChips GProbe software and hardware tool. Contact MegaChips for the GProbe software and board.

1. Install the GProbe diagnostic tool on a Windows OS based PC/NB and set the baud rate to 115,200.

2. Connect the GProbe board to the serial port (or USB port if using the USB version of the GProbe board) of the computer.

3. Connect the other end of the GProbe board to the UART connector (CN502) on the STDP2650 RD board using 4-wire cable (part of the GProbe board).

Note: Check the polarity while connecting the cable; Pin 1 is marked on the board. The 4-wire cable connection from CN502 to the GProbe board is 1 to 1.

4. Hit the reset button on the board (RESET SW501). You will see the firmware version and the date of the firmware in the GProbe window. This indicates that the DP Receiver IC is functional. If the message does not appear, reprogram the SPI Flash using the ISP method described in the GProbe user guide.

5. Using an oscilloscope, check the video input and output from the STDP2650 RD board.

Note: Refer to the STDP2650 datasheet for pin-out descriptions.

2.3.1. In-System Programming (ISP)

The STDP2650 RD board uses SPI Flash to store the firmware. For new firmware upgrade, following method is recommended.

ISP through UART connector: Allows programming of the SPI Flash through the UART (CN502) connector. This requires GProbe board and GProbe software tool from MegaChips. Also contact MegaChips for the latest binary file.

3. RD3-2650 board description

3.1. Connection diagram

Figure 3.   Connection diagram
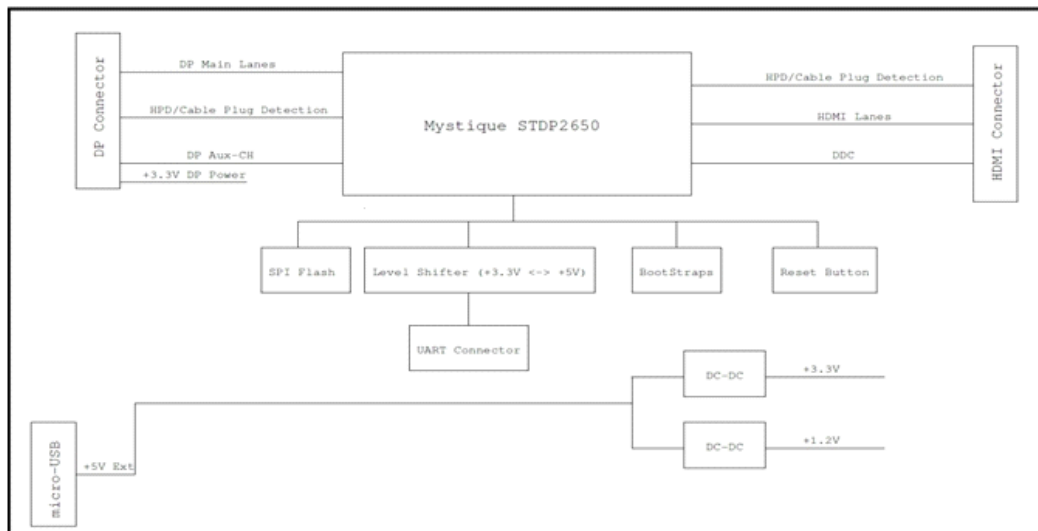
3.2. Principal components and functions

Below is a summary of all necessary connectors, switches, and other components. Please refer to the latest board schematics for further details.

Table 1.   Principal components and functions

Label	Description	Ref des
Power Input (+5 V, uUSB)	Input 5 V, down conversion to 3.3 V, and 1.2 V. This board uses an LDO [low-dropout] for 3.3 V and 1.2 V. Note the analog and digital supplies (3.3 A and 3.3 D or 1.2 A and 1.2 D) are isolated using ferrite beads.	CN301
STDP2650	MegaChips DP1.2 to HDMI1.4 converter IC	U601
DP Input	DP input connector	CN401
HDMI Output	DP output connector	CN701
SPI Flash	The board includes an SPI Flash of 4 MB to hold the firmware. The SPI Flash can be programmed (ISP) through UART interface.	U502
S/PDIF Output Not populated	Single wire S/PDIF output signal. Can route the encoded audio through SPDIF audio port	CN503 Not Populated
Host Interface (I2C)	Host Interface (I2C): This is a provision to access the STDP2650 device from an external host controller through the Host Interface (I2C port) connection.	CN501
UART (GProbe)	GProbe Interface (+3.3 V logic): GProbe connector that connects to the STDP2650 UART port for communication with external PC sources for debug purposes. The MegaChips GProbe tool (software) and PC interface board together create a debug environment for device debug and firmware update. The GProbe interface is also used for ISP purposes.	CN502
Reset	The reset button, when pressed, triggers a system reset through the internal reset circuitry. The reset button is used for system reset and debugs purposes	SW501
LED	Single LED for indicating the power on status.	D301
Crystal	A crystal of 27 MHz.	Y501
ESD Diodes	ESD protection diodes for HDMI and DisplayPort signal (main lanes, AUX and HPD line). The board implements low cost ESD diodes.	

3.3. Connector descriptions

The STDP2650 RD board has the following connectors. The locations of these connectors are shown in the above board picture.

CN301 – +5 V DC 2.5 A Power Input uUSB connector

CN501 – I2C Host interface (4x1 pin keyed header)

Pin 1	NC
Pin 2	I2C_SCL
Pin 3	I2C_SDA
Pin 4	GND

CN502 – UART (GProbe) Interface (4x1 pin keyed header)

Pin 1	+5V
Pin 2	UART_TX
Pin 3	UART_RX
Pin 4	GND

CN401 – DisplayPort receiver pin out details are shown below.

Pin 1	ML_L3N
Pin 2	GND
Pin 3	ML_L3P
Pin 4	ML_L2N
Pin 5	GND
Pin 6	ML_L2P
Pin 7	ML_L1N
Pin 8	GND
Pin 9	ML_L1P
Pin 10	ML_L0N
Pin 11	GND
Pin 12	ML_L0P
Pin 13	GND
Pin 14	GND
Pin 15	AUX_P
Pin 16	GND
Pin 17	AUX_N
Pin 18	HPD_OUT
Pin 19	GND
Pin 20	+3V3_AVDD

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U701 – HDMI transmitter (refer to the schematics for complete pin out details).

Pin 1	Data Lane 2+
Pin 2	GND
Pin 3	Data Lane 2-
Pin 4	Data Lane 1+
Pin 5	GND
Pin 6	Data Lane 1-
Pin 7	Data Lane 0+
Pin 8	GND
Pin 9	Data Lane 0-
Pin 10	Clock Lane +
Pin 11	GND
Pin 12	Clock Lane -
Pin 13	CEC
Pin 14	NC
Pin 15	DDC_SCL
Pin 16	DDC_SDA
Pin 17	GND
Pin 18	+5V
Pin 19	HPD

4. Revision history

Table 2.   Document revision history

Date	Revision	Changes
06-Nov-2012	A	Initial version.
02-Jun-2014	B	Updated to comply with MegaChips documentation style/formatting.

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