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| | |
|------------------------|--|
| Title | <i>Reference Design Report for a 7.5 W Continuous, 13 W Peak DVD / Set Top Box Using TNY376PN</i> |
| Specification | 85–265 VAC Input, 3.3 V (500 mA), 5 V (500 mA), 12 V (250 mA) and –12 V (30 mA) Outputs |
| Application | DVD / Set Top Box |
| Author | Power Integrations Applications Department |
| Document Number | RDR-115 |
| Date | May 22, 2007 |
| Revision | 1.0 |

Summary and Features

- Excellent cross regulation without need for post regulator
- *EcoSmart*® – Meets Energy Star / CEC requirements
 - No-load consumption <150 mW at 265 VAC (no bias winding required)
 - > 70% active-mode efficiency
 - > 0.5 W output power available for 1 W input simplifies DVD player design
- BP/M capacitor value selects MOSFET current limit for greater design flexibility
- Tightly toleranced I^2t parameter (–10%, +12%) reduces system cost:
 - Increases MOSFET and magnetics power delivery
 - Reduces overload power, which lowers output diode and capacitor costs
- Integrated *TinySwitch-PK* Safety/Reliability features:
 - Accurate ($\pm 5\%$), auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
 - Auto-restart protects against output short circuit and open loop fault conditions
 - > 3.2 mm creepage on package enables reliable operation in high humidity and high pollution environments
- Meets EN550022 and CISPR-22 Class B conducted EMI with >20 dB μ V margin

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com.



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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This document is an engineering report describing a four output flyback power supply utilizing a TNY376PN. This power supply is intended as a general purpose evaluation platform for *TinySwitch-PK*

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

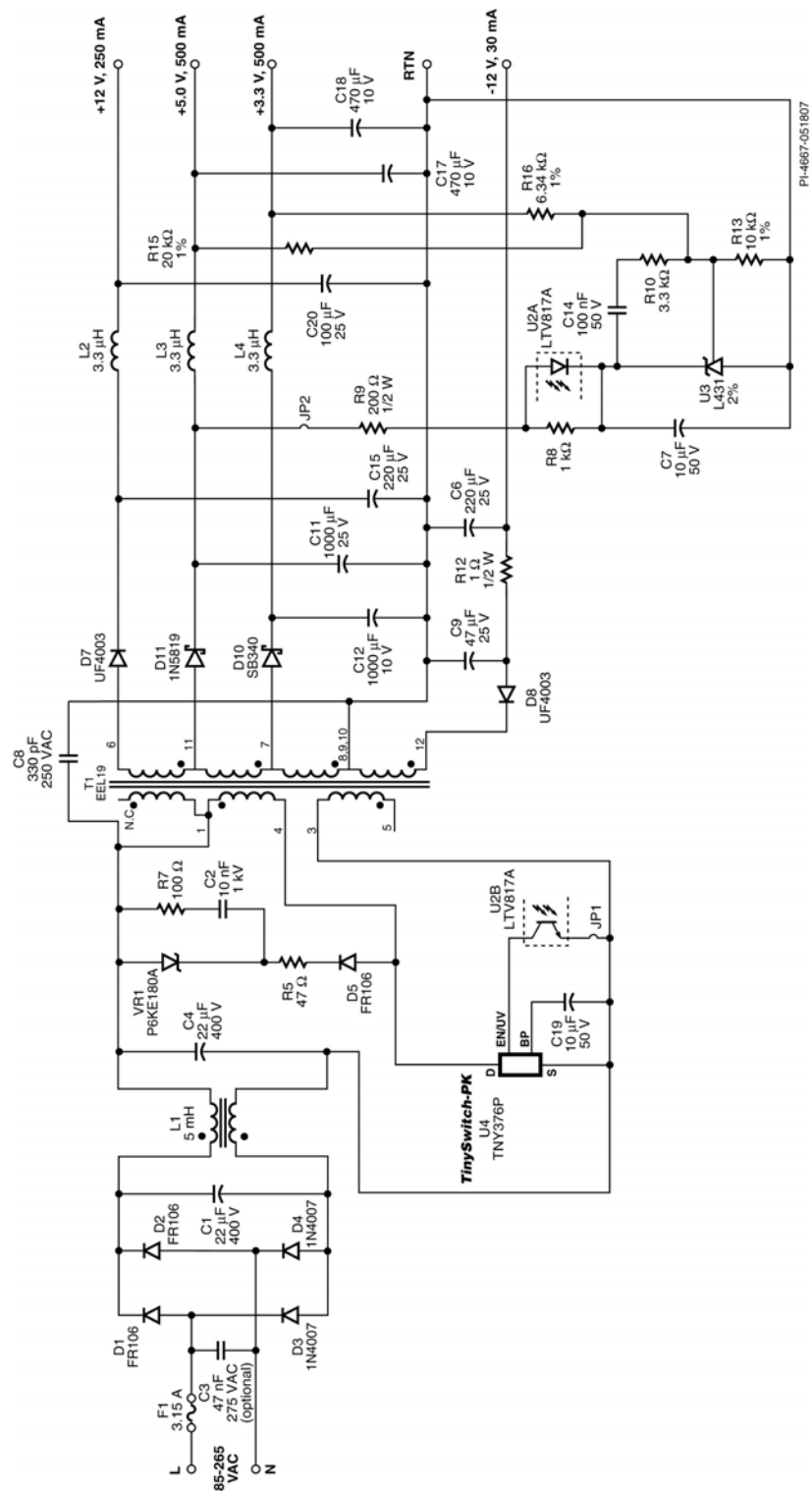


Figure 1 – Populated Circuit Board Photograph.

2 Power Supply Specification

| Description | Symbol | Min | Typ | Max | Units | Comment | |
|-------------------------------|-----------------------|--|-------|-------|-------|--|--|
| Input | | | | | | | |
| Voltage | V _{IN} | 85 | | 265 | VAC | 2 Wire – no P.E. | |
| Frequency | f _{LINE} | 47 | 50/60 | 64 | Hz | | |
| No-load Input Power (230 VAC) | | | | 0.3 | W | | |
| Output | | | | | | | |
| Output Voltage 1 | V _{OUT1} | 3.135 | 3.3 | 3.465 | V | ± 5% | |
| Output Ripple Voltage 1 | V _{RIPPLE1} | | | 100 | mV | 20 MHz bandwidth | |
| Output Current 1 | I _{OUT1} | 0.1 | 0.5 | 0.6 | A | | |
| Output Voltage 2 | V _{OUT2} | 4.75 | 5.0 | 5.35 | V | +7%,-5% | |
| Output Ripple Voltage 2 | V _{RIPPLE2} | | | 66 | mV | 20 MHz bandwidth | |
| Output Current 2 | I _{OUT2} | 0.2 | 0.5 | 0.6 | A | | |
| Output Voltage 3 | V _{OUT3} | 10.8 | 12.0 | 13.8 | V | +15%, -10% | |
| Output Ripple Voltage 3 | V _{RIPPLE3} | | | 240 | mV | 20 MHz bandwidth | |
| Output Current 3 | I _{OUT3} | 0.1 | 0.25 | 0.64 | A | | |
| Output Voltage 4 | V _{OUT4} | -10.8 | -12.0 | -13.8 | V | +15%, -10% | |
| Output Ripple Voltage 4 | V _{RIPPLE4} | | | 240 | mV | 20 MHz bandwidth | |
| Output Current 4 | I _{OUT4} | 0.03 | 0.03 | 0.03 | A | | |
| Total Output Power | | | | | | | |
| Continuous Output Power | P _{OUT} | | 7.51 | | W | | |
| Peak Output Power | P _{OUT PEAK} | | 13 | | W | | |
| Efficiency | | | | | | | |
| Standby input power | P _{sb} | | | 1 | W | P _{out} = 0.5 W, 264 VAC | |
| No load input power | P _{no load} | | | 300 | mW | 264 VAC | |
| Environmental | | | | | | | |
| Conducted EMI | | Meets CISPR22B / EN55022B | | | | 1.2/50 μs surge, IEC 1000-4-5, Class III Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω | |
| Safety | | Designed to meet IEC950, UL1950 Class III | | | | | |
| Surge | | 2 | | | kV | | |
| Surge | | 2.4 | | | kV | 100 kHz ring wave, 200 A short circuit current, 12 ohm common mode; 500 A 2 ohm differential | |
| Ambient Temperature | T _{AMB} | 0 | | 50 | °C | Free convection, sea level | |





4 Circuit Description

4.1 Input EMI Filtering

One requirement of this design was to meet conducted EMI with the output return connected to safety earth ground. This simulates the condition where the DVD player or set-top box is earth grounded either by an antenna or cable TV input cable.

The EMI filtering consists of a π filter formed by C1, L1 and C4 together with capacitor C8. A common mode choke was selected over discrete inductors for L1 to meet the earth grounded requirement. Such a simple arrangement was possible due to the switching frequency jitter feature of U4 and the E-Shield™ techniques used in the transformer. Provision for an additional X class capacitor (C3) is made on the board but is not required.

4.2 TinySwitch-PK Primary

The TNY376 (U4) has the following functions integrated onto a monolithic IC: a 700 V power MOSFET, a low-voltage CMOS controller, a high-voltage current source (provides startup and steady-state operational current to the IC), hysteretic thermal shutdown, and auto-restart. The excellent switching characteristics of the integrated power MOSFET allow efficient operation up to 132 kHz (264 kHz in Peak Power Mode).

Under normal operation, the rectified and filtered input voltage is applied to one side of the primary winding of T1. The other side of the T1 primary winding is connected to the DRAIN pin of U4. As soon as the voltage is applied across the DRAIN and SOURCE pins of U4, the internal high voltage current source (connected to the DRAIN pin of the IC) begins charging the capacitor (C19) connected to the BYPASS/MULTIFUNCTION (BP/M) pin. Once the voltage across C19 reaches 5.8 V, the controller enables MOSFET switching. MOSFET current is sensed (internally) by the voltage developed across the Drain to Source resistance ($R_{DS(ON)}$) while it is turned on. When the current reaches the preset (internal) current-limit trip point (I_{LIMIT}), the controller turns the MOSFET off.

The controller regulates the output voltage by skipping switching cycles (ON/OFF control) whenever the output voltage is above the reference level. During normal operation, MOSFET switching is disabled whenever the current flowing out of the EN/UV pin is greater than 90 μ A. If less than 90 μ A is flowing out of the EN/UV pin when the oscillator's (internal) clock signal occurs, MOSFET switching is enabled for that switching cycle, and the MOSFET turns on. That switching cycle terminates when the current through the MOSFET reaches I_{LIMIT} , or the DC_{MAX} signal is encountered. At full load, few switching cycles will be skipped (disabled) resulting in a high effective switching frequency. As the load reduces, more switching cycles are skipped, which reduces the effective switching frequency. At no-load, most switching cycles are skipped, which is what makes the no-load power consumption of supplies designed around the *TinySwitch-PK* family so low, since switching losses are the dominant loss mechanism at light loading. Additionally, since the amount of energy per switching cycle is fixed by



I_{LIMIT} , the skipping of switching cycles gives the supply a fairly consistent efficiency over the load range.

The *TinySwitch-PK* can supply additional output power to the load for short periods of time. If the MOSFET switching occurs for 14 consecutive clock cycles (132 kHz), the I_{LIMIT} increases, and the MOSFET is enabled to switch at 264 kHz. While in the Peak Power Mode of operation, if the MOSFET is disabled (via the feedback loop) for 12 consecutive clock cycles (264 kHz), then the *TinySwitch-PK* reverts back to its normal mode of operation at 132 kHz.

To limit the peak drain voltage spike caused by leakage inductance D5, R5, VR1, R7 and C2 form a clamp network. This arrangement offers the low EMI performance of an RCD clamp with the energy efficiency of a Zener clamp. By limiting the voltage across R7 and C2 using a Zener, the clamp voltage does not collapse as the output load, and therefore effective switching frequency, reduces. This prevents the clamp becoming a significant load at light load and therefore maintains high efficiency and low no-load input power.

4.3 Output Feedback

The output voltages of the +3.3 V and +5 V outputs are regulated by the sum of the currents through R15 and R16. The combined currents passing through R13 are regulated at 2.5 Volts by U3. If the voltage changes across R13, U3 changes the current through U2A (opto's LED), which proportionately changes the current through U2B (opto's transistor). If the collector current of U2B is greater than 90 μ A, U4 will skip the next switching cycle. If not, the switching cycle will occur. Sensing the outputs voltages via R15 and R16 helps improve the cross regulation between these outputs. The ± 12 V outputs are cross regulated via the transformer's turns ratios. Optional capacitor C7 provides soft-finish, reducing the output voltage slew rate at start-up.

4.4 Bypass/Multifunction Pin

The *TinySwitch-PK*'s BP/M pin can be used to set the peak current limit of the primary switching cycle. This allows the designer more flexibility to optimize the power supply for the specific power range. Setting the current limit is done by selecting a capacitor value that is connected to the BP/M pin. The selection sizes are: 1.0 μ F, 0.1 μ F and 10 μ F. This sets the peak current threshold to the minimum, typical, and maximum level. Refer to the data sheet for the specific current limit for each *TinySwitch-PK* device.



5 PCB Layout

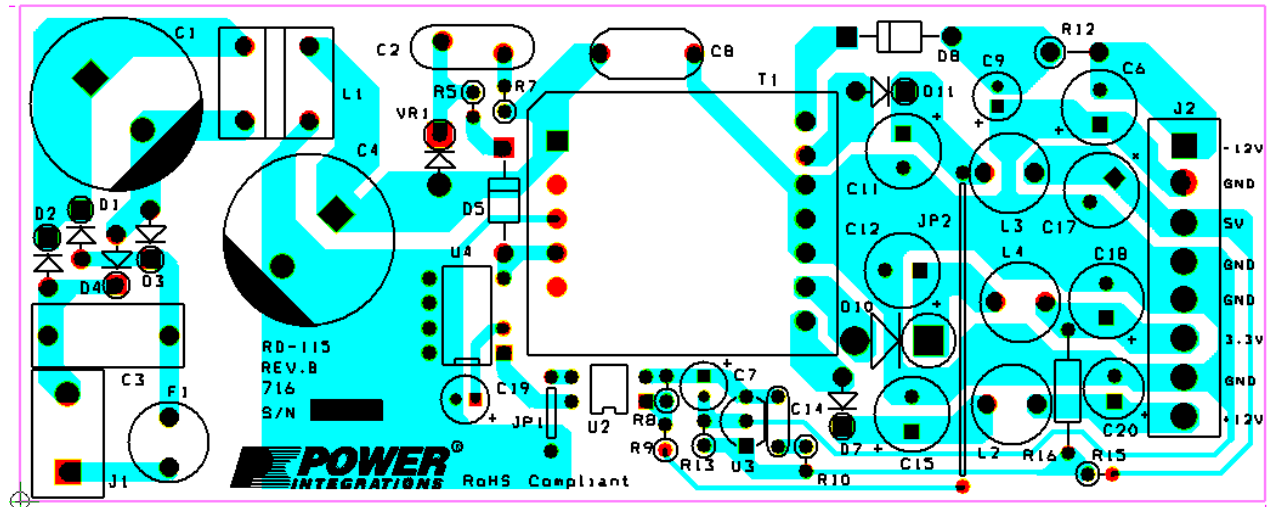


Figure 3 – Printed Circuit Layout.



6 Bill of Materials

| Item | Qty | Part Reference | Value | Description | Mfg Part Number | Mfg |
|------|-----|----------------|--------------|--|--------------------|------------------|
| 1 | 2 | C1 C4 | 22 μ F | 22 μ F, 400 V, Electrolytic, Low ESR, 901 m Ω , (16 x 20) | EKMX401ELL220ML20S | Nippon Chemi-Con |
| 2 | 1 | C2 | 10 nF | 10 nF, 1 kV, Disc Ceramic | 562R5HKMS10 | Vishay/Sprague |
| 3 | 1 | C3 | 47 nF | 47 nF, 275 VAC, Film, X2 | ECQU2A473ML | Panasonic |
| 4 | 2 | C6 C15 | 220 μ F | 220 μ F, 25 V, Electrolytic, Very Low ESR, 72 m Ω , (8 x 11.5) | EKZE250ELL221MHB5D | Nippon Chemi-Con |
| 5 | 2 | C7 C19 | 10 μ F | 10 μ F, 50 V, Electrolytic, Gen. Purpose, (5 x 11) | EKMG500ELL100ME11D | Nippon Chemi-Con |
| 6 | 1 | C8 | 330 pF | 330 pF, Ceramic Y1 | 440LT33-R | Vishay |
| 7 | 1 | C9 | 47 μ F | 47 μ F, 25 V, Electrolytic, Very Low ESR, 300 m Ω , (5 x 11) | EKZE250ELL470ME11D | Nippon Chemi-Con |
| 8 | 2 | C11 C12 | 1000 μ F | 1000 μ F, 10 V, Electrolytic, Very Low ESR, 41 m Ω , (8 x 20) | EKZE100ELL102MH20D | Nippon Chemi-Con |
| 9 | 1 | C14 | 100 nF | 100 nF, 50 V, Ceramic, Z5U, .2 Lead Space | C317C104M5U5TA | Kemet |
| 10 | 2 | C17 C18 | 470 μ F | 470 μ F, 10 V, Electrolytic, Very Low ESR, 72 m Ω , (8 x 11.5) | EKZE100ELL471MHB5D | Nippon Chemi-Con |
| 11 | 1 | C20 | 100 μ F | 100 μ F, 25 V, Electrolytic, Very Low ESR, 130 m Ω , (6.3 x 11) | EKZE250ELL101MF11D | Nippon Chemi-Con |
| 12 | 3 | D1 D2 D5 | FR106 | 800 V, 1 A, Fast Recovery Diode, 500 ns, DO-41 | FR106 | Diodes Inc. |
| 13 | 2 | D3 D4 | 1N4007 | 1000 V, 1 A, Rectifier, DO-41 | 1N4007 | Vishay |
| 14 | 2 | D7 D8 | UF4003 | 200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41 | UF4003-E3 | Vishay |
| 15 | 1 | D10 | SB340 | 40 V, 3 A, Schottky, DO-201AD | SB340-E3 | Vishay |
| 16 | 1 | D11 | 1N5819 | 40 V, 1 A, Schottky, DO-41 | 1N5819-E3 | Vishay |
| 17 | 1 | F1 | 3.15 A | 3.15 A, 250 V, Fast, TR5 | 37013150410 | Wickman |
| 18 | 1 | J1 | CON2 | 2 Position (1 x 2) header, 0.312 pitch, Vertical | 26-50-3039 | Molex |



| | | | | | | |
|----|---|----------|-----------|--|---|---|
| 19 | 1 | J2 | CON8 | 8 Position (1 x 8) header, 0.156 pitch, Vertical | 26-48-1081 | Molex |
| 20 | 1 | JP1 | J | Wire Jumper, insulated, 22 AWG, 0.3 in, | 298 | Alpha |
| 21 | 1 | JP2 | J | Wire Jumper, insulated, 22 AWG, 1.3 in | 298 | Alpha |
| 22 | 1 | L1 | 5 mH | 5 mH, 0.3 A, Common Mode Choke | HT9V-03050 | CUI |
| 23 | 3 | L2 L3 L4 | 3.3 uH | 3.3 uH, 5.5 A | RL622-3R3K-RC | JW Miller |
| 24 | 1 | R5 | 47 | 47 R, 5%, 1/4 W, Carbon Film | CFR-25JB-47R | Yageo |
| 25 | 1 | R7 | 100 | 100 R, 5%, 1/4 W, Carbon Film | CFR-25JB-100R | Yageo |
| 26 | 1 | R8 | 1 k | 1 k, 5%, 1/4 W, Carbon Film | CFR-25JB-1K0 | Yageo |
| 27 | 1 | R9 | 200 | 200 R, 5%, 1/4 W, Carbon Film | CFR-25JB-200R | Yageo |
| 28 | 1 | R10 | 3.3 k | 3.3 k, 5%, 1/4 W, Carbon Film | CFR-25JB-3K3 | Yageo |
| 29 | 1 | R12 | 1 | 1 R, 5%, 1/2 W, Carbon Film | CFR-50JB-1R0 | Yageo |
| 30 | 1 | R13 | 10 k | 10 k, 1%, 1/4 W, Metal Film | ERO-S2PHF1002 | Panasonic |
| 31 | 1 | R15 | 20 k | 20 k, 1%, 1/4 W, Metal Film | MFR-25FBF-20K0 | Yageo |
| 32 | 1 | R16 | 6.34 k | 6.34 k, 1%, 1/4 W, Metal Film | MFR-25FBF-6K34 | Yageo |
| 33 | 1 | T1 | EEL19 | Bobbin, EEL19, Horizontal, 12 pins (5 x 7) | Bobbin CWS-T1-DAK-115 SIL6041 TELP-32280-0001 R1396 | Ngai Cheong Elect Ltd CWS Hical Precision Santronics |
| 34 | 1 | U2 | LTV817A | Optocoupler, 35 V, CTR 80-160%, 4-DIP | LTV-817A | Liteon |
| 35 | 1 | U3 | TL431 | 2.495 V Shunt Regulator IC, 2%, 0 °C to 70 °C, TO-92 | TL431CLPG | On Semiconductor |
| 36 | 1 | U4 | TNY376P | TinySwitch-PK, TNY376P, DIP-8C | TNY376P | Power Integrations |
| 37 | 1 | VR1 | P6KE180 A | 180 V, 5 W, 5%, TVS, DO204AC (DO-15) | P6KE180ARLG | On Semi |

***A TNY375P can be used for U4, with a reduced power output. See Appendix A in this report.**

Note: Parts listed above are RoHS compliant.



7 Transformer Specification

7.1 Electrical Diagram

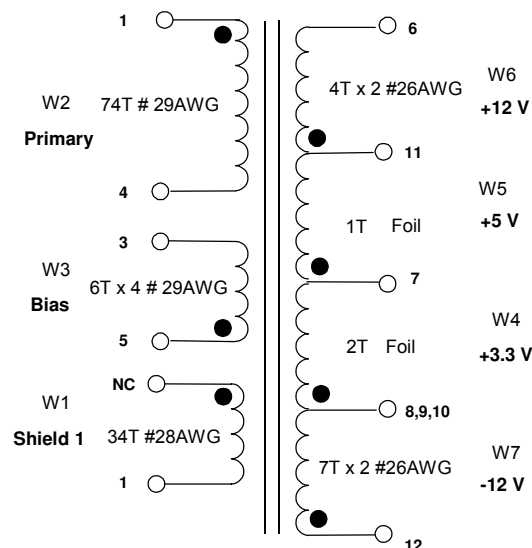


Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

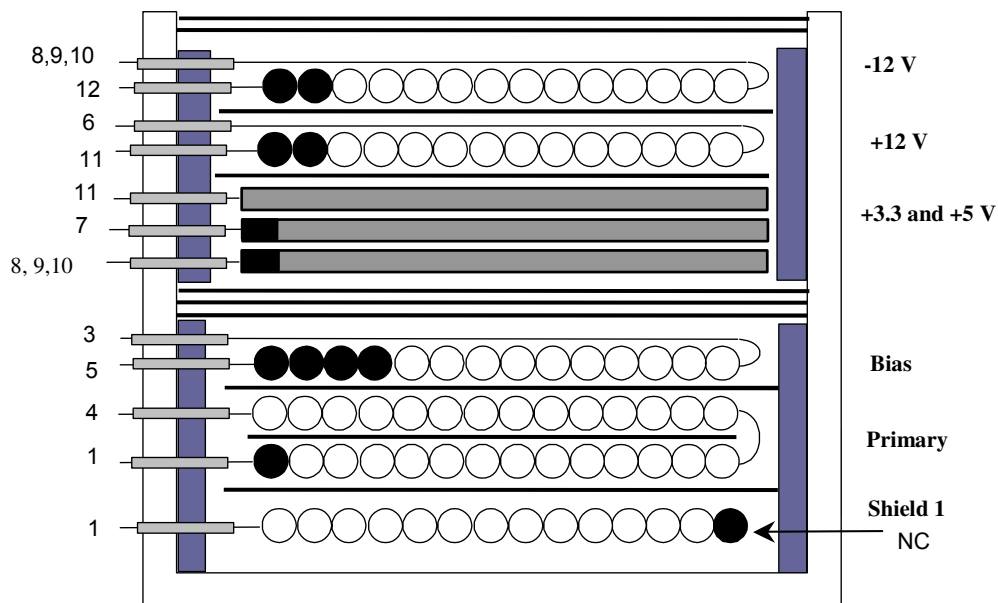
| | | |
|-----------------------------------|---|------------------|
| Electrical Strength | 60Hz 1 second, from Pins 1-5 to Pins 6-12 | 3000 V ac |
| Primary Inductance | Pin 1 to Pin 4, all other windings open Measured at 132 kHz. | 0.813 mH +/- 12% |
| Resonant Frequency | Pin 1 to Pin 4, all other windings open | 300 kHz (Min.) |
| Primary Leakage Inductance | Pin 1 to Pin 4, Pins 6-12 shorted | 30 μ H Max. |

7.3 Materials

| Item | Description |
|------|--|
| [1] | Core: EEL19, Nicera NC-2H or equiv. gapped for AL of 150 nH/T ² |
| [2] | Bobbin: EEL19 Horizontal 12 pins |
| [3] | Magnet Wire: # 28 AWG |
| [4] | Magnet Wire: # 29 AWG |
| [5] | Magnet Wire: # 26 AWG |
| [6] | Teflon Tubing # 22 |
| [7] | Margin Tape: 3M # 44 Polyester web. 3.0 mm wide |
| [8] | Copper Foil 0.52 mm thick, 12 mm wide. |
| [9] | Tape for Copper 2.0 mils thick, 16 mm wide. |
| [10] | Tape: 3M 1298 Polyester Film, 12.8 mm wide |
| [11] | Tape: 3M 1298 Polyester Film, 18.2 mm wide |
| [12] | Varnish |

7.4 Transformer Build Diagram

Pin Side



NC = No Connection to a pin

Figure 5 – Transformer Build Diagram.

7.5 Copper Foil Preparation

The following figure shows the copper foils to be used for +3.3 V and +5 V outputs (W4 and W5)

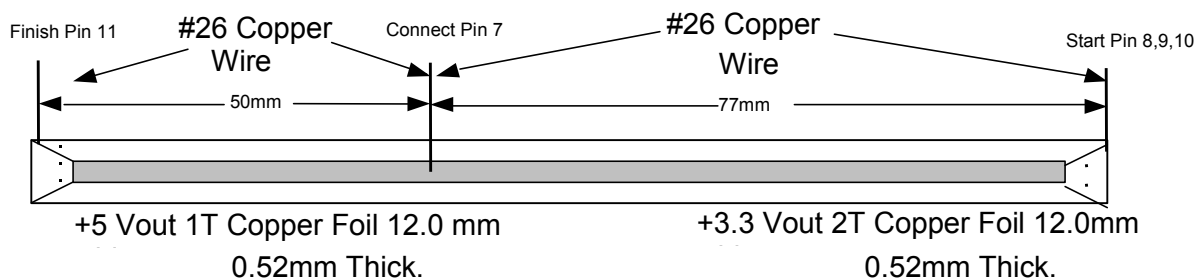


Figure 6 – Copper Foil Diagram.



7.6 Transformer Construction

| | |
|---|--|
| Bobbin Set Up Orientation | Set up the bobbin with pin #1 oriented to the left-hand side. |
| Margin Tape | Apply 3.0 mm margin at each side of bobbin using item [7]. Match combined height of primary, shield and bias windings. |
| W1 Shield 1 | Start with a floating lead temporary tie on pin 8. Wind 34 turns of item [3] from right to left. Wind tightly and uniformly across entire width of bobbin. Finish at pin 1 using item [6] at the finish leads. Remove the wire from pin 8 and cut the starting lead just at the starting of the winding. |
| Basic Insulation | Apply one layer of tape item [10]. |
| W2 Two Layers Primary | Start on pin 1 using item [6] at the start leads. Wind 37 turns of item [4] from left to right. Apply one layer of item [10]. Continue the same wire on second layer. Wind 37 turns from right to left. The two layers should be wound tightly with the turns uniformly distributed across entire width of bobbin. Finish on pin 4 using item [6] at the finish leads. |
| Basic Insulation | Apply one layer of tape item [10]. |
| W3 Bias | Start on pin 5 using item [6] at the start leads. Wind 6 turns of 4 parallel wires of item [4]. Wind from left to right in a single layer. The wires should be tightly and uniformly wound spread across the bobbin width. Finish on pin 3 using item [6] at the finish leads. |
| Insulation | Apply 3 Layers of tape [11] for insulation. |
| Margin Tape | Apply 3.0 mm margin at each side of bobbin using item [7]. Match combines height of secondary windings. |
| W4 and W5 +3.3 V and +5 V outputs. | Prepare copper foil item [8] and item [9] as shown in figure 6. Start at pin 8,9,10 using item [6] at the start leads. Wind 2 turns. Connect the second lead to pin 7 using item [6] at the finish leads; wind 1 turn. Connect the end lead to pin 11 using item [6] at the finish leads. |
| Basic Insulation | Apply one layer of tape item [10]. |
| W6 +12 V out | Start on pin 11 using item [6] at the start leads. Wind 4 turns of Bifilar wires of item [5]. Wind from right to left in a single tightly wound spread across the bobbin width. Finish on pin 6 using item [6] at the finish leads. |
| Basic Insulation | Apply one layer of tape item [10]. |
| W7 -12 V output. | Start at pin 12 using item [6] at the start leads. Wind 7 turns of Bifilar wires of item [5]. Wind from right to left in a uniform and tightly wound spread across the bobbin width. Finish on pin 8,9,10 using item [6] at the finish leads. |
| Outer Insulation | 2 Layers of tape [11] for insulation. |
| Core Assembly | Assemble and secure core halves. Item [1] |
| Final Assembly | Dip Varnish uniformly in item [12]. |



8 Design Spreadsheet

| ACDC_TinySwitch-PK_041207; Rev.0.22; Copyright Power Integrations 2007 | INPUT | INFO | OUTPUT | UNIT | ACDC_TinySwitch-PK_041207_Rev0-22.xls; TinySwitch-PK Continuous/Discontinuous Flyback Transformer Design Spreadsheet |
|--|--------|--------|-------------------------|--------------------|--|
| ENTER APPLICATION VARIABLES | | | | | |
| VACMIN | 85 | | | Volts | Minimum AC Input Voltage |
| VACMAX | 265 | | | Volts | Maximum AC Input Voltage |
| fL | 50 | | | Hertz | AC Mains Frequency |
| VO | 5.00 | | | Volts | Output Voltage (at continuous power) |
| Peak Load Current, IO | 2.60 | | | Amps | Power Supply Output Current (corresponding to peak power) |
| Peak Power | | | 13.00 | Watts | Peak Output Power. Used in estimation of Primary inductance |
| Continuous / Average Power | 7.5 | | 7.5 | Watts | Continuous/Average Output Power. Used in estimation of Core size |
| n | 0.67 | | | | Efficiency Estimate at output terminals. Under 0.7 if no better data available |
| Z | | | 0.6 | | Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.6 if no better data available |
| tC | 3.00 | | | mSeconds | Bridge Rectifier Conduction Time Estimate |
| CIN | 44.00 | | 44 | uFarads | Input Capacitance |
| ENTER TinySwitch-PK VARIABLES | | | | | |
| TinySwitch-PK | TNY376 | | TNY376 | | User defined TinySwitch-PK |
| Chosen Device | | TNY376 | | | |
| Chose Configuration | INC | | Increased Current Limit | | Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications) |
| ILIMITMIN | | | 0.465 | Amps | Minimum Current Limit |
| ILIMITTYP | | | 0.500 | Amps | |
| ILIMITMAX | | | 0.535 | Amps | Maximum Current Limit |
| fSmin | | | 248000 | Hertz | Minimum Device Switching Frequency |
| I ² fmin | | | 59.40 | A ² kHz | I ² f (product of current limit squared and frequency is trimmed for tighter tolerance) |
| PO_132kHz | | | 8.77 | Watts | Estimated Maximum Power while still in 132 kHz operation |
| VOR | 135.00 | | 135 | Volts | Reflected Output Voltage (VOR < 135 V Recommended) |
| VDS | | | 10 | Volts | TinySwitch-PK on-state Drain to Source Voltage |
| VD | | | 0.5 | Volts | Output Winding Diode Forward Voltage Drop |
| KP | | | 0.53 | | Ripple to Peak Current Ratio (KP < 6) |
| KP_TRANSIENT | | | 0.36 | | Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25 |
| ENTER BIAS WINDING VARIABLES | | | | | |
| VB | | | 22.00 | Volts | Bias Winding Voltage |
| VDB | | | 0.70 | Volts | |
| NB | | | 12.00 | | Bias Winding Number of Turns |
| VZOV | | | 28.00 | Volts | Over Voltage Protection zener diode. |
| UVLO VARIABLES | | | | | |
| V_UV_TARGET | | | 100.07 | Volts | Target under-voltage threshold, above which the power supply will start |
| V_UV_ACTUAL | | | 914.70 | Volts | Typical start-up voltage based on standard value of RUV_ACTUAL |
| RUV_IDEAL | | | 3.91 | Mohms | Calculated value for UV Lockout resistor |
| RUV_ACTUAL | | | 36.50 | Mohms | Closest standard value of resistor to RUV_IDEAL |
| ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES | | | | | |
| Core Type | EEL19 | | EEL19 | | User defined Core Size (Verify thermal performance under |



| | | | | | |
|---|------|--------------|--------|-----------|--|
| | | | | | continuous load conditions) |
| Core | | EEL19 | | P/N: | PC40EE19/27/5-Z |
| Bobbin | | EEL19_BOBBIN | | P/N: | EEL19_BOBBIN |
| AE | | | 0.2454 | cm^2 | Core Effective Cross Sectional Area |
| LE | | | 6.185 | cm | Core Effective Path Length |
| AL | | | 720 | nH/T^2 | Ungapped Core Effective Inductance |
| BW | | | 19.7 | mm | Bobbin Physical Winding Width |
| M | 3.00 | | 3 | mm | Safety Margin Width (Half the Primary to Secondary Creepage Distance) |
| L | 2.00 | | 2 | | Number of Primary Layers |
| NS | | | 3 | | Number of Secondary Turns |
| DC INPUT VOLTAGE PARAMETERS | | | | | |
| VMIN | | | 91 | Volts | Minimum DC Input Voltage |
| VMAX | | | 375 | Volts | Maximum DC Input Voltage |
| CURRENT WAVEFORM SHAPE PARAMETERS | | | | | |
| DMAX | | | 0.63 | | Duty Ratio at full load, minimum primary inductance and minimum input voltage |
| IAVG | | | 0.24 | Amps | Average Primary Current |
| IP | | | 0.47 | Amps | Minimum Peak Primary Current |
| IR | | | 0.25 | Amps | Primary Ripple Current |
| IRMS | | | 0.32 | Amps | Primary RMS Current |
| TRANSFORMER PRIMARY DESIGN PARAMETERS | | | | | |
| LP | | | 813 | uHenries | Typical Primary Inductance. +/- 12% to ensure a minimum primary inductance of 725 uH |
| LP_TOLERANCE | | | 12 | % | Primary inductance tolerance |
| NP | | | 74 | | Primary Winding Number of Turns |
| ALG | | | 150 | nH/T^2 | Gapped Core Effective Inductance |
| BM | | | 2406 | Gauss | Maximum Operating Flux Density at LP_TYP and ILIMITMAX, BM<3200 is recommended |
| BAC | | | 641 | Gauss | AC Flux Density for Core Loss Curves (0.5 X Peak to Peak) |
| ur | | | 1444 | | Relative Permeability of Ungapped Core |
| LG | | | 0.16 | mm | Gap Length (Lg > 0.1 mm) |
| BWE | | | 27.4 | mm | Effective Bobbin Width |
| OD | | | 0.37 | mm | Maximum Primary Wire Diameter including insulation |
| INS | | | 0.06 | mm | Estimated Total Insulation Thickness (= 2 * film thickness) |
| DIA | | | 0.31 | mm | Bare conductor diameter |
| AWG | | | 29 | AWG | Primary Wire Gauge (Rounded to next smaller standard AWG value) |
| CM | | | 128 | Cmils | Bare conductor effective area in circular mils |
| CMA | | | 404 | Cmils/Amp | Primary Winding Current Capacity (200 < CMA < 500) |
| TRANSFORMER SECONDARY DESIGN PARAMETERS | | | | | |
| Lumped parameters | | | | | |
| ISP | | | 11.41 | Amps | Peak Secondary Current |
| ISRMS | | | 6.03 | Amps | Secondary RMS Current |
| IRIPPLE | | | 5.44 | Amps | Output Capacitor RMS Ripple Current |
| CMS | | | 1206 | Cmils | Secondary Bare Conductor minimum circular mils |
| AWGS | | | 19 | AWG | Secondary Wire Gauge (Rounded up to next larger standard AWG value) |
| VOLTAGE STRESS PARAMETERS | | | | | |
| VDRAIN | | | 678 | Volts | Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance) |
| PIVS | | | 20 | Volts | Output Rectifier Maximum Peak Inverse Voltage |



9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

9.1 Efficiency

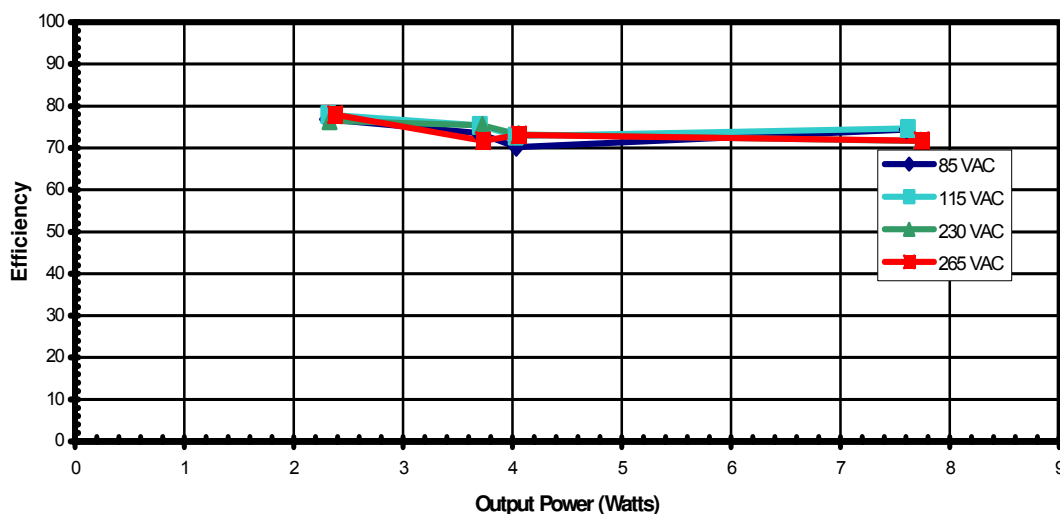


Figure 7 – Efficiency vs. Output Power, Room Temperature, 60 Hz.

9.1.1 Active Mode CEC Measurement Data

All single output adapters, including those provided with products, for sale in California after Jan 1st, 2007 must meet the California Energy Commission (CEC) requirement for minimum active mode efficiency and no load input power. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of rated output power with the limit based on the nameplate output power:

| Nameplate Output (P_O) | Minimum Efficiency in Active Mode of Operation |
|--|---|
| $< 1\text{ W}$ | $0.49 \times P_O$ |
| $\geq 1\text{ W to } \leq 49\text{ W}$ | $0.09 \times \ln(P_O) + 0.5$ [ln = natural log] |
| $> 49\text{ W}$ | 0.84 W |

For adapters that are single input voltage only, the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC); for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).



To meet the standard, the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the CEC/Energy Star standard.

| Percent of Full Load | Efficiency (%) | |
|--|----------------|---------|
| | 115 VAC | 230 VAC |
| 25 | 83.9 | 78.2 |
| 50 | 78.2 | 73.5 |
| 75 | 75.0 | 74.2 |
| 100 | 73.8 | 73.1 |
| Average | 77.7 | 74.8 |
| CEC specified minimum average efficiency (%) | 68.1 | |

More states within the USA and other countries are adopting this standard; for the latest up to date information please visit the PI Green Room:

<http://www.powerint.com/greenroom/regulations.htm>

9.2 No-load Input Power

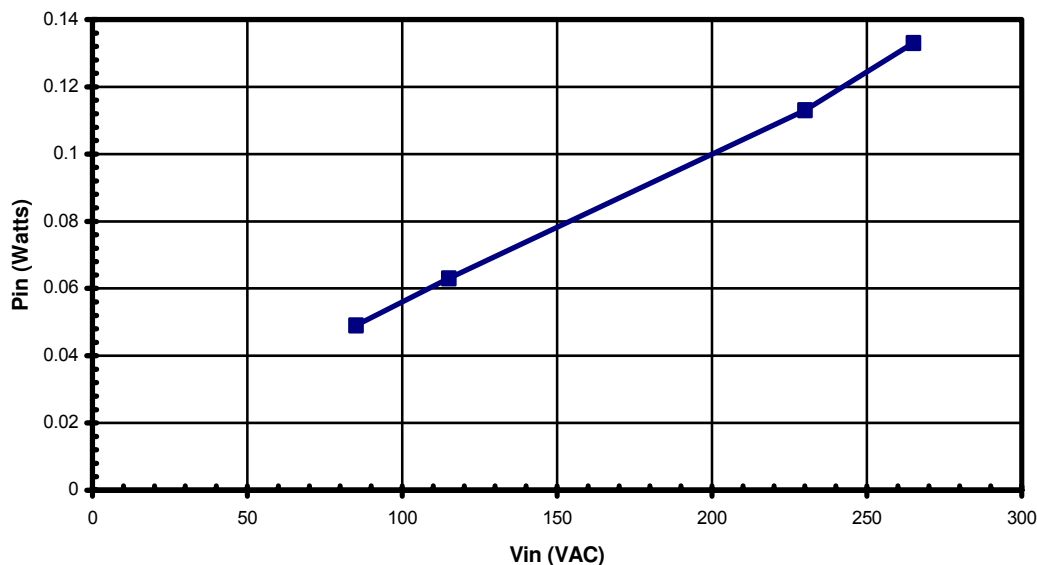


Figure 8 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.



9.3 Available Standby Output Power

The chart below shows the available output power vs line voltage for an input power of 1 W, 2 W and 3 W.

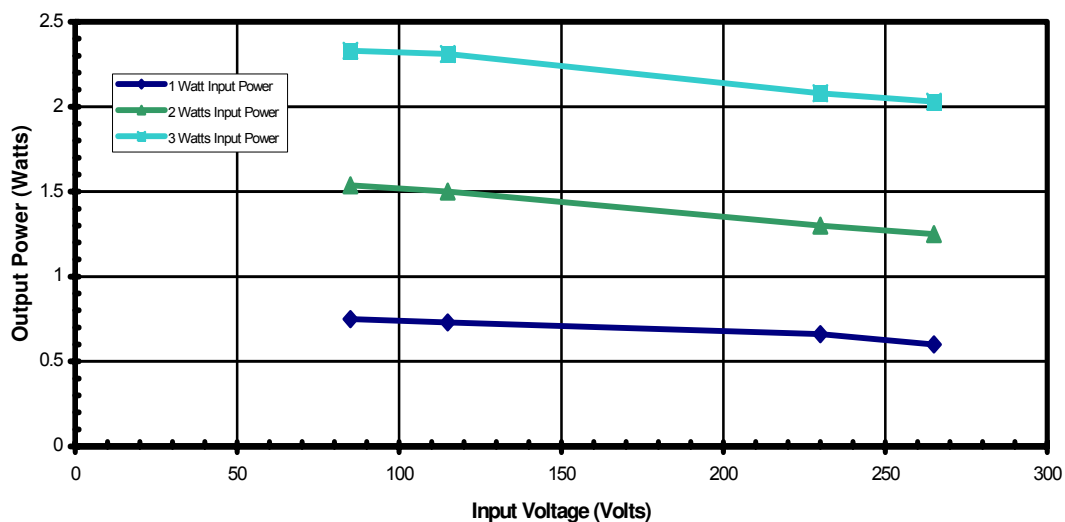


Figure 9 – Output Power vs. Line Voltage.



9.4 Regulation

9.4.1 Load Regulation, Room Temperature, 115 VAC input

These results represent the total variation as all outputs are swept from minimum to maximum load.

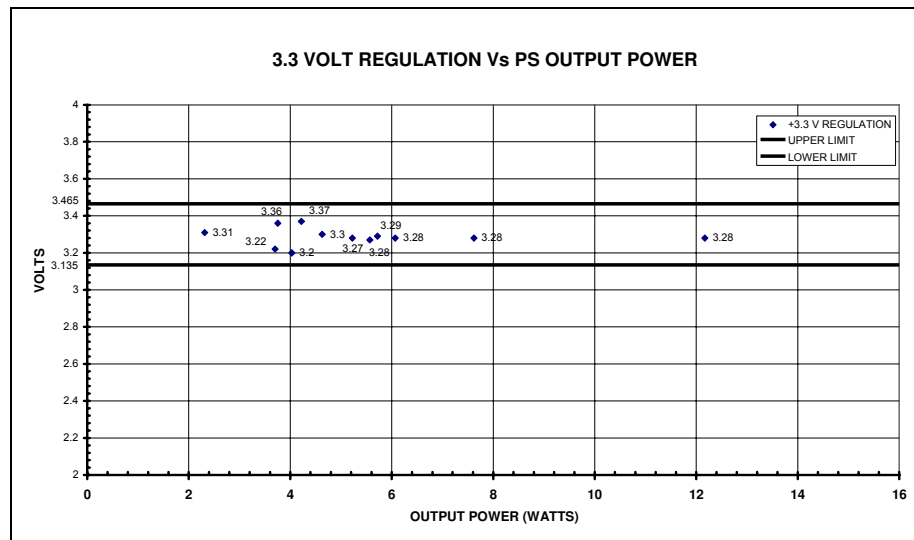


Figure 10 – 3.3 V Regulation vs. total output power.

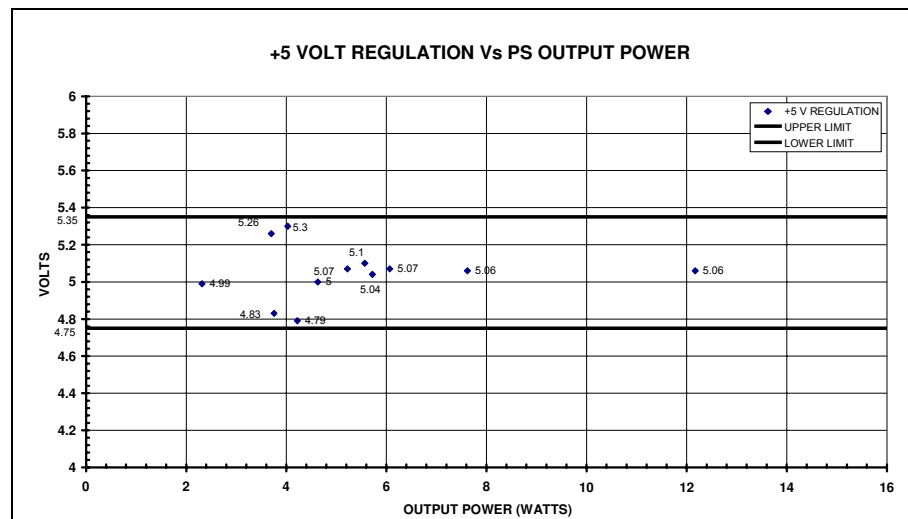


Figure 11 – 5.0 V Regulation vs. total output power.



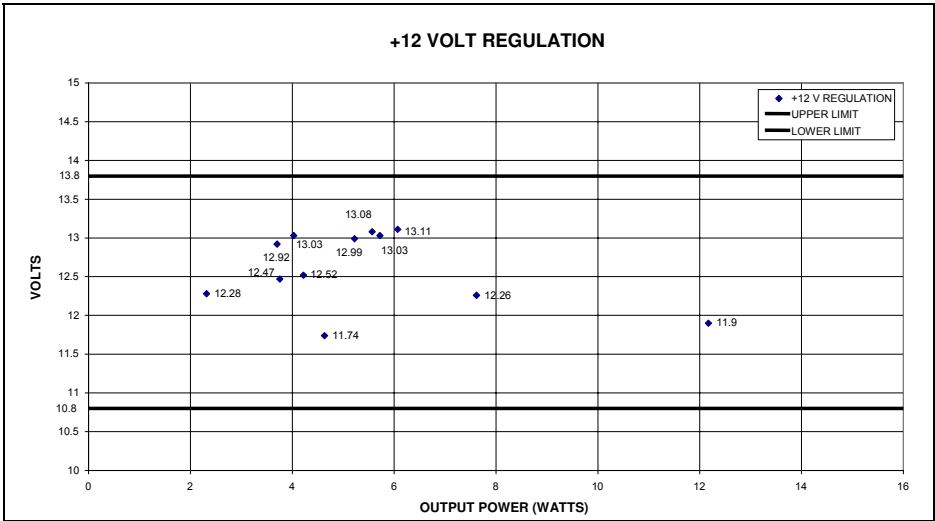


Figure 12 – +12 V Regulation vs. total output power.

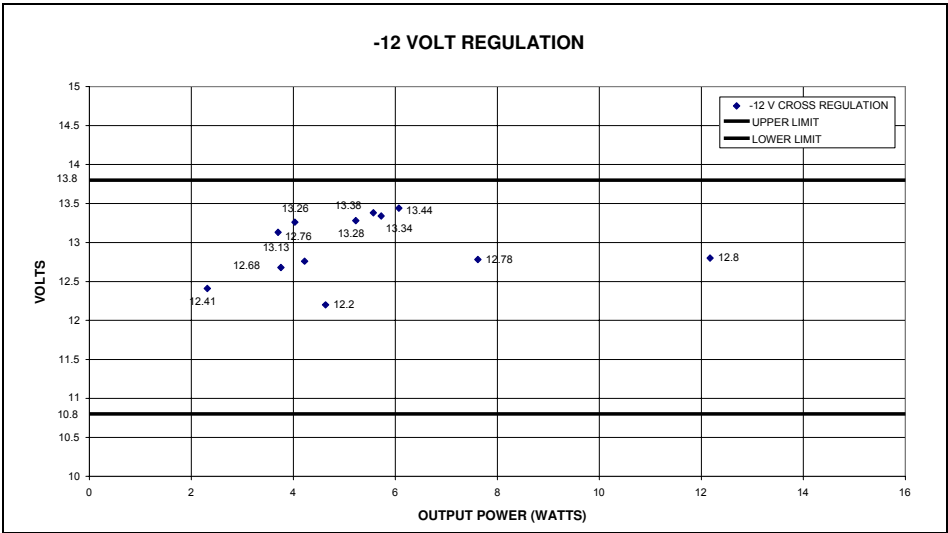
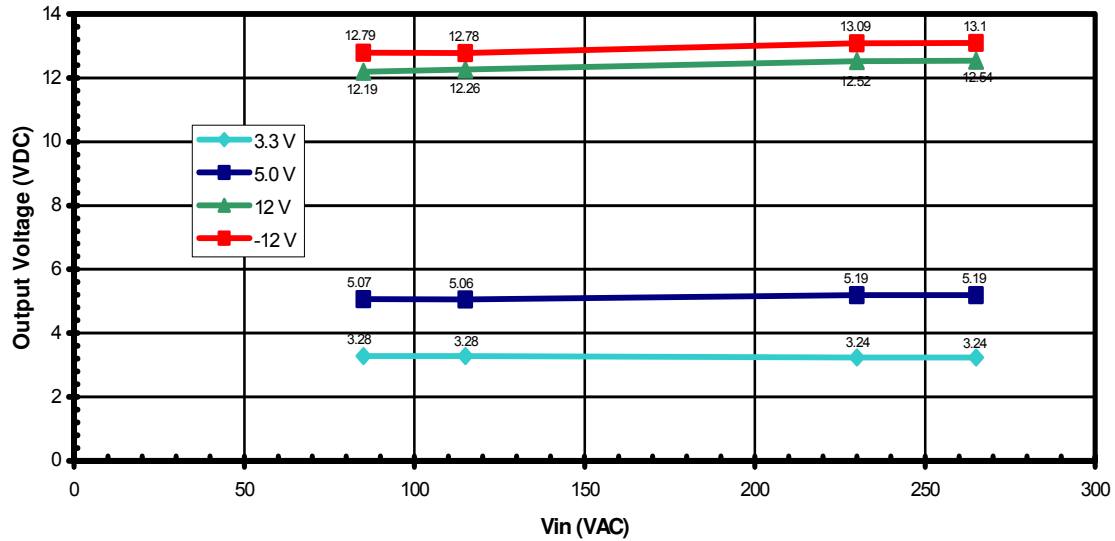


Figure 13 – -12 V Regulation vs. total output power.



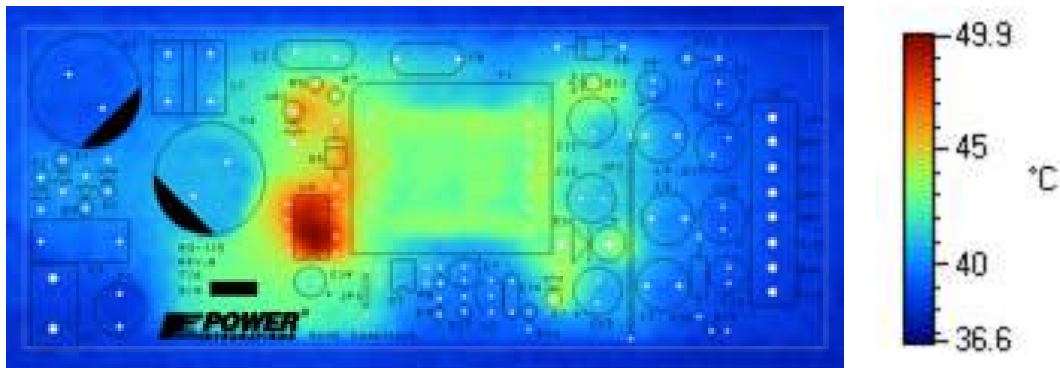
9.4.2 Line

**Figure 14** – Line Regulation, Room Temperature, Full Load.

10 Thermal Performance

Output was loaded to 7.51 W. RD-115 was housed in the intended enclosure, which was within a box inside the thermal test chamber (no air flow permitted). Ambient temperature was measured inside the enclosure. Test chamber temperature was set to 50 °C.

| Item | Temperature (°C) | | |
|-------------|------------------|---------|---------|
| | 85 VAC | 115 VAC | 230 VAC |
| Ambient | 54.5 °C | 54 °C | 56.2 °C |
| TNY376 (U4) | 92 °C | 92.6 °C | 94.5 °C |



90 VAC, 7.5 W load, 21°C Ambient

Figure 15 – Infrared Thermograph of Open Frame Operation, at Room Temperature

11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

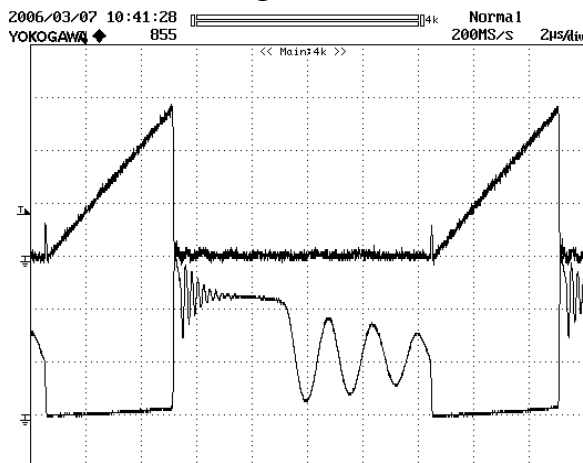


Figure 16 – 85 VAC, Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 100 V, 2 μ s / div.

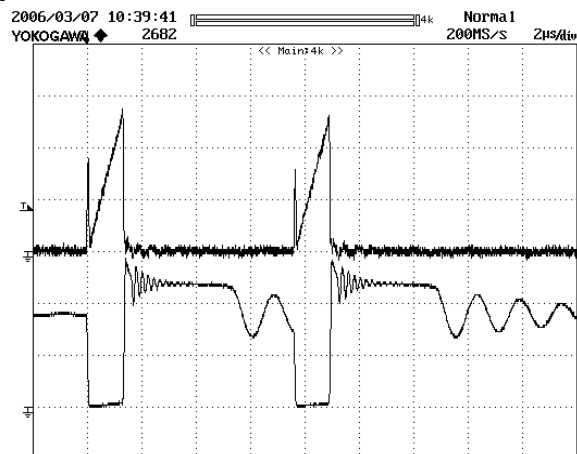


Figure 17 – 265 VAC, Full Load
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.

11.2 Output Voltage Start-up Profile

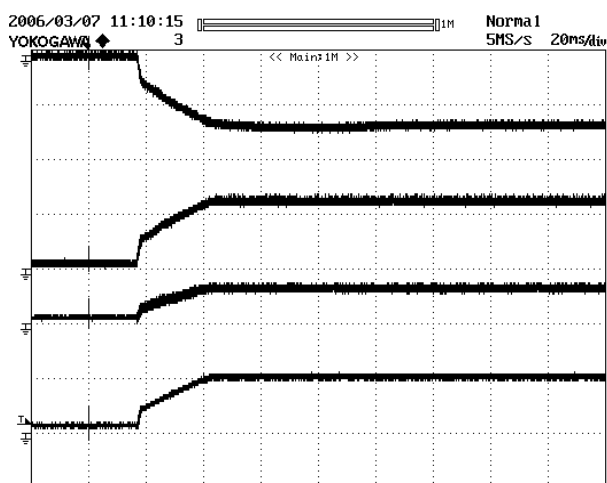


Figure 18 – Start-up Profile, 115 VAC.
Bottom Trace: 5 V Output at 5 V / div.
Next Trace: 3.3 V Output at 5 V / div.
Next Trace: +12 V Output at 10 V / div.
Top Trace: -12 V Output at 10 V / div.
20 ms / div.

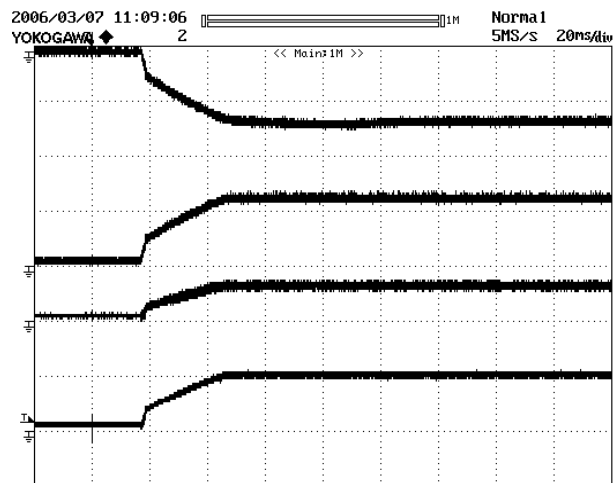


Figure 19 – Start-up Profile, 230 VAC.
Bottom Trace: 5 V Output at 5 V / div.
Next Trace: 3.3 V Output at 5 V / div.
Next Trace: +12 V Output at 10 V / div.
Top Trace: -12 V Output at 10 V / div.
20 ms / div