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Application Note AN-47
TOPSwitch®-JX Family

Design Guide

Introduction

The TOPSwitch-JX is a highly integrated monolithic off-line switcher IC designed for off-line power supplies. TOPSwitch-JX integrated circuits enable design of power supplies up to 244 W, while providing high efficiency under all load conditions. TOPSwitch-JX also provides very good performance at low load and during standby (no-load) operation. The TOPSwitch-JX family allows the designer to easily meet efficiency requirements for the latest energy-efficiency standards. Innovative and proprietary features enable design of compact and cost effective switching power supplies while reducing overall design cycle time and system cost. The TOPSwitch-JX family also enables the design of power supplies with robust functionality and provides enhanced safety features such as output overvoltage protection, overload power limiting and hysteretic thermal protection.

Each member of the family has a high-voltage power MOSFET and its controller combined monolithically. Internal start-up bias current is drawn from a high-voltage current source connected to the DRAIN pin, eliminating the need for external start-up circuitry. The internal oscillator is frequency modulated (jitter) to reduce EMI. In addition, the ICs have integrated functions that provide system-level protection. The auto-restart function limits power dissipation in the MOSFET, the transformer and the output diode during overload, output short circuit or open-loop conditions. The auto-recovering hysteretic thermal shutdown function also disables MOSFET switching if the junction temperature exceeds safe limits. A programmable undervoltage/overvoltage (UV/OV) detection feature allows glitch free start-up and shutdown of the power supply during line sag or line surge conditions. Power Integrations' EcoSmart® technology enables supplies designed around the TOPSwitch-JX family to consume less than 100 mW at no-load and maintain constant efficiency over the full line and load range. TOPSwitch-JX family of solutions easily meets energy efficiency standards such as European Code of Conduct, EC EuP and ENERGY STAR.

Basic Circuit Configuration

The discussion of application-specific requirements, such as constant current, constant power outputs, etc., are beyond the scope of this design guide. However, such requirements may be satisfied by adding additional circuitry to the basic converter descriptions shown here. For more information on additional circuit capabilities, design examples and other information visit the Power Integrations web site or contact your PI sales representative.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the TOPSwitch-JX family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable transformer design. To help simplify the task, the application note refers directly to the PI Xls design spreadsheet that is part of the PI Expert® design software suite available at no charge from

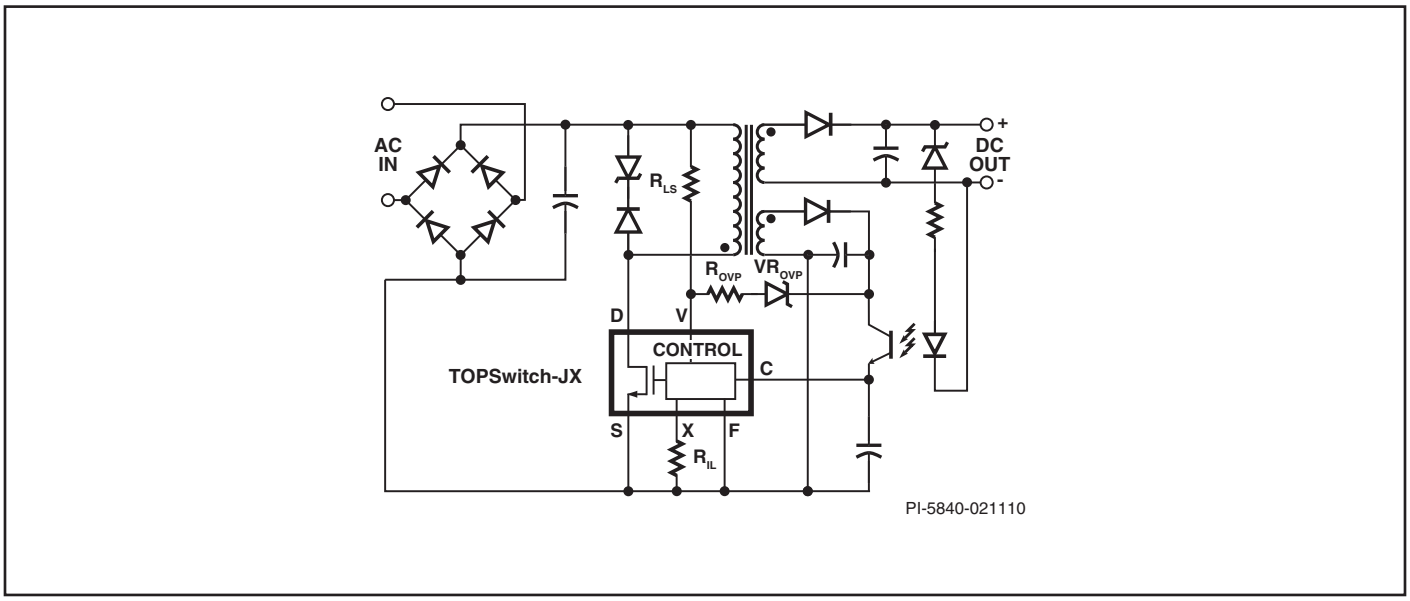


Figure 1. Typical TOPSwitch-JX Flyback Power Supply With Primary Sensed Output Overvoltage Protection, Line Undervoltage Lockout, Line Overvoltage Shutdown and Programmable Current Limit.

www.powerint.com. The basic configuration used in TOPSwitch-JX flyback power supplies is shown in Figure 1, which also serves as the reference circuit for component identifications used in descriptions throughout this application note.

In addition to this application note, the reader may also find the TOPSwitch-JX Reference Design Kits (RDKs) useful. Each contains a fully functional engineering prototype board, engineering report and device samples. Further details on downloading PI Expert, and obtaining an RDK and updates to this document can be found at www.powerint.com.

Quick Start

Readers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach described later, and can use the following information to quickly design the transformer and select the components necessary for a first prototype. For this approach, only the information described below needs to be entered into the PI Xls spreadsheet, other parameters will be automatically selected based on typical design requirements. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter AC input voltage range VAC_{MIN}, VAC_{MAX} and minimum line frequency f_L [B3, B4, B5]
- Enter nominal output voltage V_O [B6]
- For designs with a peak load condition, enter average output power, else enter continuous (average) output power [B7]
- For designs with a peak load current, enter peak load current else leave blank [B8]
- Enter efficiency estimate [B11]
- 0.8 for universal input voltage (85-265 VAC) or single
  - 100/115 VAC (85-132 VAC) and 0.85 for a single 230 VAC (185-265 VAC) design. Adjust the number accordingly based on measurement at peak load and VAC_{MIN}.
- Enter loss allocation factor Z [B12]
  - 0.5 for typical application (adjust the number accordingly after first prototype-board evaluation)
- Enter input capacitance (C_{IN}) [B15]
  - 2~3 µF/W for universal (85-265 VAC) or single (100/115 VAC)
  - Use 1 µF/W single 230 VAC for single (185-265 VAC)
- Select the TOPSwitch-JX part from the drop down list or enter directly [B19]
  - Select the device in the table below according to output power and line input voltage
  - Enter operating frequency – [B24]
  - "H" for 66 kHz operation
  - "F" for 132 kHz operation
- Enter core type (if desired) from drop down menu [B54]
  - A suggested core size will be selected automatically if none is entered
- If any warnings are generated, make changes to the design by following instructions in spreadsheet column F
- Build transformer
- Select key components
- See Steps 7 through 12.
- Build prototype and iterate design as necessary, replacing estimates in the spreadsheets with measured values as appropriate (e.g. efficiency, V_{MIN}).
- Power Integrations offers a transformer prototyping service and links to other vendors: for details see www.powerint.com/componentsuppliers.htm

Output Power Table

Product[5]	PCB Copper Area[1]				Product[5]	Metal Heat Sink[1]			
	230 VAC ±15%[4]		85-265 VAC			230 VAC ±15% [4]		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]		Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
TOP264VG	21 W	34 W	12 W	22.5 W	**TOP264EG/VG**	30 W	62 W	20 W	43 W
TOP265VG	22.5 W	36 W	15 W	25 W	**TOP265EG/VG**	40 W	81 W	26 W	57 W
TOP266VG	24 W	39 W	17 W	28.5 W	**TOP266EG/VG**	60 W	119 W	40 W	86 W
TOP267VG	27.5 W	44 W	19 W	32 W	**TOP267EG/VG**	85 W	137 W	55 W	103 W
TOP268VG	30 W	48 W	21.5 W	36 W	**TOP268EG/VG**	105 W	148 W	70 W	112 W
TOP269VG	32 W	51 W	22.5 W	37.5 W	**TOP269EG/VG**	128 W	162 W	80 W	120 W
TOP270VG	34 W	55 W	24.5 W	41 W	**TOP270EG/VG**	147 W	190 W	93 W	140 W
TOP271VG	36 W	59 W	26 W	43 W	**TOP271EG/VG**	177 W	244 W	118 W	177 W

Table 1. Output Power Table.

Notes:
1. See Key Application Considerations in device data sheet section for more details.
2. Maximum continuous power in a typical non-ventilated enclosed adapter measured at +50 °C ambient temperature.
3. Maximum continuous power in an open frame design at +50 °C ambient temperature.
4. 230 VAC or 110/115 VAC with doubler.
5. Packages: E: eSIP-7C, V: eDIP-12. See Part Ordering Information in device data sheet.

Step-by-Step Transformer Design Procedure Introduction

The design flow allows for design of power supplies both with or without a peak output power requirement. For peak power requirements the device current limit is programmed to enable the delivery of peak power for a short duration limited only by thermal characteristics of the TOPSwitch-JX package and ratings of other components in the circuit.

As average power increases, based on the measured transformer and device temperature, it may be necessary to select a larger transformer to allow increased copper area for the windings and/or to increase the amount of device heatsinking.

The power table (Table 1) provides guidance for peak and continuous (average) power levels obtainable in both sealed adapter and open frame applications. For the V package without an external heatsink, the power values for adapter and open frame are thermally limited. The peak values represent the electrically limited output power, assuming operation at current limit ($I_{LIM(MIN)}$). For the E package, the adapter power values are also thermally limited, however, the open frame values are electrically limited and therefore also represent the peak output power. As the continuous power values are thermally limited, they indicate the upper limit of continuous power for worst case conditions but may vary depending on the specific application. For example, if the peak power condition has a very low duty cycle, such as the 1-second peak required to close the drawer in a DVD player, then the thermal rise of the device (and transformer) is only a function of the continuous average power. However, if the peak power is repetitive with a significant duty cycle, then it would need to be considered as a limiting factor in the design.

Figure 2 shows how to calculate the average power requirements for a design with two different peak load conditions.

$$P_{AVE} = P_1 + (P_3 - P_1) \times \delta_1 + (P_2 - P_1) \times \delta_2$$

$$\delta_1 = \frac{\Delta t_1}{T}, \delta_2 = \frac{\Delta t_2}{T}$$

Where P_X are the different output power conditions, Δt_X are the durations of each peak power condition and T is the period of one cycle of the pulsed load condition.

The design procedure requires both peak and continuous (average) powers to be specified. If there is no peak power requirement for the design, the same value should be used for both continuous and peak power.

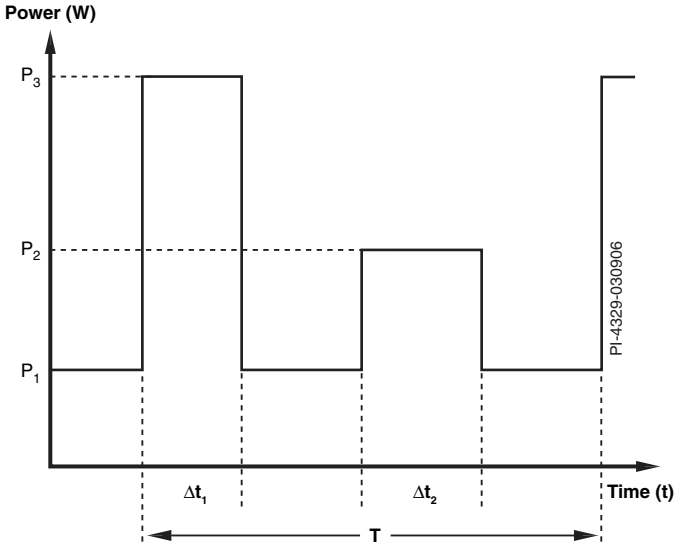


Figure 2. Continuous (average) Output Power Calculation Example.

The peak power is used to select the TOPSwitch-JX device and design the transformer for power delivery at minimum input line voltage while continuous (or average power if the peak load is periodic) is used for thermal design and may affect the size of the transformer and the heatsink.

Step 1. Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, $P_{O(AVE)}$, $P_{O(PEAK)}$, η, Z, V_B, t_C, C_{IN}

Determine the input voltage range from Table 2.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 2. Standard Worldwide Input Line Voltage Ranges.

Line Frequency, f_L

50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimums. For most applications this gives adequate overall design margin. For absolute worst case or based on the product specification, reduce these numbers by 6% (47 Hz or 56 Hz). For half-wave rectification, use f_L/2. For DC input, enter the voltage directly into Cells B67 and B68.

ENTER APPLICATION VARIABLES					Design title
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.00			Volts	Output Voltage (main)
PO_AVG	35.00			Watts	Average Output Power
PO_PEAK			35.00	Watts	Peak Output Power
Heatsink Type	**External**		External		Heatsink Type
Enclosure	**Adapter**				Open Frame enclosure assume sufficienct airflow while adapter means a sealed enclosure.
n	0.80			%/100	Efficiency Estimate
Z	0.50				Loss Allocation Factor
VB	12			Volts	Bias Voltage - Verify that VB is > 8 V at no load and VMAX
tC	3.00			ms	Bridge Rectifier Conduction Time Estimate
CIN	68.0		68	uFarads	Input Filter Capacitor

Figure 3. Application Variable Section of TOPSwitch-JX *Design Spreadsheet.*

DC INPUT VOLTAGE PARAMETERS					
VMIN			74	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage

Figure 4. DC Input Voltage Parameters Showing Grey Override Cells for DC Input Designs.

Nominal Output Voltage, V_O (V)
Enter the nominal output voltage of the main output during the continuous load condition. Generally the main output is the output from which feedback is derived.

Continuous / Average Output Power $P_{O(AVE)}$ (W)
Enter the average output power of the power supply. If the power supply is a multiple output power supply, enter the sum total power of all the outputs.

Peak Output Power $P_{O(PEAK)}$ (W)
Enter the peak output power under peak load conditions. If the design does not have a peak load condition, then leave this entry blank and a value equal to $P_{O(AVE)}$ is assumed. $P_{O(PEAK)}$ is used to calculate the primary inductance value.

In multiple output designs, the output power of the main output (typically the output from which feedback is taken) should be increased such that the peak power (or maximum continuous output power as applicable) matches the sum of the output power from all the outputs in the design. The individual output voltages and currents should then be entered at the bottom of the spreadsheet (cells [B122 to B168]).

Select Heatsink Type and Enclosure
The enclosure determines the maximum power capability of the TOPSwitch-JX device. If the power supply is going to be housed in a sealed plastic case (much like an laptop power supply) then select the adapter enclosure. If on the other hand the power supply has better air flow, select the open frame enclosure.

Depending on the package selected an appropriate heatsink type can be selected. The E package always needs an external heatsink but a V package may be used either with or without an external heatsink. When used without a heatsink the copper area on the PCB provides the only heatsinking. However due to the increased thermal resistance of the PCB, as compared to an external heatsink, the maximum power capability in this configuration will be reduced.

Power Supply Efficiency, η
Enter the estimated efficiency of the complete power supply measured at the output terminals under peak load conditions and worst-case line (generally lowest input voltage). Start with a value of 80% for VAC_{MIN} of 85 VAC and 85% for 195 VAC. These are typical for a design where the majority of the output power is drawn from an output voltage of 12 V and no output current sensing is present on the secondary. For a 5 V output starting values of 75% for VAC_{MIN} of 85 VAC and 80% for 195 VAC are recommended. Once a prototype has been constructed, then measured efficiency can be entered and a further transformer iteration performed, as appropriate.

Power Supply Loss Allocation Factor, Z
This factor represents the proportion of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency number to determine the actual power that must be delivered by the power stage. For example, losses in the input stage (EMI filter, rectification, etc) are not processed by the power stage (transferred through the transformer) and therefore, although they reduce efficiency, the transformer design is not affected by their effect on efficiency.

$$Z = \frac{\text{Secondary Side Losses}}{\text{Total Losses}}$$

Examples of primary side losses are losses incurred in the input rectifier and EMI filter, MOSFET conduction losses and primary side winding losses. Examples of secondary side losses include the losses in secondary diode, secondary windings and core losses, losses associated with the primary side clamp circuit and the bias winding. For designs that do not have a peak power requirement, a value of 0.5 is recommended. For designs with a peak power requirement, enter 0.65. This difference accounts for increased input stage losses under peak power loading

Bias Winding Output Voltage (V_B)
Enter the voltage at the output of the bias winding output. A starting value of 15 V is recommended. The voltage may be set to different values, for example, when the bias winding output is also used as a primary side (non-isolated) auxiliary output. Higher voltages increase no-load input power while values below 8 V are not recommended as at light load there may be insufficient voltage to correctly bias the optocoupler, causing loss of output regulation. A 10 µF, 50 V electrolytic capacitor is the recommended minimum value for the bias winding output filter.

Bridge Diode Conduction Time, t_C (ms)
Enter a bridge diode conduction time of 3.00 ms if there is no better data available.

Total Input Capacitance, C_{IN} (µF)
Table 3 suggests suitable multiplication factors to be used for calculating input capacitance for different AC input voltage ranges.

AC Input Voltage (VAC)	Total Input Capacitance per Watt Output Power (µF/W) Full Wave Rectification
100/115	2 – 3
230	1
85-265	2 – 3

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, V_{MIN} >70 V.

Step 2 – Enter TOPSwitch-JX Variables: Device, Current Limit, V_{OR}, V_{DS}, V_D, Select the Correct TOPSwitch-JX Device

First, refer to the TOPSwitch-JX power table and select a device based on the peak output power design. Then compare the continuous power to adapter column numbers in the power table, if the power supply is of fully enclosed type, or compare to the open-frame column if the power supply is an open-frame design. If the continuous power exceeds the value given in the power table (Table 1), then the next largest device should be selected. Similarly, if the continuous power is close to the adapter power levels given in the power table, then it may be necessary to switch to a larger device based on the measured thermal performance of the prototype.

External Current Limit Reduction Factor, KI

The factor KI sets the value of the current limit threshold. This allows the current limit level to be adjusted slightly above the minimum peak current (I_P) required for power delivery. This optimizes the transformer design by limiting the peak flux density (BP) during overload and start-up.

For higher efficiency and improved thermal performance, KI also allows the selection of a larger TOPSwitch-JX device to be used than required for power delivery by reducing KI, such that the current limit of the larger device is equal to the original smaller part selected.

High Line Operating Mode

This parameter confirms the mode of operation of the TOPSwitch-JX at high line. It is desirable to operate in full-frequency mode at high line as the switching frequency jitter feature will be enabled. (See TOPSwitch-JX data sheet for an explanation of operating modes). This provides improved EMI performance.

Reflected Output Voltage, V_{OR} (V)

This parameter is the secondary winding voltage during diode conduction, reflected back to the primary through the turns ratio of the transformer. The default value is 135 V; however the acceptable range for V_{OR} is between 80 V and 135 V, provided that no warnings in the spreadsheet are triggered. For design optimization purposes, the following trade-offs should be considered:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the input capacitance value and maximizes power delivery from a given TOPSwitch-JX device.
2. Higher V_{OR} reduces the voltage stress on the output diodes, which in some cases may allow the use of a lower forward drop Schottky diode for higher efficiency.
3. Higher V_{OR} can increase leakage inductance and increase clamp losses that reduces efficiency of the power supply and degrade cross regulation in multiple output designs.
4. Higher V_{OR} increases peak and RMS current on the secondary side, which may increase secondary side copper and diode losses.

Optimal selection of the V_{OR} value depends on the specific application and is based on a compromise between the factors mentioned above.

For lower voltage outputs (approximately 5 V or multiple output designs) a lower V_{OR} of approximately 100 V - 110 V is usually better suited. For higher voltage outputs (12 V and above) a higher V_{OR} of approximately 120 and 135 V is better suited.

Values below 80 V are not usually recommended. Low V_{OR} may cause excessive triggering of the MOSFET self-protection feature during start-up, especially in designs where all outputs are >5 V (see Table 4 for a summary).

TOPSwitch-JX ON-State DRAIN to SOURCE Voltage, V_{DS} (V)

This parameter is the average ON state voltage developed across the DRAIN and SOURCE pins of TOPSwitch-JX. By default, if the grey override cell is left empty, a value of 10 V is assumed. Use the default value if no better data is available.

Output Diode Forward Voltage Drop, V_D (V)

Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 0.7 V for a PN diode if no better data is available. By default, a value of 0.5 V is assumed.

Bias Winding Diode Forward Voltage Drop, V_{DB} (V)

Enter the average forward voltage drop of the bias winding output diode. Use 0.7 V for a PN diode.

Ripple to Peak Current Ratio, K_P

Figure 6 shows $K_P < 1$, indicating continuous conduction mode, K_P is the ratio of ripple to peak primary current.

ENTER TOPSWITCH-JX VARIABLES					
TOPSwitch-JX	**TOP266E**			Universal / Peak	115 Doubled/230V
Chosen Device		*TOP266E*	Power Out	40 W / 86 W	60W
KI	0.53				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN_EXT			1.257	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX_EXT			1.446	Amps	Use 1% resistor in setting external ILIMIT
Frequency (F)=132kHz, (H)=66kHz	**F**		F		Select 'H' for Half frequency - 66kHz, or 'F' for Full frequency - 132kHz
fS			132000	Hertz	TOPSwitch-JX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			119000	Hertz	TOPSwitch-JX Minimum Switching Frequency
fSmax			145000	Hertz	TOPSwitch-JX Maximum Switching Frequency
High Line Operating Mode			FF		Full Frequency, Jitter enabled
VOR	135.00			Volts	Reflected Output Voltage
VDS			10	Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.50				Ripple to Peak Current Ratio (0.3 < KRP < 1.0 : 1.0< KDP<6.0)

Figure 5. TOPSwitch-JX Section of Design Spreadsheet.

Performance Goal	V_{OR} Value Suggestion	Comment
Maximum output power / smallest TOPSwitch-JX Device	135 V	Maximizes power from given device
Highest Efficiency	100 V - 120 V	Gives lowest overall losses between, conduction, output diode and leakage inductance
Multiple Output Design	90 V - 110 V	Improves cross regulation by reducing transformer leakage inductance and peak secondary currents

Table 4. Suggested Values for V_{OR}.

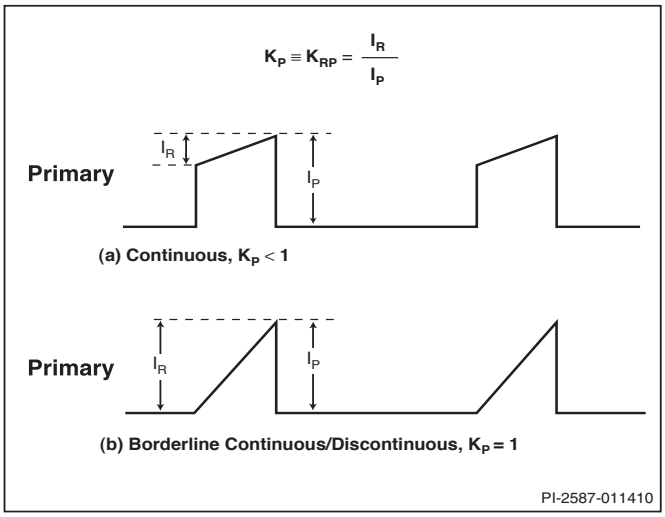


Figure 6. Continuous Mode Current Waveform, $K_P \leq 1$.

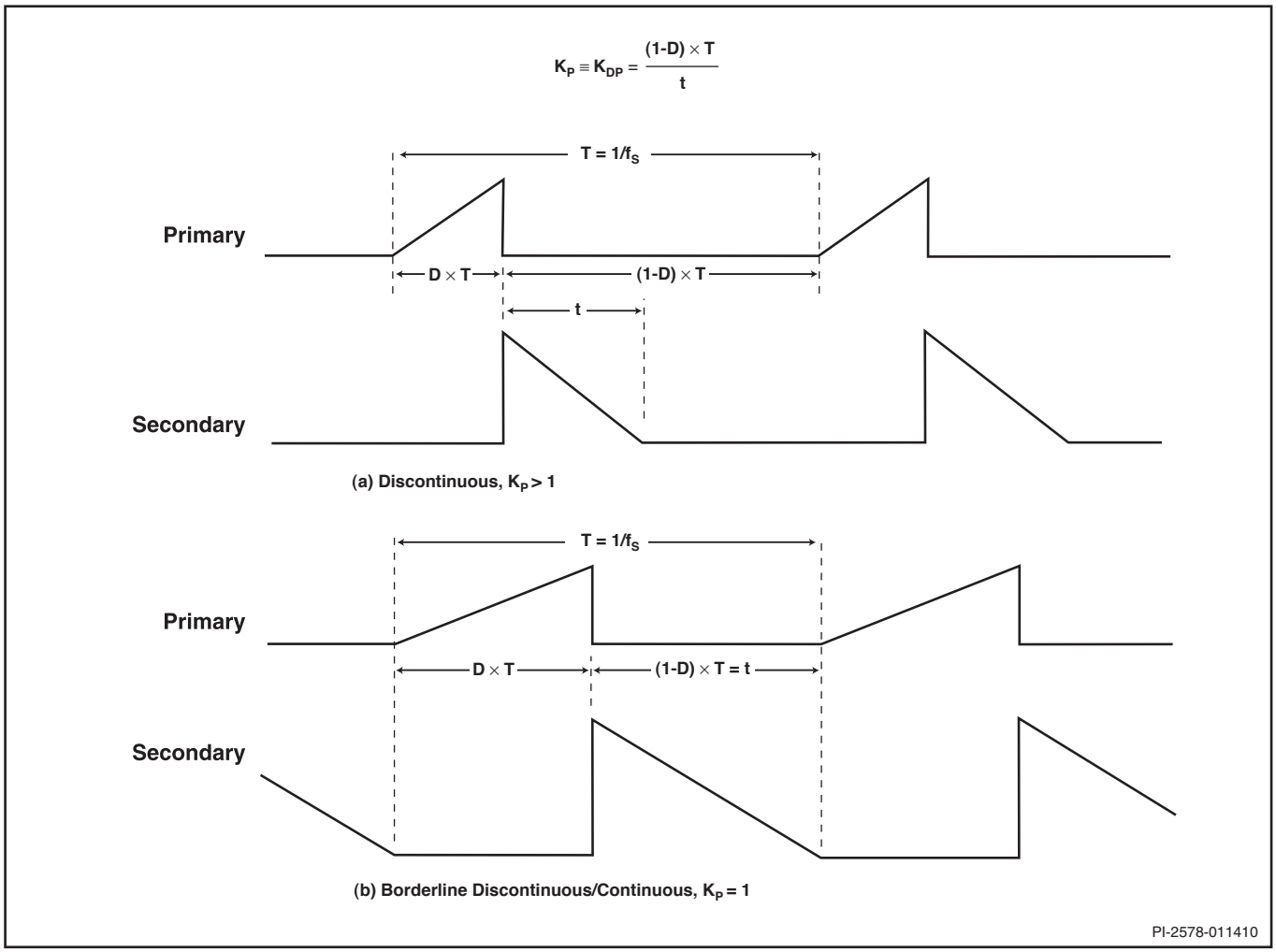


Figure 7. Discontinuous Mode Current Waveform, $K_P \geq 1$.

PROTECTION FEATURES					
LINE SENSING					V pin functionality
VUV_STARTUP			95	Volts	Minimum DC Bus Voltage at which the power supply will start-up
VOV_SHUTDOWN			445	Volts	Typical DC Bus Voltage at which power supply will shut-down (Max)
RLS			4.0	M-ohms	Use two standard, 2 M-Ohm, 5% resistors in series for line sense functionality.
OUTPUT OVERVOLTAGE					
VZ			22	Volts	Zener Diode rated voltage for Output Overvoltage shutdown protection
RZ			5.1	k-ohms	Output OVP resistor. For latching shutdown use 20 ohm resistor instead
OVERLOAD POWER LIMITING					X pin functionality
Overload Current Ratio at VMAX			1.2		Enter the desired margin to current limit at VMAX. A value of 1.2 indicates that the current limit should be 20% higher than peak primary current at VMAX
Overload Current Ratio at VMIN			1.08		Margin to current limit at low line.
ILIMIT_EXT_VMIN			1.16	A	Peak primary Current at VMIN
ILIMIT_EXT_VMAX			1.04	A	Peak Primary Current at VMAX
RIL			11.74	k-ohms	Current limit/Power Limiting resistor.
RPL			N/A	M-ohms	Resistor not required. Use RIL resistor only

CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.68		Maximum Duty Cycle (calculated at PO_PEAK)
IAVG			0.59	Amps	Average Primary Current (calculated at average output power)
IP			1.16	Amps	Peak Primary Current (calculated at Peak output power)
IR			0.58	Amps	Primary Ripple Current (calculated at average output power)
IRMS			0.73	Amps	Primary RMS Current (calculated at average output power)

Figure 8. Circuit Protection Component Section of Design Spreadsheet.

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$

Figure 7 shows $K_P \geq 1$, indicating discontinuous conduction mode, K_P is the ratio of primary MOSFET off time to the secondary diode conduction time.

$$K_P \equiv K_{DP} = \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

The value of K_P should be in the range of $0.3 < K_P < 6$, and guidance is given in the comments cell if the value is outside this range.

A K_P value of <1 will result in higher efficiency by lowering the primary RMS current. A K_P between 0.6 and 0.8 is recommended for 230 VAC (compared to between 0.4 and 0.6 for 100/115 VAC and universal input) to accommodate for a significantly taller and wider leading edge current spike caused by the discharge of the drain node capacitance at higher voltage levels.

The spreadsheet will calculate the values of peak primary current, the RMS ripple current, average primary current and the maximum duty cycle for the design.

Step 3 – Choose Protection Features, Line Under / Overvoltage, Output Overvoltage and Overload Power Limiting - Optional

The optional line undervoltage lockout feature of TOPSwitch-JX, defines the start-up voltage of the supply and prevents the power supply output from glitching when the input voltage is below the normal operating range. Connecting a resistor from the input capacitor to the V pin enables this feature. Enter the desired DC voltage across the input capacitor, at which the power supply should operate in the cell adjacent to $V_{UV(START-UP)}$. The spread-sheet calculates the closest standard 5% resistor value R_{LS}.

The value of R_{LS} also defines the line OV threshold. The voltage at which the power supply will stop operating due to an input overvoltage condition is displayed in the cell adjacent to $V_{OV(SHUTDOWN)}$.

Output Overvoltage Shutdown - Optional

The output voltage of the bias winding can be used to provide primary sensed output overvoltage. This is an inexpensive way of protecting the power supply should a component in the feedback circuit fail.

This feature can be enabled by connecting a series combination of a resistor and Zener diode from the bias winding output to the V pin (as shown in Figure 1). The spreadsheet estimates a value of the Zener diode required to initiate shutdown in case of loss of feedback but without false triggering during transient conditions such as during dynamic load changes.

During a fault, the bias winding voltage rises causing the Zener diode to conduct and current to flow into the V pin. If this current exceeds 112 µA (I_{OV}), switching is immediately disabled. Switching can resume anytime if this current falls below 108 µA within 100 µs. After 100 µs however, the supply enters auto-restart mode. This prevents further increase in output voltage but does not latch off the power supply. Switching is enabled again when the current reduces by greater than the 4 µA, V pin hysteresis requirement. If the current through the Zener and into the V pin exceeds 336 µA, the latching shutdown feature of TOPSwitch-JX is triggered, and the power supply latches off. To reset the latched condition, either the input AC supply has to be removed, long enough for the CONTROL pin capacitor to discharge below $V_{C(RESET)}$ (~3 V) or when the X pin current falls below 27 µA.

In a typical circuit, a high series resistance R_{OVP} in the order of 5.1 kΩ will result in a non-latching shutdown. A low resistance in the range of 4.7 Ω to 22 Ω will result in a latching shutdown.

To avoid noise coupling it is recommended that the resistor should be connected to the V pin and the Zener diode cathode should be connected to the bias winding output.

With the OVP components fitted there is an additional ~2s delay from applying AC (above the line UV threshold) to the supply operating. This delay is caused by the time for the V pin to charge the bias winding capacitor via R_{OVP} and V_{ROVP}. This can be prevented by adding a small signal (e.g. BAV21/1N4148) diode in series with V_{ROVP} (see Figure 21).

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**Auto**		EI28		Core Type
Core		*EI28*		*P/N:*	PC40EI28-Z
Bobbin		*EI28_BOBBIN*		*P/N:*	BE-28-1110CPL
AE			0.86	cm^2	Core Effective Cross Sectional Area
LE			4.82	cm	Core Effective Path Length
AL			4300	nH/T^2	Ungapped Core Effective Inductance
BW			9.6	mm	Bobbin Physical Winding Width
M	0.00			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00				Number of Primary Layers
NS			3		Number of Secondary Turns

Figure 9. Transformer Core and Construction Variables Section of Spreadsheet.

Output Power Limiting vs. Input Voltage (Optional)

The X pin on the TOPSwitch-JX can be used to program a current limit value lower than the maximum internal current limit for the part selected. A resistor connected from the X pin to the SOURCE pin (R_{IL} in Figure 1) allows selection of a fixed externally programmed current limit. See data sheet for current limit resistor selection curves.

The addition of a second resistor connected from the X pin to the DC-Bus (R_{PL}), as shown in Figure 12, allows reduction of the programmed current limit as a function of the line voltage. This is desirable as typical flyback power supplies that operate in continuous conduction mode at low line (K_P <1) will have a higher overload power capability at high line by 200-300%. In certain applications this may require over design of the output diode, transformer and output capacitors to handle the increased dissipation during an overload fault.

The PIXIs spreadsheet calculates the values of the two resistors required for power limiting vs. line based on the choice of the TOPSwitch-JX part and the value of K_P selected. At V_{MIN} the target current limit value is equal to $I_{LIMIT(MIN\_EXT)}$. At high line the target current limit value is calculated based on the value required for specified $P_{O(PEAK)}$ multiplied by the margin factor, overload current limit ratio at V_{MAX}. The recommended value of 120% ensures that the MOSFET protection mode is not triggered during start-up, especially with high output voltage designs. Lower values are acceptable, but start-up into maximum (peak) load at high input line voltage must be verified.

Resistor values are calculated using the worst case current limit reduction curves provided in the TOPSwitch-JX data sheet.

Step 4 – Choose Core and Bobbin Based on Output Power and Enter A_E, L_E, A_L, BW, M, L, N_S

Core effective cross-sectional area, A_E: (cm^2)
Core effective path length, L_E: (cm).
Core ungapped effective inductance, A_L: ($nH/turn^2$).
Bobbin width, BW: (mm)
Tape margin width equal to half the total margin, M (mm)
Primary Layers, L
Secondary Turns, N_S

Core Type

If the core type cell is left empty, the spreadsheet will default to the smallest commonly available core suitable for the continuous (average) output power specified. The entire list of cores available can be selected from the drop down list in the tool bar of the PIXIs design software.

The grey override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list, or the specific core or bobbin information differs from that referenced by the spreadsheet.

Output Power	66 kHz		132 kHz	
	Triple Insulated Wire	Margin Wound	Triple Insulated Wire	Margin Wound
0 - 10 W	EF12.6 EE13 EF16 EE16 EE19 EI22 EI22/19/6	EI22 EE19 EI22/19/6 EEL16 EF20 EI25 EEL19	EF12.6 EE13 EF16 EE16	EI22 EE19 EI22/19/6 EEL16
10 W - 20 W	EF20	EI28 EEL22 EF25	EE19 EI22 EI22/19/6 EF20	EF20 EI25 EEL19
20 W - 30 W	EF25	EI30 EPC30 EEL25		EI28
30 W - 50 W	EI28 EI30 E30/15/7 EER28	E30/15/7 EER28 ETD29 EI35 EI33/29/ 13-Z EER28L	EF25	EEL22
50 W - 70 W	ETD29 EI35 EF32	EF32 ETD34	EI28	EEL25 E30/15/7 EER28
70 W - 100 W	ETD34 E36/18/11 EI40	EI40 E36/18/11 EER35	EI30 E30/15/7 EER28 ETD29	ETD29 EI35 EI33/29/ 13-Z EER28L EF32
100 W - 150 W	ETD39 EER40	ETD39 EER40 E42/21/15	EI35 EF32 ETD34	ETD34 EI40 E36/18/11 EER35
>150 W	E42/21/15 E42/21/20 E55/28/21	E42/21/20 E55/28/21	E36/18/11 EI40 ETD39 EER40 E42/21/15 E42/21/20 E55/28/21	ETD39 EER40 E42/21/15 E42/21/20 E55/28/21

Table 5. Transformer Core Table.

Table 5 provides a list of commonly available cores and power levels at which these cores can be used for typical designs.

Safety Margin, M (mm)
For designs that require safety isolation between primary and secondary but do not use triple-insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. For universal input designs, a total windings margin of 6.2 mm would be required, and a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical. However, if a total margin of 6.2 mm were required, then 3.1 mm would still be entered even if the physical margin were only on one side of the bobbin.

For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet the required safety creepage distances. Typically, many bobbins exist for any core size and, each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required.

As the margin reduces the available area for the windings, the margin format described above may not be suitable for small core sizes. If after entering the margin, more than 3 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design approach using triple-insulated wire.

Primary Layers, L
Primary layers should be in the range of $1 < L < 3$, and in general it should be the lowest number that meets the primary current density limit (CMA). Values of 100 Cmils/Amp for designs <5 W scaling linearly to 500 Cmils/Amp at 200 W are typical in designs without forced air cooling. Designs with more than 3 layers are possible, but the increased leakage inductance and issues associated with the physical fit of the windings should be considered. A split primary construction may be helpful for designs where leakage inductance clamp dissipation is too high. Here half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement.

Secondary Turns, NS
If the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density B_M is kept below the recommended maximum of 3000 Gauss (300 mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired (see the explanation of B_M limits).

Step 5 – Iterate Transformer Design / Generate Prototype

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to wind a prototype transformer or sent to a vendor for samples. (See note on transformer prototyping services in Quick Start section.)

The key transformer electrical parameters are:

Primary Inductance, L_P (µH)
This is the target nominal primary inductance of the transformer.

Primary Inductance Tolerance, $LP_{(TOLERANCE)}$(%)
This is the assumed primary inductance tolerance. A value of 10% is used by default; however if specific information is known from the transformer vendor, then this may be entered in the grey override cell.

Number of Primary Turns, N_P
For low leakage inductance applications, a split primary construction may be used, and is recommended for designs above 20 W.

Gapped Core Effective Inductance, A_{LG}: (nH/T^2)
Used by the transformer vendor to specify the core center leg air gap.

Maximum Operating Flux Density, B_M (Gauss)
A maximum value of 3000 Gauss during normal operation is recommended. This limits transformer core loss and audible noise generated at light load levels. This limit also prevents core saturation during start-up or output short circuit. Under these conditions the output voltage is low and little reset of the transformer core occurs during the MOSFET off time. This typically allows the transformer flux density to increase during the next and subsequent cycles (staircasing) until the core saturates. A value of 3000 Gauss at the peak current limit of the selected device, together with the built in protection features of TOPSwitch-JX, provides sufficient margin to prevent core saturation under start-up or output short circuit conditions.

The multi-cycle modulation (MCM) mode of operation used in TOPSwitch-JX can generate audio frequency components in the transformer, especially if a long core is used. This audible noise generation is minimized when a value of 3000 Gauss is used for B_M. This results in an operating flux density of 750 Gauss in MCM mode. Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. A careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Ceramic capacitors that use dielectrics, such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, a solution may be to replace them with capacitors having a different dielectric, for example a polyester film type.

Peak Flux Density, B_P (Gauss)
A maximum value of 4200 Gauss is recommended to limit the maximum flux density under start-up and output short circuit conditions. This calculation assumes worst-case current limit and inductance values. In high ambient temperature applications,

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1435	uHenries	Primary Inductance
LP Tolerance			10		Tolerance of Primary Inductance
NP			74		Primary Winding Number of Turns
NB			7		Bias Winding Number of Turns
ALG			265	nH/T^2	Gapped Core Effective Inductance
BM			2637	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP			3603	Gauss	Peak Flux Density (BP<4200) at ILIMITMAX and LP_MAX. Note: Recommended values for adapters and external power supplies <=3600 Gauss
BAC			659	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1918		Relative Permeability of Ungapped Core
LG			0.38	mm	Gap Length (Lg > 0.1 mm)
BWE			28.8	mm	Effective Bobbin Width
OD			0.39	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.33	mm	Bare conductor diameter
AWG			28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			161	Cmils	Bare conductor effective area in circular mils
CMA			220	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Primary Current Density (J)			9.11	Amps/mm^2	Primary Winding Current density (3.8 < J < 9.75)

Figure 10. Transformer Primary Design Parameters Section of Spreadsheet.

TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			5	Volts	Output Voltage
IO1_AVG			7.00	Amps	Average DC Output Current
PO1_AVG			35.00	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			3.00		Output Winding Number of Turns
ISRMS1			12.363	Amps	Output Winding RMS Current
IRIPPLE1			10.19	Amps	Output Capacitor RMS Ripple Current
PIVS1			20	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			2473	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			16	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			1.29	mm	Minimum Bare Conductor Diameter
ODS1			3.20	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2_AVG				Amps	Average DC Output Current
PO2_AVG			0.00	Watts	Average Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.38		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.38		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total Continuous Output Power			35	Watts	Total Continuous Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Figure 11. Transformer Secondary Design Parameters Section of Spreadsheet – Multiple Outputs.

such as sealed adapters or with lower grade ferrite core material, this value may need to be reduced to 3600 Gauss due to the higher operating ambient temperature. It is important to verify that core saturation does not occur at maximum ambient temperature under overload conditions just prior to loss of regulation.

Maximum Primary Wire Diameter, OD (mm)

By default, if the override cell is empty, double insulated wire is assumed and the standard wire diameter is chosen. The grey override cells can be used to enter the wire diameter directly by the user.

The other factors automatically calculated by the spreadsheet include:

Estimated Total Insulation Thickness, INS (mm)
Primary wire size, DIA: (mm)
Primary wire gauge, AWG
Number of primary layers, L
Estimated core center leg gap length: L_G: (mm)
Number of secondary turns, N_S
Secondary wire size, DIAs: (mm)
Secondary wire gauge, AWG

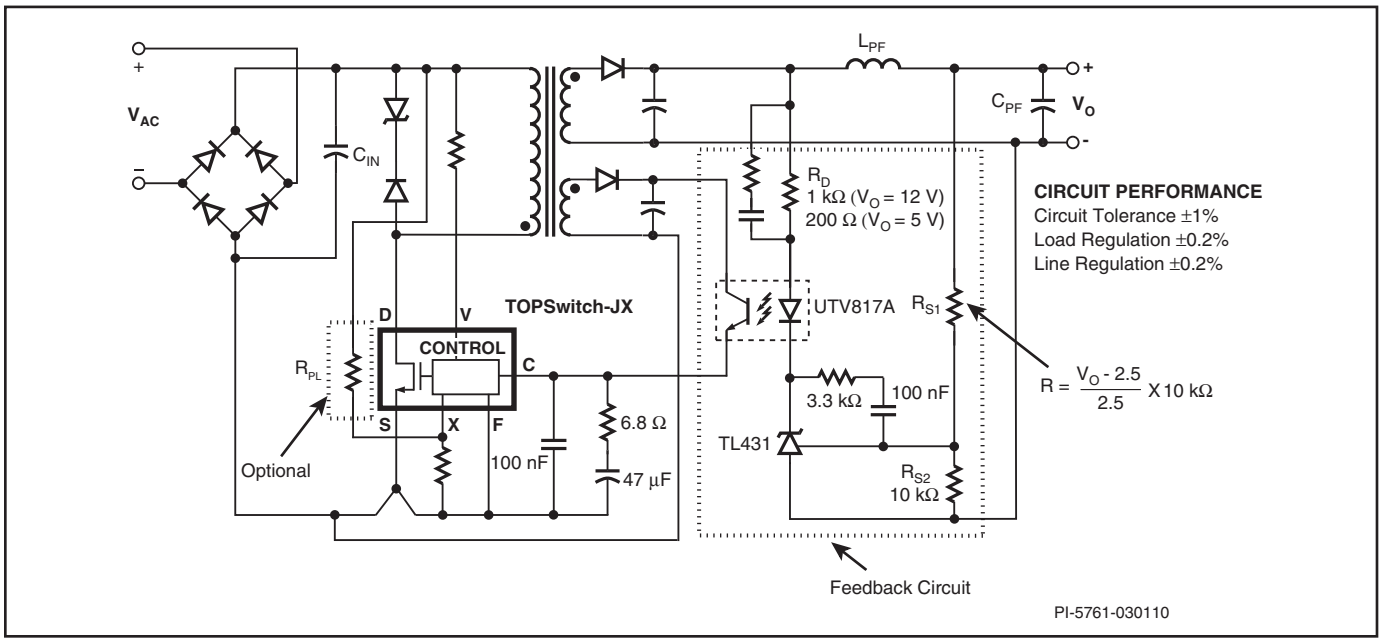


Figure 12. Typical TOPSwitch-JX Flyback Power Supply Using Optocoupler-TL431 Feedback Circuit.

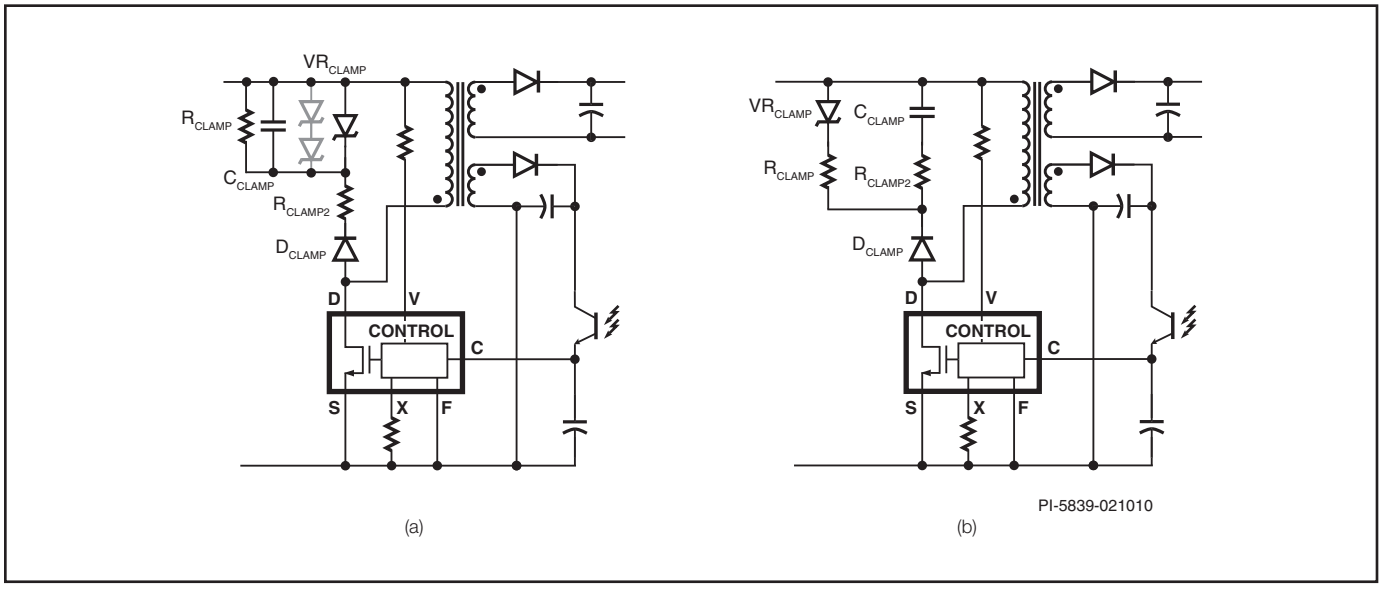


Figure 13. Recommended Clamp Circuits with TOPSwitch-JX Applications.

In multiple output design NSx, CMSx, AWGSx (where x is the output number) should also be used.

Step 6 – Selection of TOPSwitch-JX External Components

CONTROL Pin – External Components

The schematic in Figure 12 shows the external components required for a typical TOPSwitch-JX power supply design. It is strongly recommended that a 100 nF capacitor be directly connected between the CONTROL pin and the SOURCE pin of the TOPSwitch-JX. This capacitor should be located adjacent to the TOPSwitch-JX with short traces. In designs using surface mount components, this capacitor should be located directly at the pins of the TOPSwitch-JX.

In addition to the 100 nF capacitor connected to the CONTROL pin, a series combination of a 6.8 Ω resistor and a 47 µF electrolytic capacitor is required to be connected between the CONTROL pin and the SOURCE terminal of the TOPSwitch-JX. The 47 µF capacitor acts as an energy reservoir and provides power to the TOPSwitch-JX internal circuitry during start-up and also provides the timing for auto-restart. Furthermore, this capacitor together with the dynamic impedance of the CONTROL pin forms a pole at approximately 160 Hz. A small value resistor (6.8 Ω) is generally added in series with this capacitor. This external resistor, along with the ESR of the CONTROL pin capacitor (typically about 2 Ω), provides a stable series resistance and forms a zero at approximately 400 Hz. Although larger values of the external resistor may help improve the phase response, values above 22 Ω should be avoided.

Step 7 – Selection of Line - Undervoltage / Overvoltage Components

The line undervoltage detection feature prevents the power supply from starting until the input voltage is above a defined level. During power-up or when the switching of the power MOSFET is disabled during auto-restart, the current into the V pin must exceed 25 µA to initiate switching (I_{UV} in data sheet). As a resistor from the DC rail to the V pin is used to sense the input voltage, the supply voltage that causes the current into the V pin to exceed 25 µA defines the undervoltage threshold. The same resistor also defines the line overvoltage threshold. When the current into the V pin exceeds I_{OV} (112 µA typical) the device stops switching, increasing the voltage withstand of the TOPSwitch-JX to its 725 V BV_{DSS} rating.

With a typical value of 4 MΩ connected from the DC rail to the V pin line UV is programmed to 100 VDC and OV to 450 VDC.

The sense resistor should be rated above 400 V, generally requiring either a single 0.5 W or two 0.25 W devices connected in series. A typical value of 4 MΩ is suggested for use as line sense resistor for universal input applications. Additional guidance is provided by the design spreadsheet.

If the undervoltage (UV) or the overvoltage (OV) functions are to be used selectively, a number of circuits are provided in the TOPSwitch-JX family data sheet to ease the selection of external components. If the V pin function is not used, the V pin should be connected to the SOURCE pin. The V pin should not be left unconnected.

Step 8 – Selection of Primary Clamp Components

It is recommended that either a Zener clamp or an RCD combined with a Zener clamp be used in TOPSwitch-JX designs. This is to ensure that the peak drain voltage is limited to below the BV_{DSS} of the internal MOSFET while still maximizing efficiency and minimizing no-load consumption.

A standard RCD clamp designed to limit the peak drain voltage under peak load conditions represents a significant load as the output power is reduced, resulting in lower light-load efficiency and higher no-load consumption.

Rec. Diode	V_R(V)	I_D(A)	Package	Manufacturer
Schottky				
1N5819	40	1	Axial	Vishay
SB140	40	1	Axial	Vishay
SB160	60	1	Axial	Vishay
MBR160	60	1	Axial	IR
11DQ06	60	1.1	Axial	IR
1N5822	40	3	Axial	Vishay
SB340	40	3	Axial	Vishay
MBR340	40	3	Axial	IR
SB360	60	3	Axial	Vishay
MBR360	60	3	Axial	IR
SB540	40	5	Axial	Vishay
SB560	60	5	Axial	Vishay
MBR745	45	7.5	TO-220	Vishay / IR
MBR760	60	7.5	TO-220	Vishay
MBR1045	45	10	TO-220	Vishay / IR
MBR1060	60	10	TO-220	Vishay
MBR10100	100	10	TO-220	Vishay
MBR1645	45	16	TO-220	Vishay / IR
MBR1660	60	16	TO-220	Vishay
MBR2045CT	45	20(2×10)	TO-220	Vishay / IR
MBR2060CT	60	20(2×10)	TO-220	Vishay
MBR20100	100	20(2×10)	TO-220	Vishay / IR
UFR				
UF4002	100	1	Axial	Vishay
UF4003	200	1	Axial	Vishay
MUR120	200	1	Axial	Vishay
EGP20D	200	2	Axial	Vishay
BYV27-200	200	2	Axial	Vishay / NXP
UF5401	100	3	Axial	Vishay
UF5402	200	3	Axial	Vishay
EGP30D	200	3	Axial	Vishay
BYV28-200	200	3.5	Axial	Vishay / NXP
MUR420	200	4	TO-220	Vishay
BYW29-200	200	8	TO-220	Vishay / NXP
BYV32-200	200	18	TO-220	Vishay / NXP

Table 6. List of Diodes Suitable for use as the Output Rectifier.

Figure 13a shows an example of an RCD + Zener clamp. During normal operation the Zener diode does not conduct, clamping is provided by R_{CLAMP} and C_{CLAMP}. This allows the values to be optimized for full load rather than overload and start-up. This results in lower dissipation and improved light load and no-load input power. During output overload and start-up VR_{CLAMP} provides a defined maximum drain voltage below the BV_{DSS} rating of the MOSFET. In high power designs, multiple Zeners may be required to share dissipation, shown in gray in Figure 13a. A Zener clamp may also be used (R_{CLAMP} and C_{CLAMP} are eliminated) which results in excellent full load and light efficiency plus low no-load input power but higher EMI.

Figure 13b shows an efficient RCDZ clamp circuit. This configuration provides the light load and no-load performance of the Zener clamp as well as the low EMI characteristic of an RCD clamp. The benefit of this circuit is that at light load or no-load C_{CLAMP} does not discharge below the value of VR_{CLAMP}. In a normal RCD clamp at light or no-load the capacitor ripple voltage becomes very large (>V_{OR}) and the clamp the main load giving poor no-load input power and low light load efficiency. The operation is similar to the traditional RCD clamp. After the turn-off event of the switch, capacitor C_{CLAMP} is discharged via R_{CLAMP} and VR_{CLAMP}, resetting the capacitor ready for the next turn-off event. Dissipation is shared between VR_{CLAMP} and R_{CLAMP} in proportion to the voltages across these two components. The recommended value for VR_{CLAMP} is about 10% higher than the V_{OR} of the design. Two Zeners can be placed in series to increase the power capability of the Zeners.

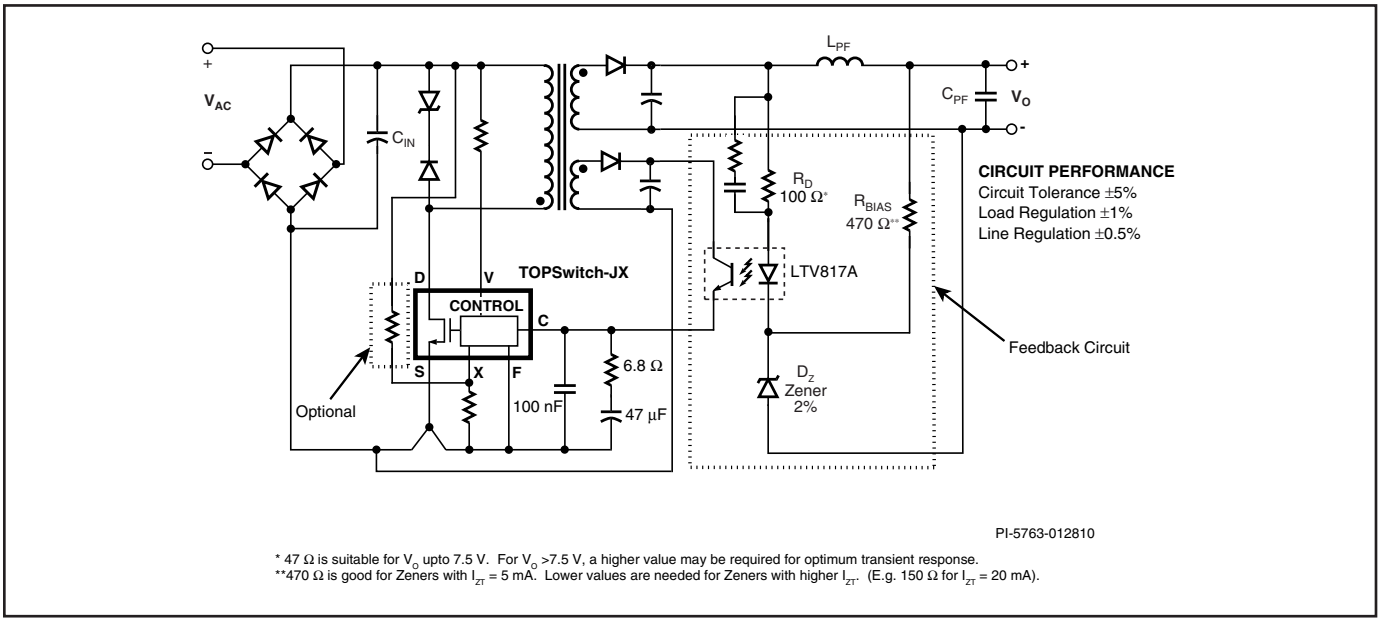


Figure 14. Typical Zener Feedback Circuit.

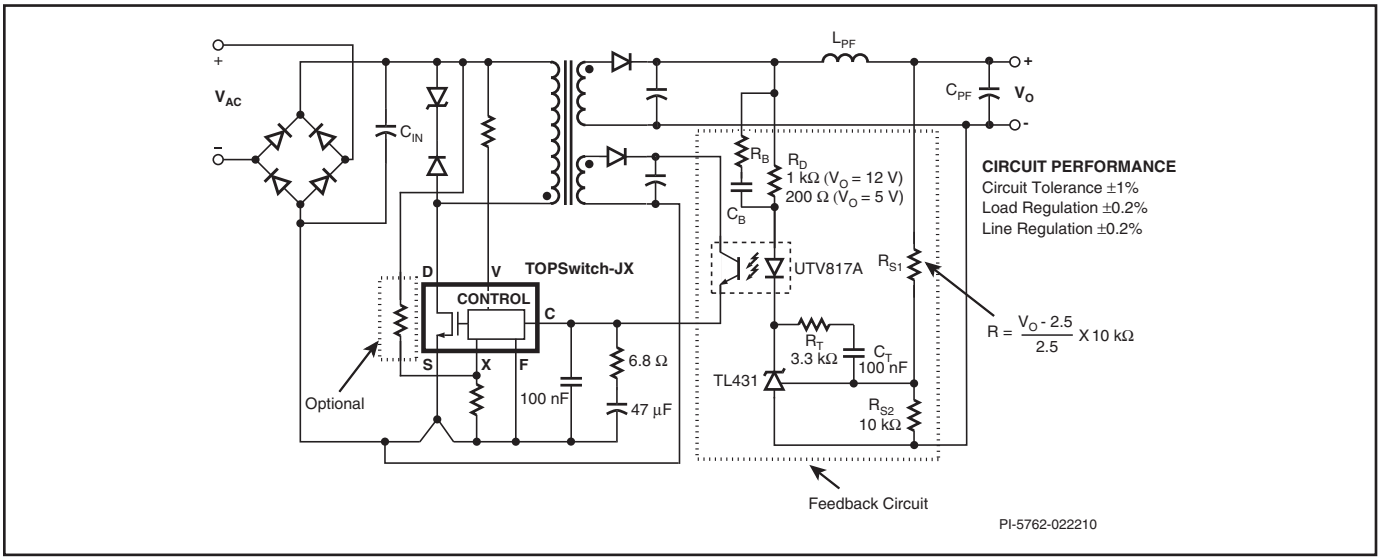


Figure 15. Optocoupler-TL431 Feedback Circuit.

The peak drain voltage should be limited to a maximum of 675 V under these conditions to provide a margin for component variation. The clamp diode (D_{CLAMP}) must be a fast or an ultra-fast recovery type with a reverse recovery time <500 ns. Under no circumstances should a standard recovery rectifier diode be used. The high dissipation that may result during start-up or an output short circuit can cause failure of the diode. Resistor R_{CLAMP1} damps ringing for reduced EMI. Power supplies using different members of the TOPSwitch-JX family will have different peak primary currents and leakage inductances, and therefore different leakage energy. Capacitor C_{CLAMP} and R_{CLAMP} must be optimized for each design. As a general rule, minimize the value of capacitor C_{CLAMP} and maximize the value of resistor R_{CLAMP} while still meeting the recommended 675 V peak drain voltage limit.

Step 9 – Select Output Rectifier Diode

For each output use the values of peak inverse voltage (V_R) and output current (I_O) provided in the design spreadsheet to select the output diodes. Table 6 shows some commonly available types.

$V_R \geq 1.25 \times PIV_S$: where PIV_S is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters (Multiple Outputs).

$I_D \geq 2 \times I_O$: where I_D is the diode rated DC current, and I_O is the average output current. Depending on the temperature rise and the duration of the peak load condition, it may be necessary to increase the diode current rating once a prototype has been built. This also applies to the amount of heatsinking required.

Step 10 – Select Output Capacitor

Ripple Current Rating

The spreadsheet calculates output capacitor ripple current using the average output power. Therefore the actual rating of the capacitor will depend on the peak to average power ratio of the design. In most cases this assumption will be valid as capacitor ripple rating is a thermal limitation, and most peak load durations are shorter than the thermal time constant of the capacitor (<1s). For such designs, select the output capacitor(s) such that the ripple rating is greater than the calculated value of I_{RIPPLE} from the spreadsheet. However, in designs with high peak to continuous (average) power and long duration peak load conditions, the capacitor rating may need to be increased based on the measured capacitor temperature rise under worst-case load and ambient conditions.

In either case, if a suitable individual capacitor cannot be found, then two or more capacitors may be used in parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ratings.

Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This should also be considered to ensure that the capacitor is not oversized.

P/N	CTR(%)	BVCEO	Manufacturer
4 Pin DIP			
PC123Y6	80-160	70 V	Sharp
PC817X1	80-160	70 V	Sharp
PC817X4J	300-600	80 V	Sharp
SFH615A-2	63-125	70 V	Vishay, Isocom
SFH617A-2	63-125	70 V	Vishay, Isocom
SFH618A-2	63-125	55 V	Vishay, Isocom
ISP817A	80-160	35 V	Vishay, Isocom
LTV817A	80-160	35 V	Liteon
LTV816A	80-160	80 V	Liteon
LTV123A	80-160	70 V	Liteon
LTV817D	300-600	35 V	Liteon
K1010A	60-160	60 V	Cosmo
6 Pin DIP			
LTV702FB	63-125	70 V	Liteon
LTV703FB	63-125	70 V	Liteon
LTV713FA	80-160	35 V	Liteon
K2010	60-160	60 V	Cosmo
PC702V2NSZX	63-125	70 V	Sharp
PC703V2NSZX	63-125	70 V	Sharp
PC713V1NSZX	80-160	35 V	Sharp
PC714V1NSZX	80-160	35 V	Sharp
MOC8102	73-117	30 V	Vishay, Isocom
MOC8103	108-173	30 V	Vishay, Isocom
MOC8105	63-133	30 V	Vishay, Isocom
CNY17F-2	63-125	70 V	Vishay, Isocom, Liteon

Table 7. Optocouplers.

ESR Specification

The switching ripple voltage on the output is equal to the peak secondary current multiplied by the ESR of the output capacitor (electrolytic types assumed). It is therefore important to select low ESR capacitor types to reduce the ripple voltage. In general, selecting a capacitor rated for the output ripple, will result in an acceptable value of ESR.

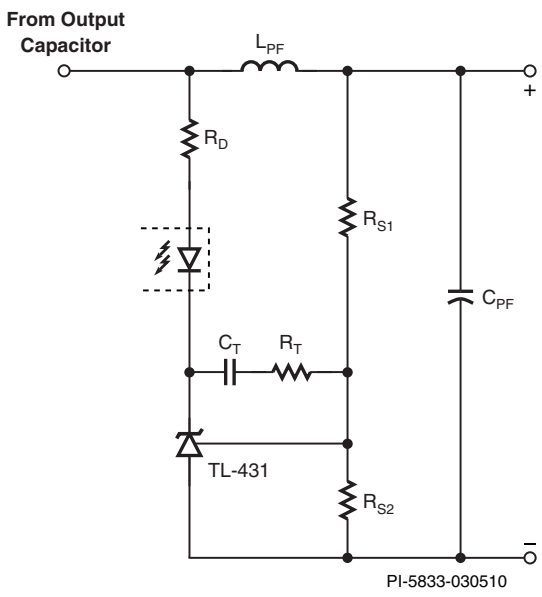
Voltage Rating

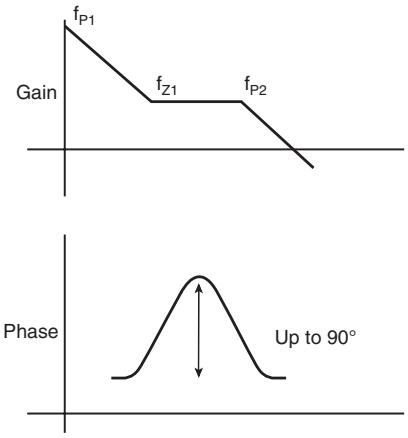
Select a voltage rating such that $V_{RATED} \geq 1.25 \times V_O$.

Step 11 – Select Feedback Circuit Components

The choice of the feedback circuit for a power supply is governed by the desired output regulation. A simple feedback circuit can be configured using a Zener diode in series with the optocoupler diode. Though this method is inexpensive, it relies on the Zener diode to control the output voltage, which limits performance due to the device's wide tolerance and large temperature coefficient as compared to a referenced IC.

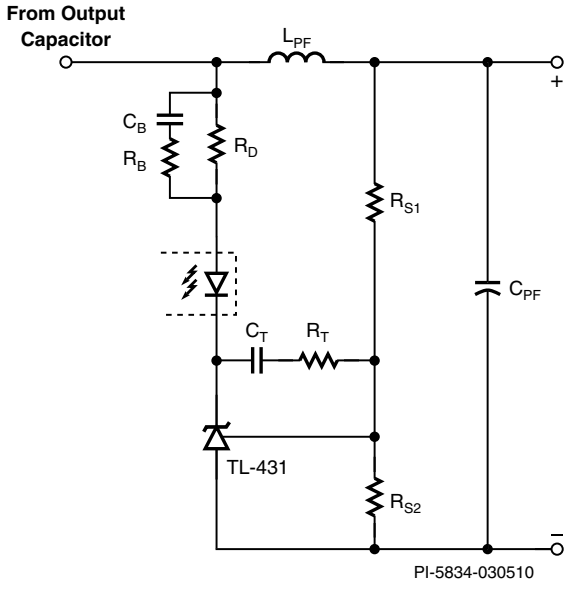
Figure 14 shows a typical implementation of Zener feedback. The drop across the Zener diode D_Z, optocoupler series resistor

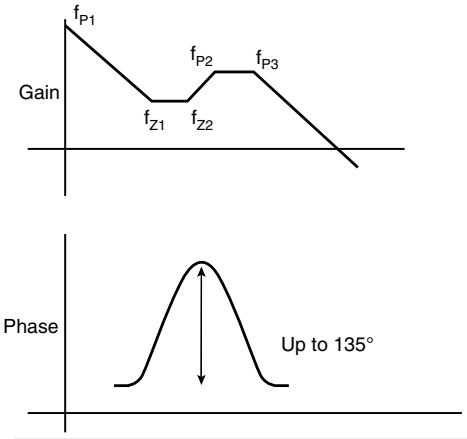




Pole/Zero	Formed by	Approximate Location
f_{P1}	C_T	0 Hz
f_{Z1}	R_T, C_T, R_{S1}	100 Hz
f_{P2}	TOPSwitch	7 kHz

Figure 16. Typical "Type 2" Controller Implementation Using TOPSwitch-JX.





Pole/Zero	Formed by	Approximate Location
f_{P1}	C_T	0 Hz
f_{Z1}	R_T, C_T, R_{S1}	100 Hz
f_{Z2}	R_B, C_B, R_D	f_C
f_{P2}	TOPSwitch	7 kHz
f_{P3}	R_B, C_B, R_D	10 f_C

Figure 17. Modified "Type 2" Controller to Provide Additional Phase Boost Near Crossover.

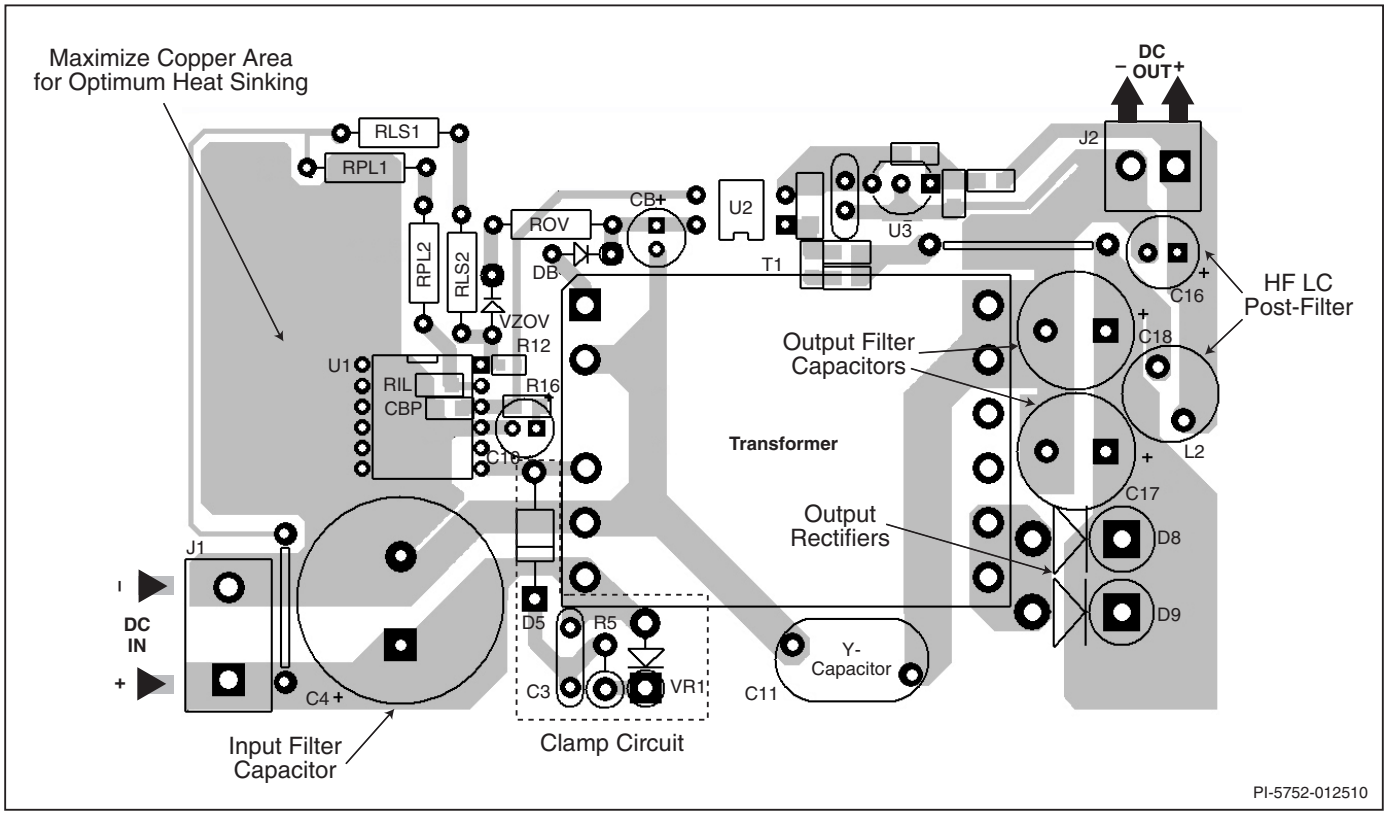


Figure 18a. Layout Considerations for TOPSwitch-JX Using V-Package.

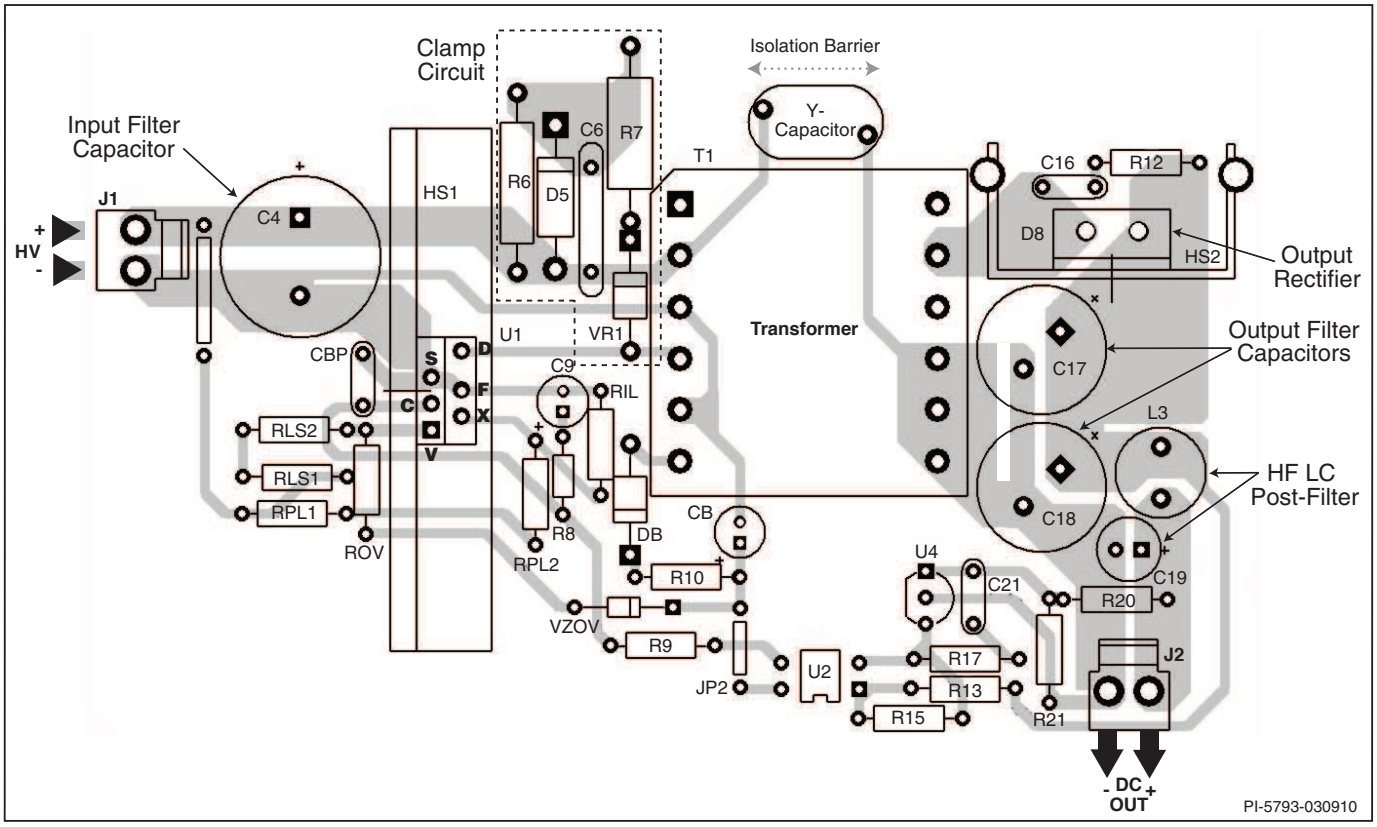


Figure 18b. Layout Considerations for TOPSwitch-JX Using E-Package.

R_D and the optocoupler LED determine the output voltage. Resistor R_{BIAS} provides a 1 mA bias current so that the Zener diode is operating close to its knee voltage. Resistor R_D sets the DC gain of the feedback. Both these can be 0.125 W or 0.25 W, 5% types. Selecting a Zener with a low test current (I_{ZT} ≤5 mA) is recommended to minimize the current needed to bias the feedback network, reducing no-load input power consumption.

For improved accuracy, Figure 15 shows a typical implementation using a reference IC. A TL431 is used to set the output voltage and is programmed via a resistor divider R_{S1} and R_{S2}. Resistor R_D sets the DC gain. The presence of capacitor C_T adds a pole very near 0 Hz (practically limited by the finite gain of the TL431) in the closed loop transfer function. Furthermore, C_T together with resistors R_T and R_{S1} form a low frequency zero (f_{Z1}) located at

$$f_{Z1} = \frac{1}{2\pi(R_T + R_{S1})C_T}$$

The component values should be chosen such that this zero occurs at approximately 100 Hz.

The 7 kHz internal pole from the TOPSwitch-JX provides the high frequency pole (f_{P1}) to complete the type 2 compensation configuration (see Figure 16).

In certain cases an increase in phase (phase boost) may be required near the crossover frequency. Once the desired crossover frequency f_C has been achieved through the selection of resistor R_D, an RC network (formed by R_B and C_B) can be placed across R_D can provide this phase boost. Recommended starting values for these components are

$$R_B \approx \frac{R_D}{9}$$

$$C_B \approx \frac{9}{10(2\pi \times R_B \times f_C)}$$

This arrangement places a pole zero pair (f_{Z2} and f_{P2}) which can typically provide about 30° of additional phase margin without significantly alerting the crossover frequency f_C (see Figure 17).

A post filter (L_{PF} and C_{PF}) is typically added to reduce high frequency switching noise and ripple. Inductor L_{PF} should be in the range of 1 µH – 3.3 µH with a current rating above the peak output current. Capacitor C_{PF} should be in the range of 100 µF to 330 µF with a voltage rating ≥1.25 x V_{OUT}. The combination of L_{PF} and C_{PF} should be such that their resonant frequency should occur at or slightly beyond 10 kHz. This is to ensure that there is no phase degradation due to the post filter inside the bandwidth of the power supply. If a post filter is used then the optocoupler should be connected as shown, before the post filter inductor and the sense resistors. Connecting after the post filter typically causes oscillation.

Table 7 is a list of commonly used optocouplers for feedback control of isolated switching power supplies. Use of an optocoupler with a typical CTR of 1 to 6 is recommended.

Tips for Designs

Design Recommendations:

- A soft finish circuit is recommended for high output voltage designs (>12 V) especially where large value output capacitors are used. This ensures start-up with full load at low line and also prevent output voltage overshoot. In Figure 22, R23, D6 and C19 show one implementation of the soft finish circuit.
- A 10 µF, 50 V electrolytic capacitor is recommended for the bias winding output filter to ensure appropriate bias voltage for the optocoupler when the power supply is unloaded. At high line and no-load, the bias voltage should not drop below 7 V (worst case) for best no-load input power performance. Adjust bias winding voltage or capacitor accordingly.

Circuit Board Layout

TOPSwitch-JX is a highly integrated power supply solution that integrates on a single die both the controller and the high voltage MOSFET. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practice to ensure stable and trouble free operation of the power supply.

When designing a PCB for the TOPSwitch-JX based power supply, it is important to follow the following guidelines:

Primary Side Connections

- Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the TOPSwitch-JX SOURCE pin and bias winding return. This improves surge capabilities by returning capacitive displacement currents that flow across the isolation barrier directly to the input filter capacitor.
- The CONTROL pin bypass capacitor should be located as close as possible to the SOURCE and CONTROL pins and its SOURCE connection trace should not be shared by the main MOSFET switching currents or bias winding return connection.
- All SOURCE pin referenced components connected to the VOLTAGE MONITOR (V) or EXTERNAL CURRENT LIMIT (X) pins should also be located closely between that pin and the SOURCE pin. The SOURCE connection trace of these components should not be shared by the main MOSFET switching or bias winding return currents. It is very critical that the SOURCE pin switching current is returned to the input capacitor negative terminal through a separate trace that is not shared by the components connected to CONTROL, VOLTAGE-MONITOR or EXTERNAL CURRENT LIMIT pins. This is because the SOURCE pin is also the controller ground reference pin. Any traces to the V or X pins should be kept as short as possible and physically away from the DRAIN node, clamp components or any node with high di/dt or dv/dt, to prevent noise coupling.
- The line sense resistor should be located close to the V pin to minimize the trace length on the high impedance V pin side. The DC bus side of the V pin resistor should be connected as close to the bulk capacitor as possible.
- In addition to the 47 µF CONTROL pin capacitor, a high frequency 0.1 µF bypass capacitor in parallel should be used for local decoupling (C_{BP} in Figure 18).
- The feedback optocoupler output should be routed away from any high voltage or high current traces to prevent noise coupling.

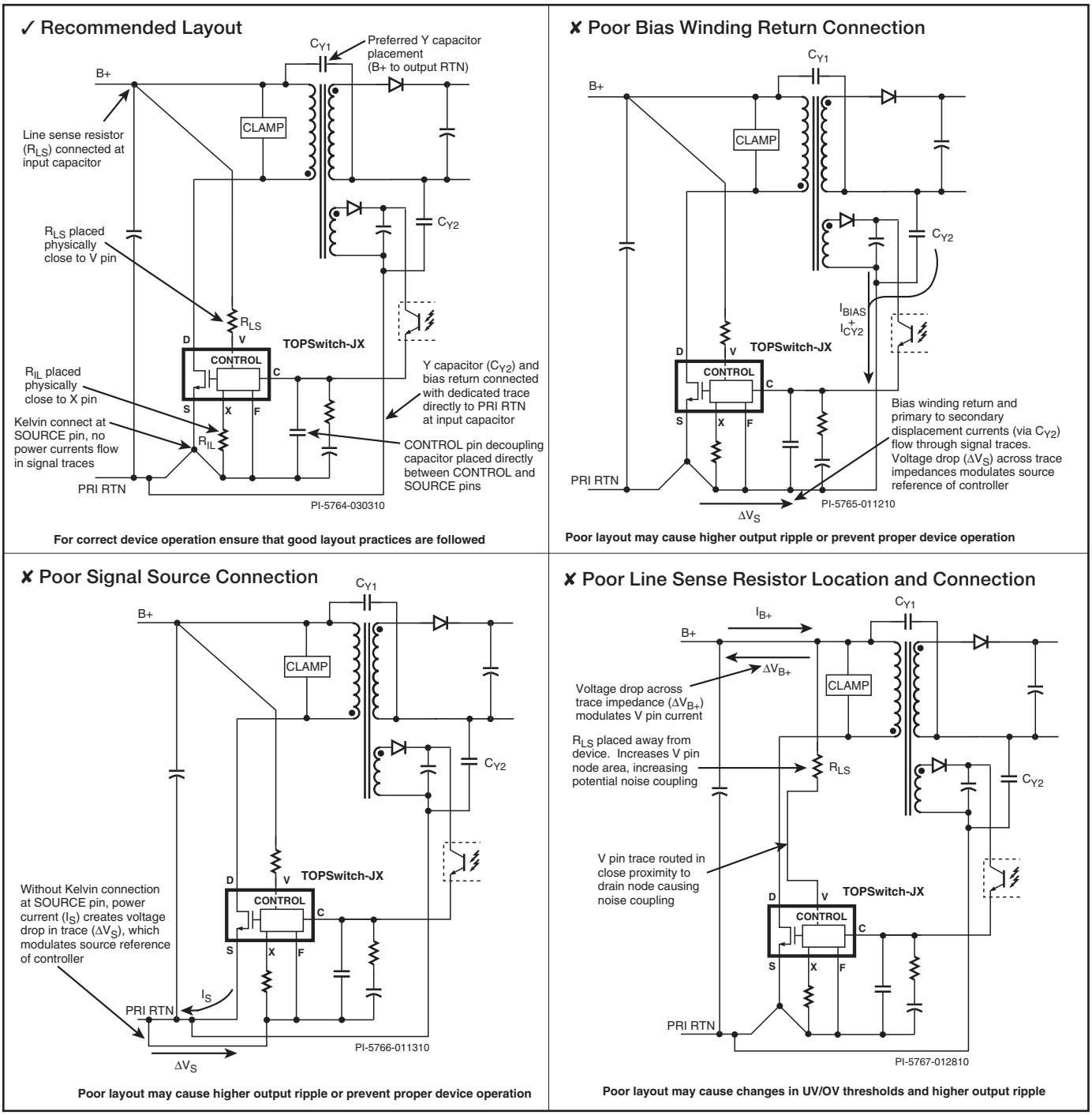


Figure 19. Layout Considerations (Shown Schematically) and Common Mistakes.

Y Capacitor

The preferred Y capacitor connection is close to the transformer secondary output return pin(s) and the positive primary DC input pin of the transformer. If the Y capacitor is connected between primary and secondary RTN, then the primary connection should be made via a dedicated trace from the Y capacitor to the negative input capacitor terminal. This ensures that line surge created displacement currents across the isolation barrier are routed away from traces connected to the TOPSwitch-JX.

Secondary

To minimize leakage inductance and EMI, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminal of the diode for heatsinking. A larger area is preferred at the quiet cathode terminal as a large anode area can increase high frequency radiated EMI.

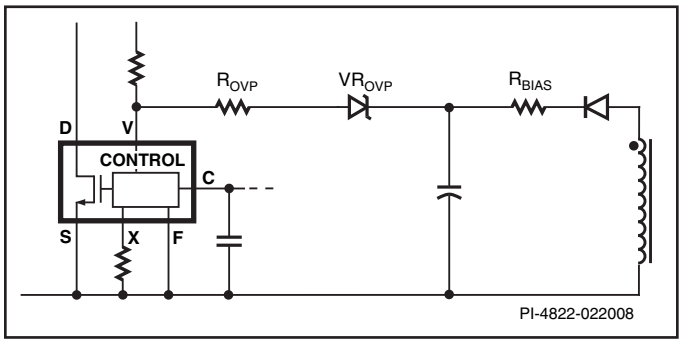


Figure 20. Primary Sensed OVP circuit for TOPSwitch-JX Based Flyback Power Supply.

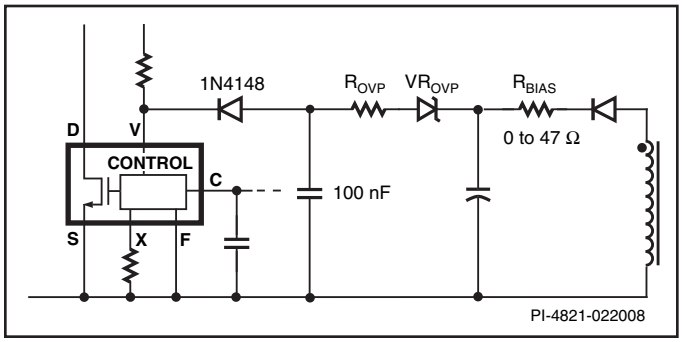


Figure 21. Primary Sensed Overvoltage Protection Circuit for a Flyback Power Supply Using TOPSwitch-JX with Additional V Pin Noise Decoupling.

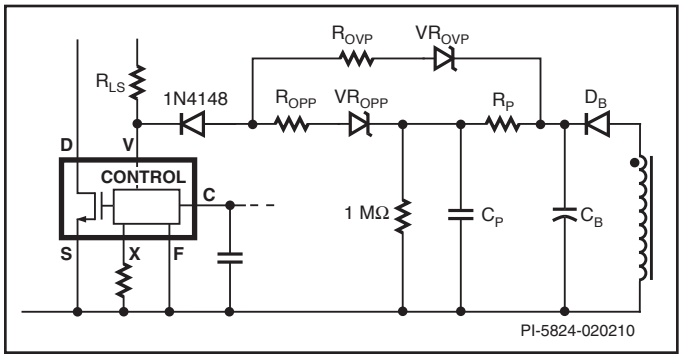


Figure 22. Implementation of Overvoltage Protection Together With Over-Power Protection Using the TOPSwitch-JX

Common Layout Problems to Avoid

A poor layout will often result in performance issues that may be time consuming to analyze, and they may occur at the end of development, when PCB design changes are difficult. Figure 19 will help quickly identify the root cause of a problem and correct the layout. The figure schematically shows common layout mistakes and the reasons they should be avoided

Light Load Efficiency and No-load Input Power Hints and Tips

Correct Power Meter Configuration

Figure 25 shows the two possible configurations for the voltage and current sense elements in a power meter and their typical impedances. The individual voltage and current elements are typically brought out onto the rear of the instrument allowing user configuration.

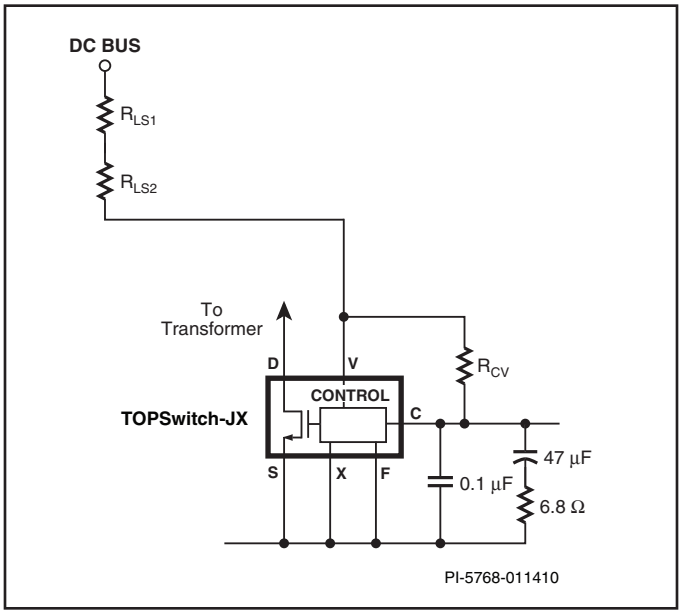


Figure 23. Biasing the V Pin from C Pin Allows for Lower No-load Power Consumption.

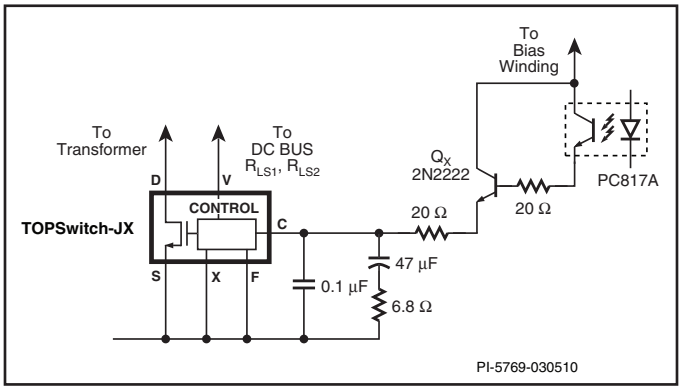


Figure 24. Use of Darlington Pair to Reduce No-load Input Power.

For low power measurements (<100 W) configuration (a) should be used. This prevents the static loss from the input impedance of the voltage sense element being included in the power readings. At 230 VAC this equals an error of 26 mW for a meter with 2 MΩ input impedance. This fails to meet the ≤0.01 W uncertainty requirement of most energy efficiency test methods (IEC 62301) when measuring no-load input power. Configuration (a) does introduce an error due to the voltage drop (power dissipation) across the current sense element. However for low current measurements this is typically negligible. For example for an 85 VAC, 2 A_{RMS} measurement the dissipation is 64 mW giving a power measurement error of <0.05% vs. the ≤2% requirement.

A quick check to see if the power meter is correctly configured is to apply 230 VAC to the power meter with no power supply unit (PSU) connected. If the power meter displays a non-zero power value then it is likely that configuration (b) is being used. Switch the power meter to configuration (a).

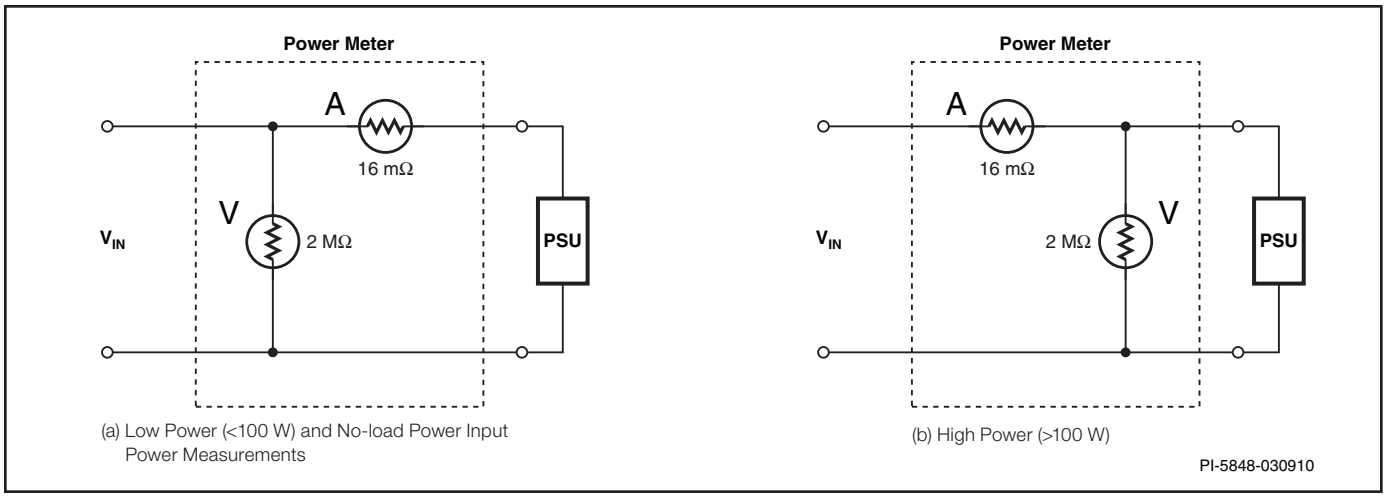


Figure 25. Correct Power Meter Configurations for Accurate Measurement of Low Power / No-load and Higher Power Designs. Configuration (a) is Recommended for TOPSwitch-JX Power Levels.

No-load Input Power Settling Time

When measuring input power under no-load or standby conditions ensure an adequate measurement time to allow the input power to stabilize. Figure 27 shows the typical settling time for a no-load input power measurement of a TOPSwitch-JX design at 230 VAC input. Input power measurements were taken using a Yokogawa WT210 power meter every 100 ms for 5.5 minutes (330 s). Note that a delay of >90 s is needed to obtain a power measurement within 3 mW (5%) of the final value (55.4 mW).

No-load Input Power Repeatability

TOPSwitch-JX has minimal no-load input power and light load efficiency variability which reduces the design margin needed to meet a given specification. Figure 26 shows an example of typical performance. Here the no-load of a single power supply was measured with 48 TOP266EG parts at a device temperature of both 25 °C and 100 °C. The total spread at a single temperature was <5 mW and <7 mW including data from both temperatures.

Improving Light Load Efficiency and No-load Input Power

During light load and no-load conditions the consumption of the feedback network, line sensing resistors and clamp are significant and without optimization can double the no-load input power of a design or significantly reduce available output power under standby conditions.

The following approaches can be followed to minimize these losses

- Minimize output pre-loads
- Connect line sense resistor to V pin
- Clamp choice and optimization
- Minimize bias winding voltage
- Increase value of line sense resistance
- Configure optocoupler transistor as part of Darlington pair
- Use of TLV431 vs. TL431 secondary reference IC

However before trying these techniques first verify that the power meter used to make input power measurements is correctly configured (Figure 25).

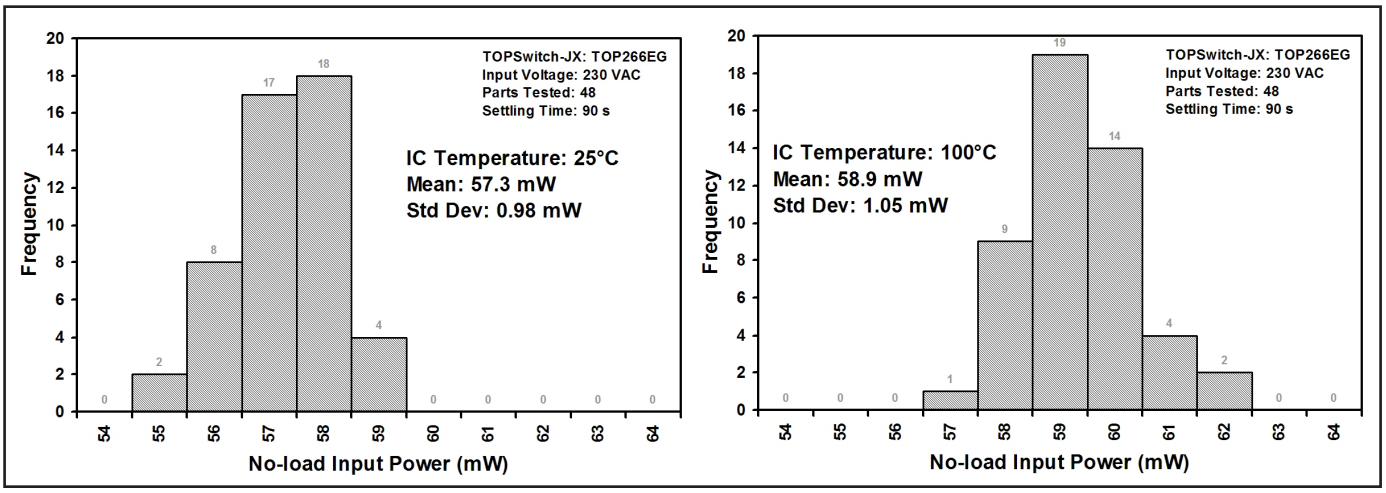


Figure 26. Example of Device to Device and Temperature Variation on No-load Input Power Measured in a Single Power Supply.

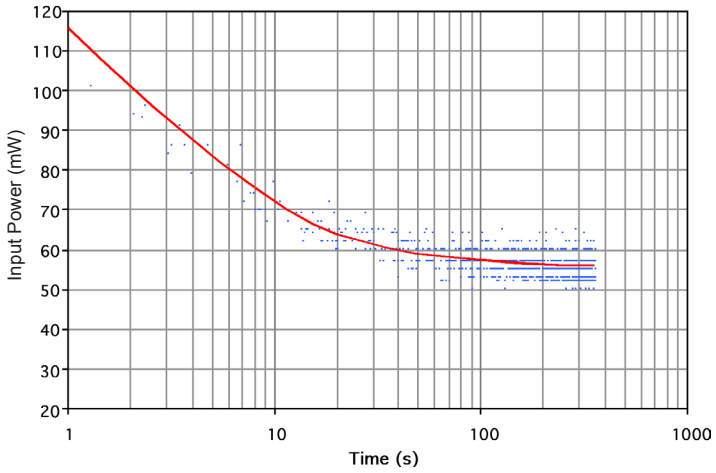


Figure 27. No-load Input Power Settling time. (Points Represent Instantaneous Measurements From Power Meter With No Filtering, Line Represents Averaged Measurements).

Minimize Output Pre-Loads

Output pre-loads are not required in single output TOPSwitch-JX designs and may be removed. In multiple output cases a small pre-load may be required on outputs to which the secondary side feedback network is not connected. Without a pre-load these outputs can peak charge significantly above their regulated voltages. To minimize no-load input power the value of pre-load resistors should be maximize. For lower dissipation a shunt regulator can be added to maintain a fixed difference between the main regulated output and a second output. Here to minimize losses the transistor of the shunt regulator should be configured to feed current into the regulated output rather then to output return.

Include Line Sense Resistor (Connected to V pin)

In addition to providing line undervoltage and overvoltage, connecting a line sense resistor to the V pin enables the line feed forward feature. This reduces the amount of current needed into the device CONTROL pin to program a given duty cycle as the line voltage is increased. As this current represents an output load (drawn from both the bias winding via the optocoupler transistor and output via to optocoupler LED) reducing the CONTROL pin current also reduces dissipation. This improves light load efficiency and no-load input power despite the additional dissipation of the line sense resistor itself.

Clamp Choice and Optimization

For lowest dissipation at light and no-load select either a Zener or Zener bleed clamp configuration. RCD clamps should be avoided as the resistor and capacitor value are selected to limit the peak drain voltage under full load and over-load conditions. However under light or no-load conditions the capacitor voltage discharges significantly as both the leakage inductance energy and switching frequency are lower. As the capacitor has to be recharged to above the reflected output voltage each switching cycle the lower capacitor voltage represents wasted energy. It has the effect of making the clamp dissipation appear as a significant load just as if it were connected to the output of the power supply.

Zener and Zener bleed clamp configurations solve this problem by preventing the voltage across the capacitor discharging below a minimum value (defined by the voltage rating of the Zener) and therefore minimizing clamp dissipation under light and no-load conditions.

Figure 13 shows recommended clamp configurations. Optimize the dissipation of the clamp by using the highest value for R_{CLAMP} that keeps the peak drain voltage below 675 V under the worst-case conditions of maximum AC input voltage and output overload just prior to loss of regulation and entering into auto-restart. Further information on clamp design is provided in Step 8 of the design flow.

Minimize Bias Winding Voltage Under No-load Conditions

On the primary side the feedback current into the CONTROL pin is fed from the output of the bias winding. Minimizing the voltage of the bias winding therefore reduces overall dissipation. Under no-load and maximum input voltage conditions monitor the bias winding capacitor voltage with an oscilloscope (C10 in Figure 31). Reduce the number of bias winding turns on the transformer until the minimum voltage seen is ≥7 V. Voltages below this can cause the optocoupler to cut off and results in a rise in the output voltage at no-load. Due to the integer nature of the bias winding turns it may not be possible to optimize the bias voltage perfectly and in this case the value of the bias capacitor may also be adjusted, increasing the value will increase the bias voltage slightly. Once optimized verify correct operation under transient loading conditions to ensure the bias voltage is always ≥7 V.

Increase Value of Line Sense Resistor

The dissipation of the line sense resistor can be reduced by adding an additional resistor from the device C to V pin (Figure 23). Resistor R_{CV} programs a fixed current from the CONTROL pin to the VOLTAGE MONITOR pin. This reduces the current needed from the DC BUS via R_{LS1} and R_{LS2} to exceed the line UV threshold current of the V pin. This allows the combined value of R_{LS1} and R_{LS2} to be increased from 4 MΩ to 10 MΩ while still maintaining the same line undervoltage threshold.

Although the line undervoltage (UV) threshold is maintained, the line overvoltage (OV) threshold voltage is doubled and the line feed-forward ripple rejection effectiveness reduced. In practice, for most consumer products, the higher line OV threshold has little impact due to the low 2 kV differential surge requirement that class of products has to withstand. This surge level results in a small increase in the DC bus voltage (filtered by the bulk capacitor) well below a voltage that could cause the device BV_{DSS} to be exceeded.

For proper operation of the device auto-restart feature a value <300 kΩ is required for R_{CV}.

Configure Optocoupler Transistor as Part of Darlington Pair

Configuring the optocoupler as one of the transistors in a Darlington pair (Figure 24) typically reduces no-load input power by ≥1 mA × V_O. The increased gain of the Darlington reduces the optocoupler LED (feedback) current required to provide a given CONTROL pin current to maintain output regulation.

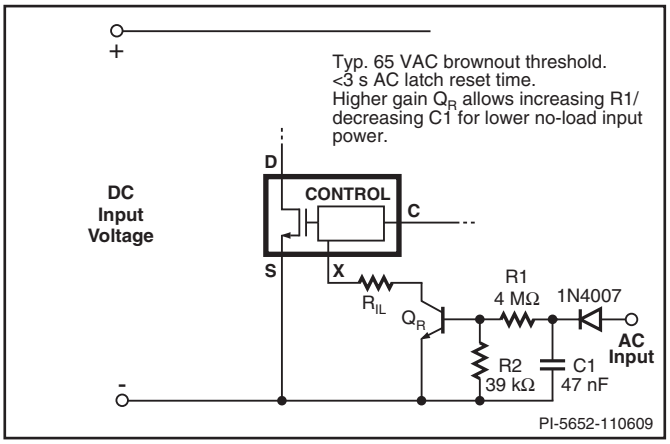


Figure 28. Externally Set Current Limit, Fast AC Latch Reset and Brownout.

As the secondary feedback current is sourced from the output, it represents an output load and therefore lowering the feedback current reduces this load and hence input power consumption. As the reduction is a function of the output voltage this approach is most effective for designs where the output feedback is derived from higher output voltage (>12 V).

Transistor Q_X can be any general purpose NPN type. For stability a small value resistor (20 Ω) should be added from the emitter of Q_X to the CONTROL pin. A second resistor from the base of Q_X to the emitter of the optocoupler transistor compensates for optocoupler leakage current. This is also the reason the gain of the optocoupler should be limited to a CTR rank of A (80-160%) to ensure that at high temperature the leakage of the optocoupler transistor doesn't modulate the feedback current.

On the secondary side the optocoupler LED series resistor (R16 in Figure 31) should be increased to correctly set the overall loop gain. A value of 10 times that of a standard feedback configuration is a good initial estimate which can then be adjusted based on the control loop bode plot.

Use of TLV431 vs. TL431 Secondary Reference IC

In high voltage output designs (>12 V) switching from a TL431 to TLV431 can reduce no-load consumption by reducing the bias current needed by the reference IC. For correct operation the TL431 requires a supply current of 1 mA whereas for the TLV431 this is reduced to 100 µA. This reduction in supply current (fed from a resistor in parallel to the optocoupler LED) directly reduces the output loading and therefore input power.

Implementing Overvoltage Protection Feature Using TOPSwitch-JX

The bias winding output tracks the changes in the output voltage for the flyback topology. If the feedback loop fails and results in an increase in output voltage, the voltage of the bias winding will also increase. This can be used to detect an output overvoltage condition (Figures 20, 21).

A suitable Zener diode with a series resistor connected between the bias winding output and the V pin can be selected such that the Zener diode conducts once the bias winding voltage rises

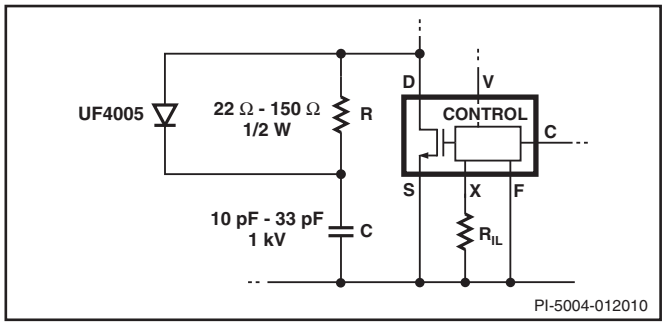


Figure 29. Recommended RCD Circuit for Higher Power Designs Using TOP269-271.

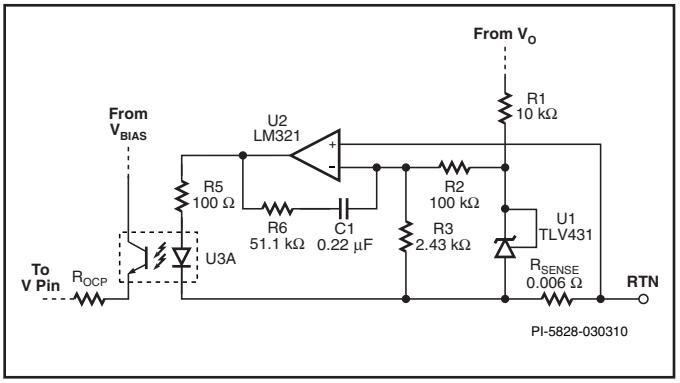


Figure 30. Implementation of Accurate Over-Current Protection Circuit.

significantly (typically 20 % to 30 %) above the highest voltage at the output of the bias winding during normal operation (or under a transient loading condition during normal operation). A current injected in the V pin in excess of 112 µA will result in the switching cycle being terminated instantaneously. If the injected current remains higher than 112 µA for over 100 µs, the part will enter hysteretic OV shutdown. In such a situation, switching will resume as soon as the injected current reduces below the hysteresis point after completing an auto-restart cycle.

If the injected current exceeds 112 µA, the V pin responds by dropping the V pin voltage by 0.5 V. If the drop in V pin voltage causes the V pin current to jump to a value higher than 336 µA, the part enters a state of latched shutdown. If the value of the series resistor R_{OVP} is very small (in the range of 5 Ω to 22 Ω), the change of V pin voltage in response to the injected current reaching 112 µA is adequate to cause a current in excess of 336 µA to flow which results in latched overvoltage condition, requiring a reset. In this state the operation will not resume unless the input AC is cycled and the C pin capacitor is allowed to discharge, thereby resetting the part. Alternatively the latch may also be reset by disconnecting the X pin from the S pin. The TOPSwitch-JX stops switching and resets the OVP latch when it detects that less than 27 µA is being pulled out of the X pin.

This property is used in the Fast AC Reset circuit shown In Figure 28. The figure shows a simple internal latch reset circuit using a single BJT. The voltage on capacitor C1 changes much more rapidly as compared to the bulk capacitor allowing for a fast reset of the latch when the AC is cycled.

In some designs the Zener diode connected from the bias winding may become a source of noise injected into the V pin. This happens when the bias winding output ripple is high, or the circuit board layout allows noise from adjacent circuits to be coupled in the trace connecting the Zener diode to the V pin. In such a situation, the solution shown in Figure 21 should be used.

Implementing Over-Power Protection (OPP)
Primary side sensed over-power protection can be implemented via the V pin by sensing the voltage on the bias winding. Figure 22 shows this configuration. Zener diode VR_{OVP} provides the output overvoltage protection and VR_{OPP} together with R_P and C_P provides overpower protection. This approach works well where the desired OPP limit is >150% of the full load output power.

The OPP feature relies on the imperfect coupling between the secondary and the bias winding. As the output load increases the bias winding voltage rises due to the effect of leakage inductance. If the bias voltage exceeds the voltage rating of VR_{OPP} current flows into the V pin causing the device to stop switching. The shutdown can be made latching or non-latching through the value of R_{OPP}, 5.1 kΩ results in non-latching while <22 Ω results in latching shutdown. To prevent false triggering during transient loads and startup R_P and C_P provide a delay, with a recommended time constant of approximately 2 ms or longer than the duration of any peak load conditions.

The voltage of VR_{OVP} should be higher than VR_{OPP} to prevent false triggering of OVP during startup and load transients

Implementing an Accurate Over-Current protection (OCP)
The over-power protection (OPP) can also be used as a form of (loose) over-current protection. However if an accurate over-current protection (OCP) feature needs to be implemented, then a separate optocoupler based circuit can be used to detect the OCP threshold and turn off the switching device through the V pin.

Figure 30 shows an implementation of an accurate over-current protection circuit. The load current is monitored by measuring the voltage drop across a current sense resistor R_{SENSE}. Shunt regulator IC U1 together with resistor divider network formed by R2 and R3 is used to generate an accurate voltage reference of 0.03 V at the inverting input of op-amp U2. This low voltage sense threshold allows for the use of small current sense resistors. Resistor R6 and C1 provide frequency compensation. In this example the value of R_{SENSE} is chosen such that the over-current threshold is set at 5 A. At this programmed current, the voltage across R_{SENSE} exceeds the reference voltage (0.03 V) causing the op-amp output to rise. This forward biases the diode in optocoupler thereby triggering a shutdown through the V pin. The value of R_{OCP} defines latching or non-latching shutdown, 5.1 kΩ results in non-latching while <22 Ω results in latching shutdown. If the over-current limit specification is wide, then a small signal diode may be used instead of U2 as a voltage reference.

Designing High-Power Power Supplies Using TOPSwitch-JX

At high power levels design of power supplies using a Flyback topology requires additional considerations.

1. Proximity losses in the transformer can be significant and makes design of flyback transformers at high power levels very sensitive to the construction method with respect to winding configuration and the choice of the number of strands in multi wire configuration. The choice of wire size in a high frequency transformer is dependent on switching frequency. Skin depth is proportional to switching frequency and limits the usable cross sectional area of each conductor. Multi-strand (filar) windings and litz wires are commonly used to reduce conduction losses in high frequency transformers. To further reduce skin effects, the use of foil windings is recommended especially for low voltage high current (>6 A) outputs.
2. Slight increases in leakage inductance of the transformer and PCB traces can lead to a large increase in dissipation in the snubber circuit. To reduce leakage inductance it is important to use sandwich winding construction in the transformer and minimize PCB trace lengths, especially the loop formed by the secondary winding, output diode and output capacitors. Design of the snubber circuit is critical in achieving high efficiency; typically at high power levels a correctly sized RCDZ clamp will ensure that the drain source voltage does not exceed 680 V.
3. At high output currents the secondary ripple current increases and may be above the rating of a single very low ESR output capacitor. It is therefore common to use multiple capacitors in parallel. In this case special attention must be paid to equalize the trace length to all capacitors to give even distribution of the ripple current. This ensures equal dissipation and temperature rise, critical to ensure an acceptable operating life. Even with multiple capacitors a second stage LC filter is required to reduce switching frequency ripple.
4. Minimize the length and loop area of PCB traces which carry large switching currents and voltages as these can be a source of radiated EMI.

For high power designs using any TOPSwitch-JX and especially for designs that use TOP269 – TOP271, it is recommended that provision is made on the PCB board for a small RC (or RCD) network positioned between the drain and source terminals (Figure 29). This reduces switching noise from affecting power supply operation and also helps in reducing radiated EMI. A 22 Ω to 150 Ω resistor and a 1 kV rated ceramic capacitor in the range of 10 pF to 33 pF will be suitable for most applications.

The addition of the diode reduces power dissipation in the snubber by up to a factor of 2.

Quick Design Checklist

As with any power supply, all TOPSwitch-JX designs should be verified with actual hardware to ensure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – verify that peak V_{DS} does not exceed 680 V at highest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just before the power supply goes into auto-restart (loss of regulation).
2. Maximum drain current – at maximum ambient temperature, maximum input voltage and maximum output load, verify

drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. TOPSwitch-JX has a minimum leading edge blanking time of 180 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit envelope for the drain current waveform at the end of the 180 ns minimum blanking period.

3. Thermal check – at maximum output power, minimum input voltage and maximum ambient temperature; verify that temperature limits are not exceeded for the TOPSwitch-JX, transformer, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation in the $R_{DS(ON)}$ of TOPSwitch-JX, as specified in the data sheet. A maximum SOURCE pin temperature for the V package or tab temperature for E package of 110 °C is recommended to allow for these variations. Alternatively, the design margin can be verified by connecting an external resistance that is in series with the DRAIN pin and is attached to the same heatsink. The resistance selected would be equal to the difference between the measured $R_{DS(ON)}$ of the device under test and the worst case maximum specification.

Appendix A

Application Example

Low No-load, High Efficiency, 65 W, Universal Input Adapter Power Supply

The circuit shown in Figure 31 shows a 90 VAC to 265 VAC input, 19 V, 3.42 A output power supply, designed for operation inside a sealed adapter case type. The goals of the design were highest full load efficiency, highest average efficiency (average of 25%, 50%, 75% and 100% load points), and very low no-load consumption. Additional requirements included latching output overvoltage shutdown and compliance to safety agency limited power source (LPS) limits. Measured efficiency and no-load performance is summarized in the table shown in the schematic which easily exceed current energy efficiency requirements.

In order to meet these design goals the following key design decisions were made.

PI Part Selection

- One device size larger selected than required for power delivery to increase efficiency.

The current limit programming feature of TOPSwitch-JX allows the selection of a larger device than needed for power delivery. This gives higher full load, low line efficiency by reducing the MOSFET conduction losses ($I_{RMS}^2 \times R_{DS(ON)}$) but maintains the overload power, transformer and other components size as if a smaller device had been used.

For this design one device size larger than required for power delivery (as recommended by the power table) was selected. This typically gives the highest efficiency. Further increases in device size often results in the same or lower efficiency due to the larger switching losses associated with a larger MOSFET.

Line Sense Resistor Values

- Increasing line sensing resistance from 4 MΩ to 10.2 MΩ to reduce no-load input power dissipation by 16 mW.

Line sensing is provided by resistors R3 and R4 and sets the line undervoltage and overvoltage thresholds. The combined value of these resistors was increased from the standard 4 MΩ to 10.2 MΩ. This reduced the resistor dissipation, and therefore contribution to no-load input power, from ~26 mW to ~10 mW. To compensate the resultant change in the UV (turn-on) threshold resistor R20 was added between the CONTROL and VOLTAGE-MONITOR pins. This adds a DC current equal to ~16 μA into the V pin, requiring only 9 μA to be provided via R3 and R4 to reach the V pin UV (turn-on) threshold current of 25 μA and setting the UV threshold to 95 VDC.

This technique does effectively disable the line OV feature as the resultant OV threshold is raised from ~450 VDC to ~980 VDC. However in this design there was no impact as the value of input capacitance (C2) was sufficient to allow the design to withstand differential line surges greater than 2 kV without the peak drain voltage reaching the BV_{DSS} rating of U1.

Clamp Configuration – RZCD vs. RCD

- An RZCD (Zener bleed) was selected over an RCD clamp to give higher light load efficiency and lower no-load consumption.

The clamp network is formed by VR2, C4, R5, R6, and D2. It limits the peak drain voltage spike caused by leakage inductance to below the BV_{DSS} rating of the internal TOPSwitch-

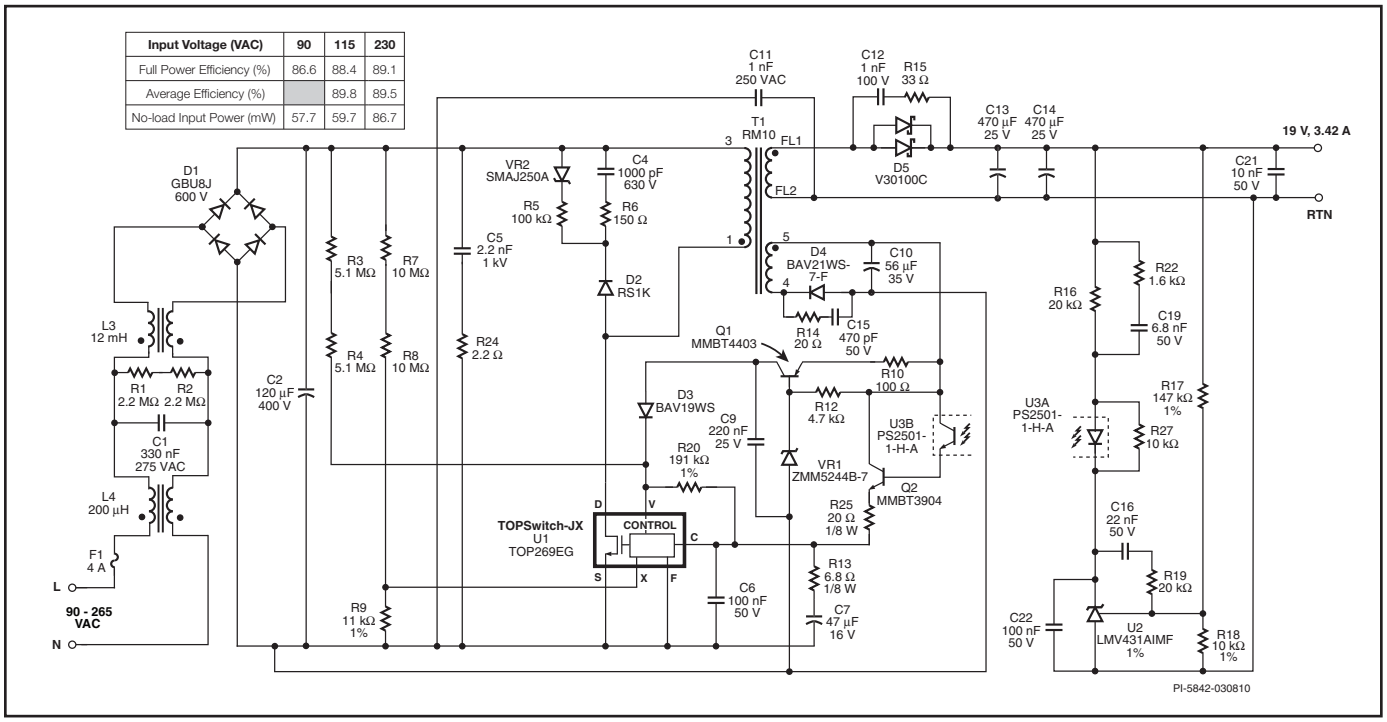


Figure 31. Schematic of High-Efficiency 19 V, 65 W, Universal Input Flyback Supply With Low No-Load.