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Simblee™ RFD77402
IoT 3D ToF Sensor Module

Simblee™ IoT 3D ToF Sensor Module RFD77402
DATASHEET

Features

- Fully Integrated microelectronic device with an embedded sensor and VCSEL(Vertical Cavity Surface Emitting Laser)
  - 850 nm VCSEL and electronic driver
  - Optical receiver sensor and optics
  - Microelectronic controller
- Time-of-Flight (ToF) is a highly accurate distance mapping and 3D imaging technology
- Eye safe invisible infrared (IR) illumination using a class 1 laser emitter
- High accuracy and high repeatability
- I^2C interface for device control and data transfer
- Ultra-small SMD package
- Standard solder reflow compatible
- Lead-free, RoHS compliant
- Small size 4.8mm x 2.8mm x 1mm

Applications

- Absolute and highly accurate distance measurement at distances ranging from 100 mm to 2000 mm
- User detection for IoT devices
- Robotics applications such as obstacle detection and obstacle avoidance
- White goods type of applications such as hand detection in automatic faucets and soap dispensers
- 1D gesture recognition
- Directional movement detection along Z-axis
- Volume or height control

Contents

1 General Characteristics

1.1 Technical Specifications

Performance and power consumption can be tuned to the application needs by changing configuration and/or through a customized firmware.

Table 1: Technical Specifications

Parameter	Unit	Description
Package size	mm	4.8 x 2.8 x 1.0 (LxWxH)
Interface		I2C (up to 1 MHz)
Light source (type/wavelength)	nm	VCSEL / 850 nm
Field of Illumination	degree	29° @1/e2
Field of View	degree	55° @1/e2
Measurement range	mm	100 mm to 2000 mm (*)
Maximum refresh rate	Hz	10
Precision	%	+/-10 (*)
Laser eye safety		Class 1 laser product
MSL		Class 3

(*) target with 90% reflectivity in dark environment and no cover glass

1.2 Electrical Specifications

Table 2: Electrical Characteristics

Parameter	Unit	Min	Typ	Max
Standby current	µA	9.3	9.7	15
Current consumption (@ full range, 10 Hz –worst case)	mA	-	7	15
Operating voltage	V_{DD}	2.7	3.0	3.3
Pull-up voltage	$V_{pull-up}$	1.8	-	VDD
Interrupt Pull-up Voltage	V_{INT}	1.8 +/- 10%(3*)	-	V_{DD}
Operating temperature	°C	-10	-	60
Temperature not to exceed	°C	-	-	250
I2C: SDA and SCL				
V_{IL}	V	0	-	0.56
V_{IH}	V	1.29	-	V_{DD}
V_{OL} (@ 3 mA)	V	-	0.02	-
I_{OL} (@ V_{OL} = 0.4 V)	mA	-	8	-

(*) Note that a pull-up to 1.8V implies that INT pin is configured as open drain (failure in doing so will cause high leakage).

1.3 System Block Diagram and Device Pinout

Figure 1: RFD77402 Block Diagram and Device Pinout (top view)

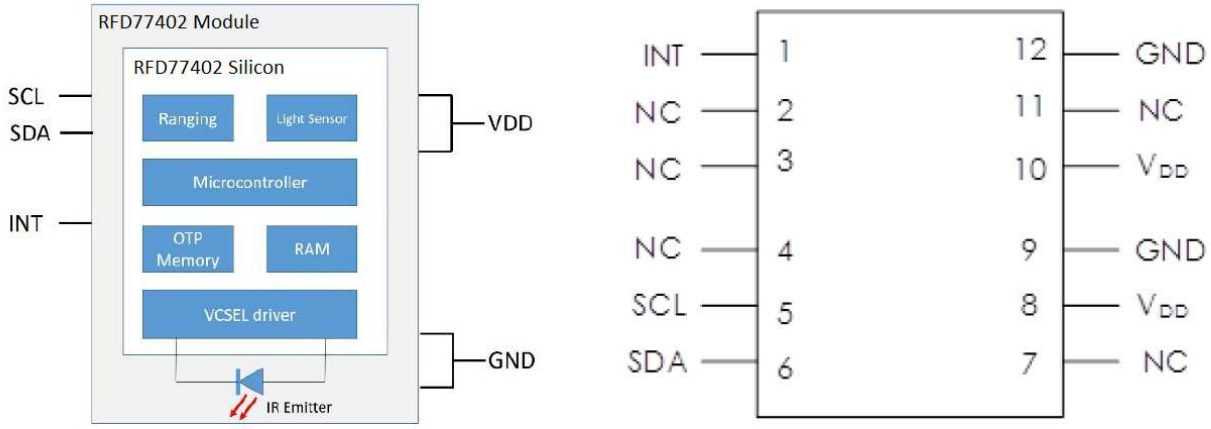
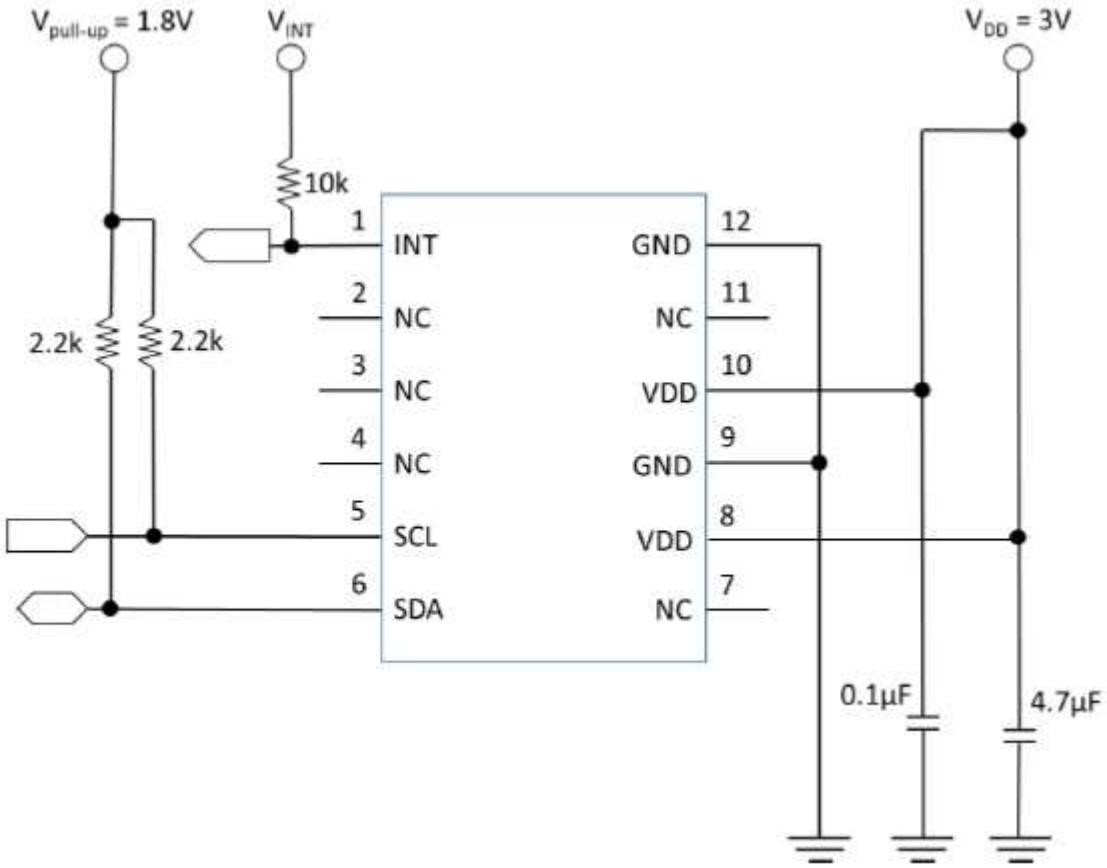


Table 3: Device Pinout

Pin Number	Signal Name	Signal Type	Signal Description
1	INT	Digital output	Indicator pin for valid measurement
2	NC	NC	No Connect
3	NC	NC	No Connect
4	NC	NC	No Connect
5	SCL	Digital input	I2C serial clock
6	SDA	Digital input/output	I2C serial data
7	NC	NC	No Connect
8	V_{DD}	Supply	Power Supply
9	GND	Ground	To be connected to main ground
10	V_{DD}	Supply	Power Supply
11	NC	NC	No Connect
12	GND	Ground	To be connected to main ground

1.4 Electrical Connectivity

Figure 2: Electrical Connectivity Schematic



2 Module Interface

2.1 Electrical Interface

The Simblee Time-of-Flight (TOF) Module interface is a standard 7-big address I²C slave (slave ID 0x4C) device capable up to 1Mbit/s.

The ToF module I²C interface supports a direct 8-bit addressing scheme used to access the module user's register set. This addressing scheme is functional also during standby mode since the module interface and the user's register set remain powered for a faster response.

The module I²C interface supports an additional 16-bit indirect addressing scheme that is mainly used for debugging purpose or special operations.

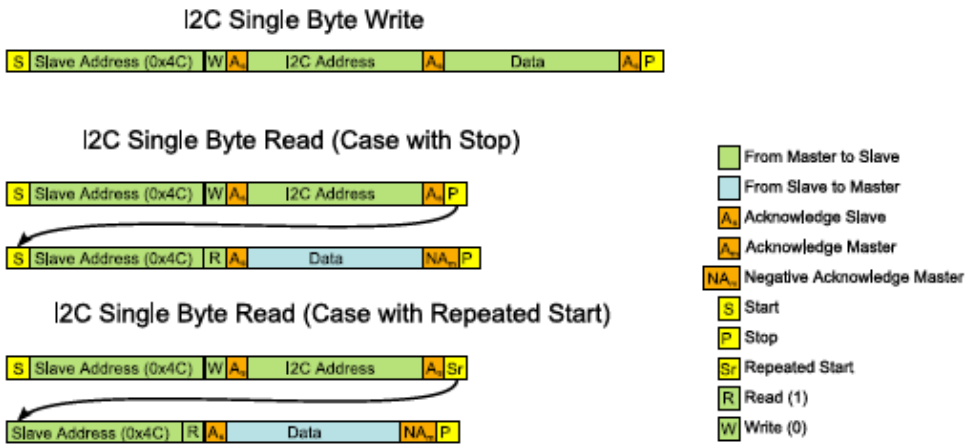
Both direct and indirect addressing schemes support the I²C address auto increment feature and word mode. When the address auto increment feature is disabled, the word mode setting is ignored. Word mode setting controls the data source/destination only when address auto increment is enabled. In such case the word mode forces the transferred data stream to be sequentially read from (or written to) the same 15-byte location pointed by the initial address.

The auto increment features and other modes of operation of the I²C interface are controlled by the I²C Init Configuration Register.

2.1.1 I²C Single Byte Access

When accessing the device one byte at a time there is no dependency from the I²C Init Configuration Register.

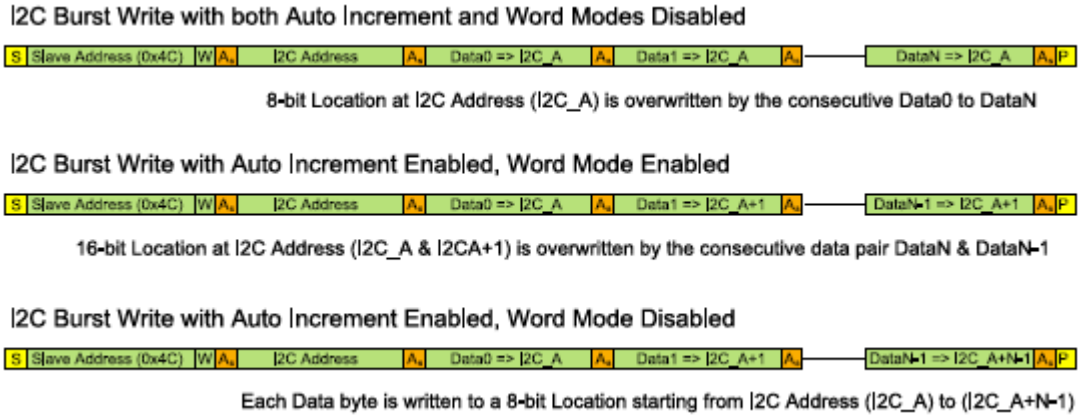
Figure 3: I²C Basic 8-bit Read and Write Cycles



2.1.2 I²C Write Access with Auto Increment and Word Mode Features

When performing a burst write to the I²C interface, the module response depends on the setting of bits 1:0 of the I²C Init Configuration Register controlling the address auto increment features and word mode. If none of these modes are enabled, the data burst write is going to be directed to the same I²C address. In case of address auto increment, the data is written sequentially to the location starting with initial the I²C address. In case both modes are enabled, each 2-byte from the data burst stream is going to overwrite the 2-byte location pointed by the I²C address.

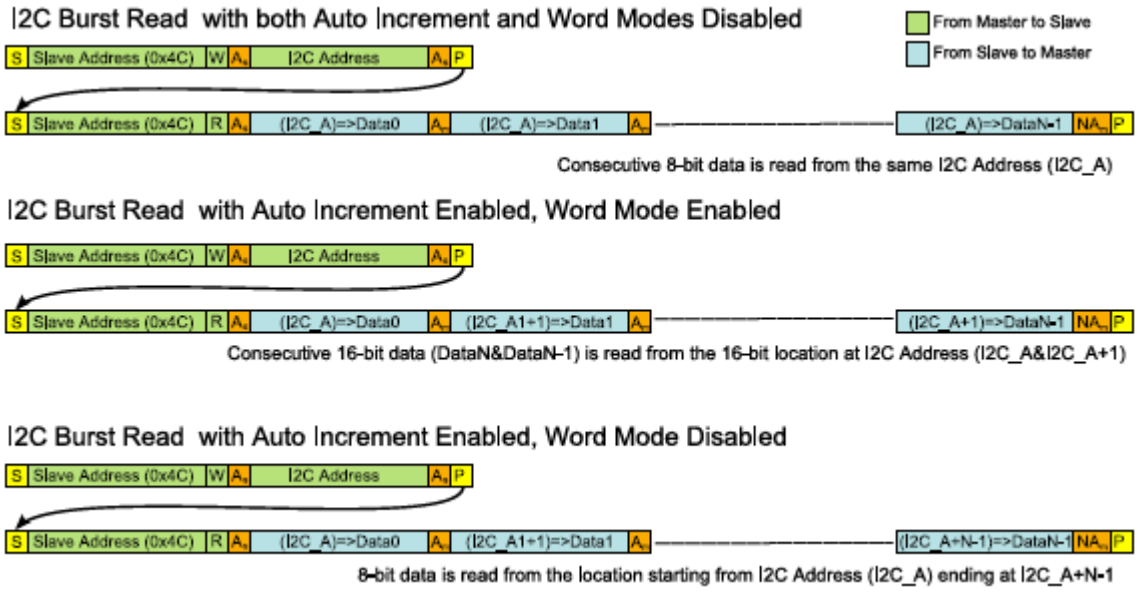
Figure 4: I²C Write Direct Access: Auto Increment and Word Mode Options



2.1.3 I²C Read Access with Address Auto Increment and Word Mode Features

The behavior of the address auto increment and word mode features are similar to the one previously described for the I²C burst write.

Figure 5: I²C Burst Read: Address Auto Increment and Word Mode



2.1.4 I²C Write Indirect Addressing with Address Auto Increment and Word Mode

As previously mentioned, the ToF module supports an I²C indirect address scheme. In this case, the 16-bit address is written to the register. Each subsequent byte will be written to the 16-bit address location pointed by the register in a manner that depends on bits 2:3 of the I²C Init of the Configuration Register (address auto increment and word mode control bits).

Figure 6: I²C Indirect Address Burst Write with Address Auto Increment and Word Mode

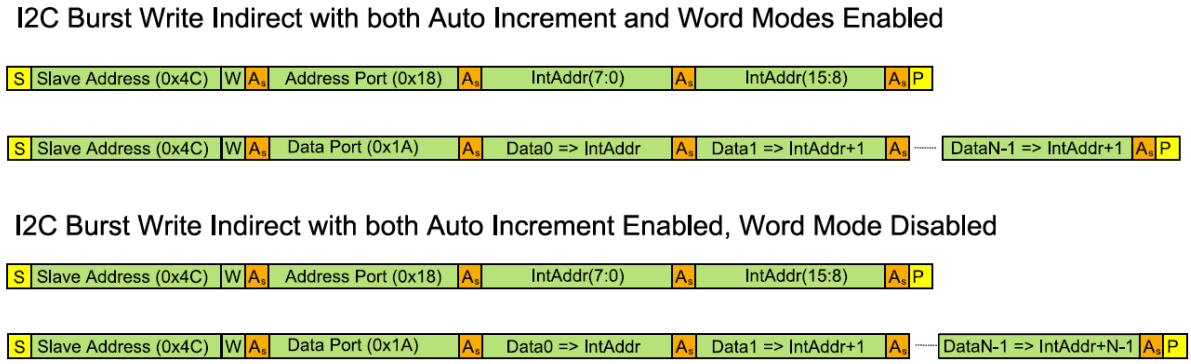


Figure 7: I²C Indirect Address Write with Address Auto Increment and Word Mode (1-Byte Access)

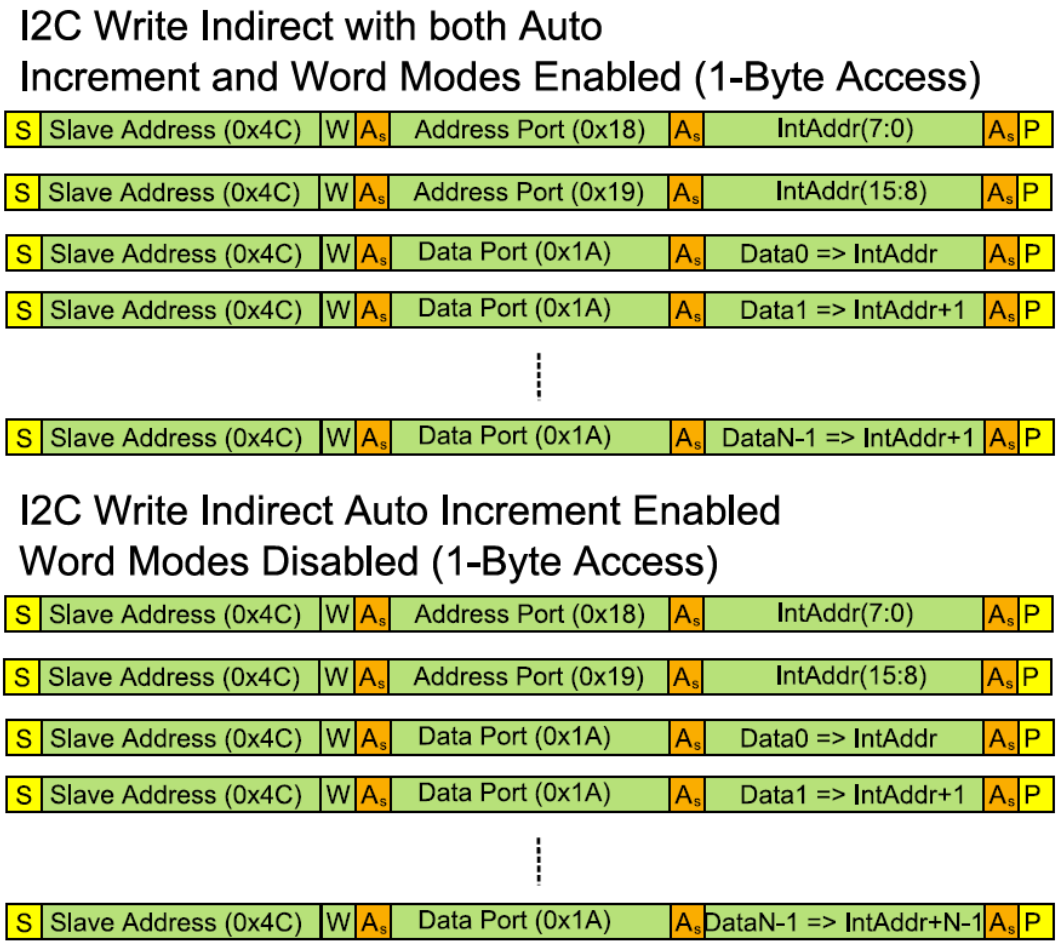
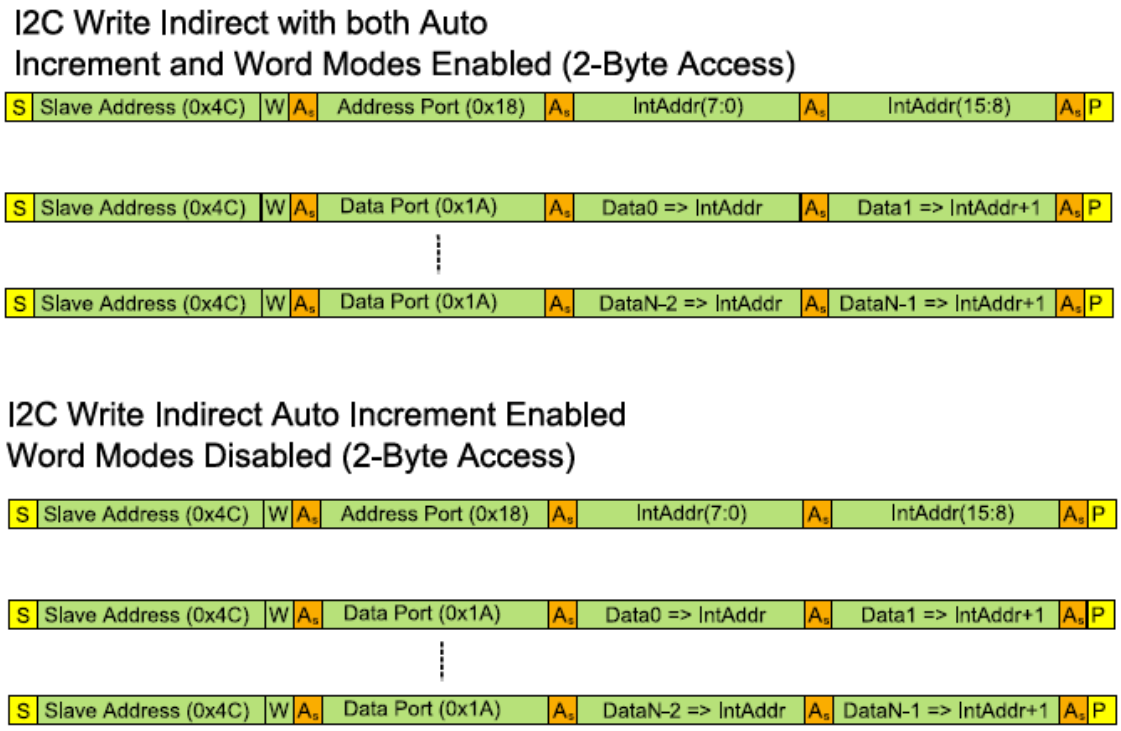


Figure 8: I²C Indirect Address Write with Address Auto Increment and Word Mode (2-Byte Access)



2.1.5 I²C Read Indirect Addressing with Address Auto Increment and Word Mode

The indirect addressing I2C read follows the same rules as described above in terms of address auto increment and word mode.

Figure 9: I²C Burst Read Indirect Addressing

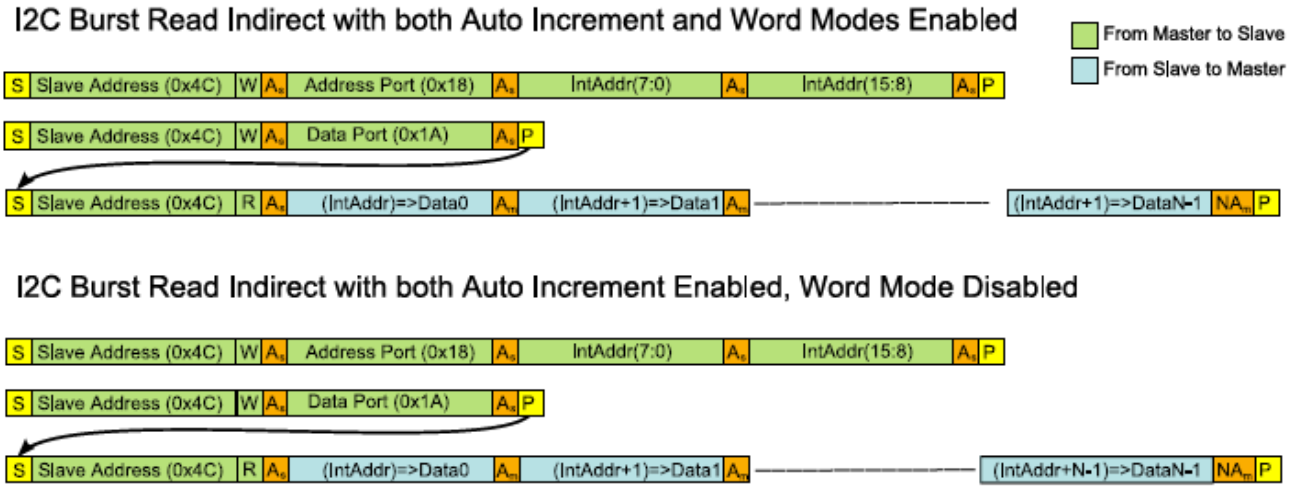


Figure 10: I²C Indirect Address Read with Address Auto Increment and Word Mode (1-Byte Access

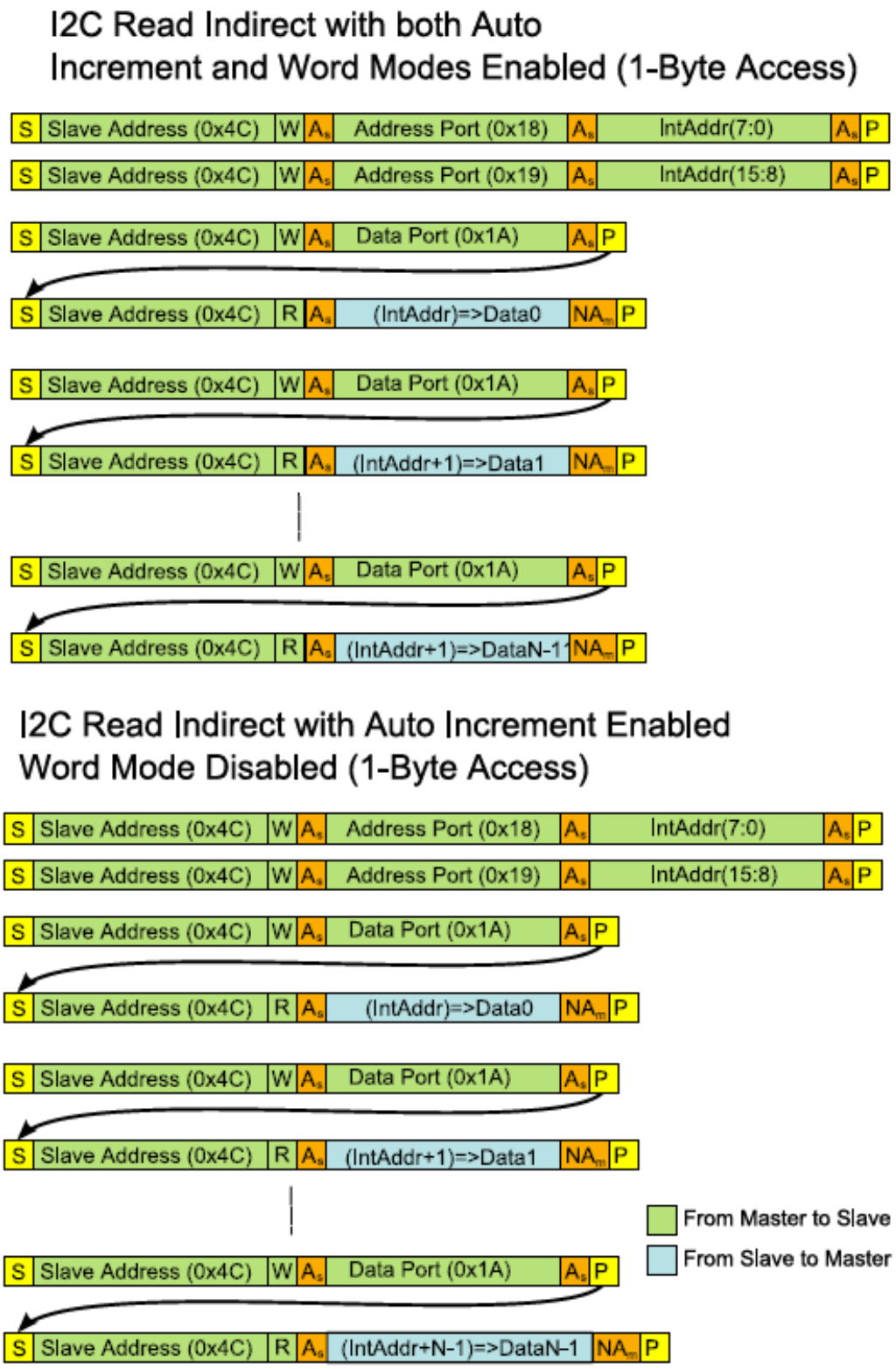
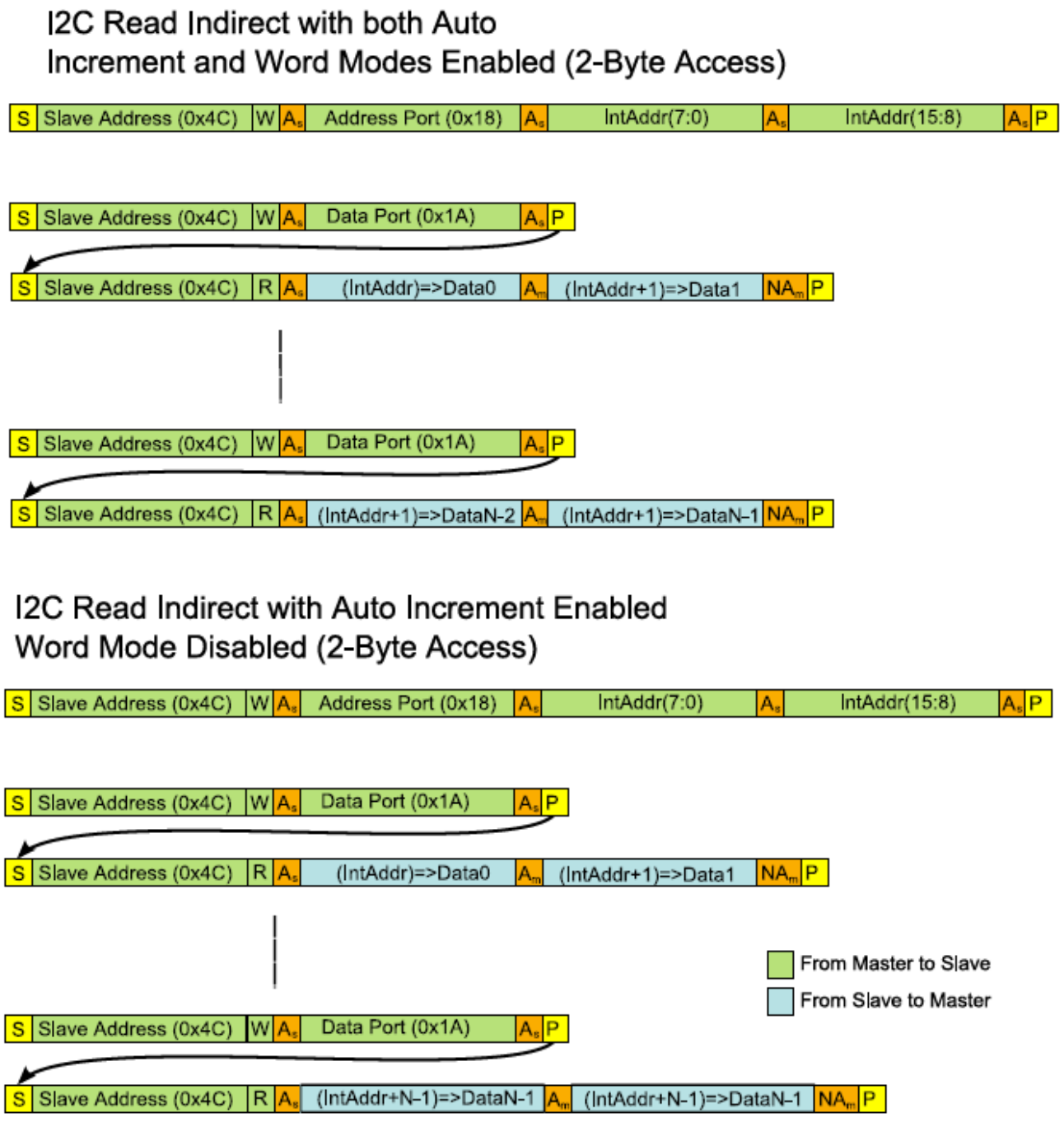


Figure 11: I²C Indirect Address Read with Address Auto Increment and Word Mode (2-Byte Access)



2.1.6 I²C Timing Information

Figure 12: I²C Timing Characteristics Definitions

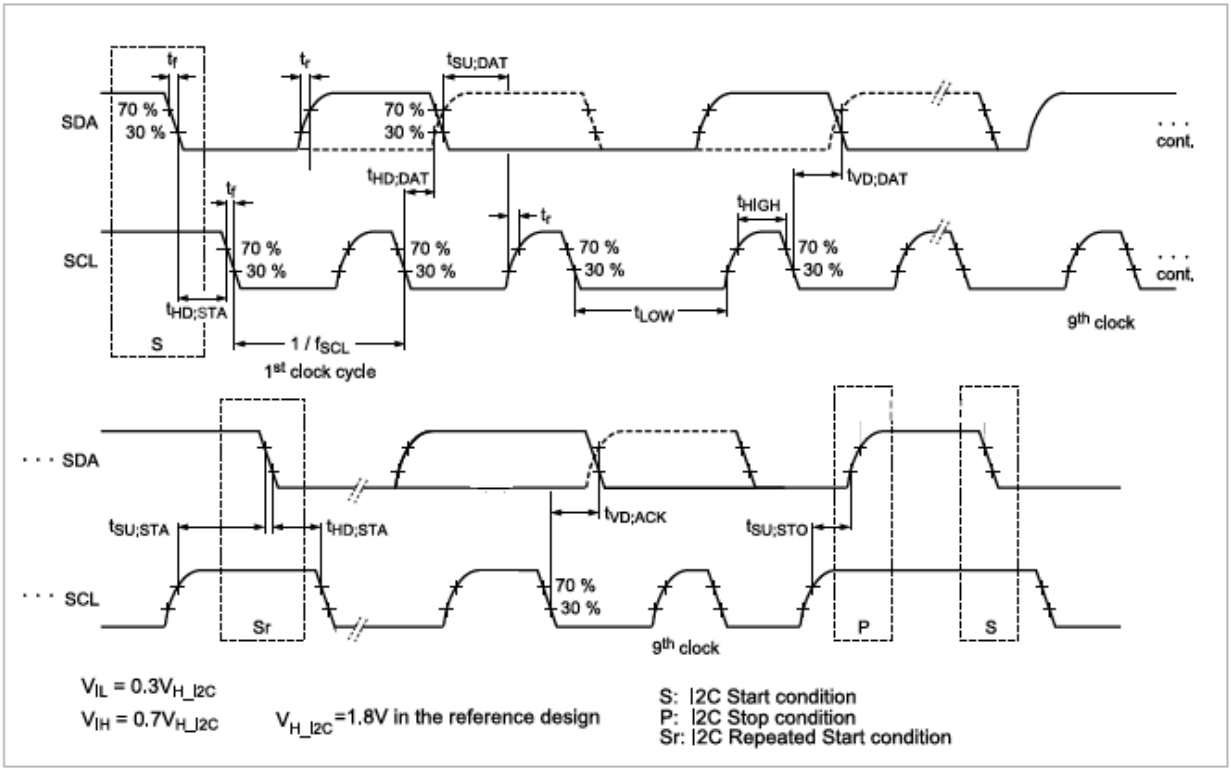


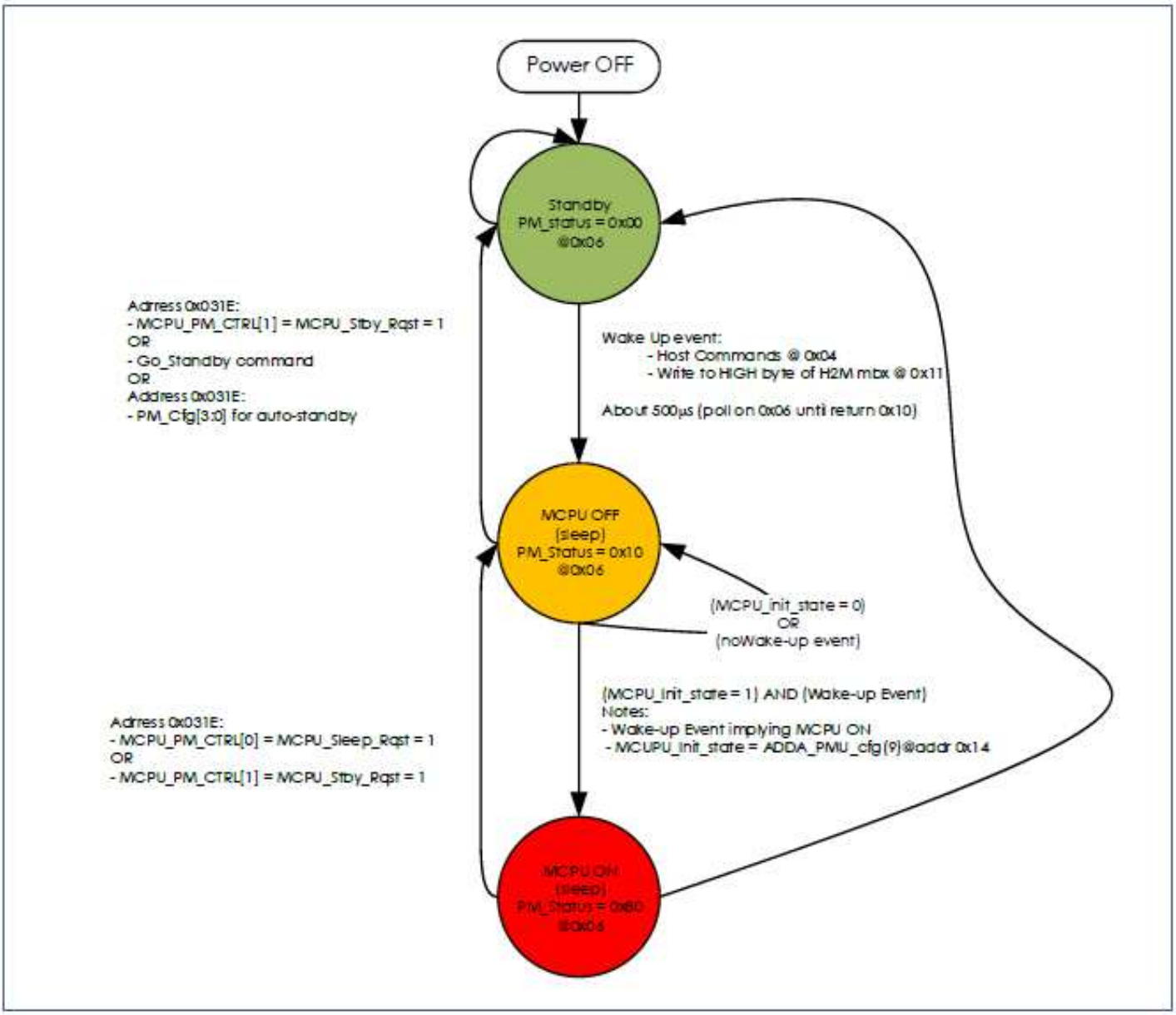
Table 2: I²C Timing Characteristics Information

Parameter	Definition	Min	Max	Unit
f_{SCL}	I2C SCL clock frequency	100	1000	kHz
$t_{HD,STAs}$	I2C (repeated) start condition hold time	0.26	-	µs
t_{LOW}	Low period of the SCL clock	0.5	-	µs
t_{HIGH}	High period of the SCL clock	0.26	-	µs
$t_{SU,STA}$	Setup time for a repeated I2C start condition	0.26	-	µs
$t_{HD,DAT}$	I2C data hold time	0	-	ns
$t_{SU,DAT}$	I2C data setup time	50	-	ns
t_r	Rise time of SDA and SCL signals	-	120	ns
t_f	Fall time of SDA and SCL signals	20 x (VDD/5.5 V)	120	ns
$t_{SU,STO}$	Setup time for I2C stop condition	0.26	-	µs
$t_{VD,DAT}$	I2C data valid time	-	0.45	ns
$t_{VD,ACK}$	I2C data valid acknowledge time	-	0.45	ns

2.2 Host Interface Power Management

The module enters standby mode once power is applied. To wake up the module to a fully on state (MCPU responding) the user must set to '1' bit 9 ("MCPU_Init_State") of the register PMU Configuration Register at address 0x14 and then issue a command that will then cause the MCPU to wake up. A command issued to the module with "MCPU_Init_State" not set to '1' will cause the module to exit the Standby state and go in MCPU OFF state. In this state power is applied to the rest of the module but the MCPU is off.

Figure 13: Module State Diagram



2.2.1 Standby / Leakage in Different Electrical Conditions

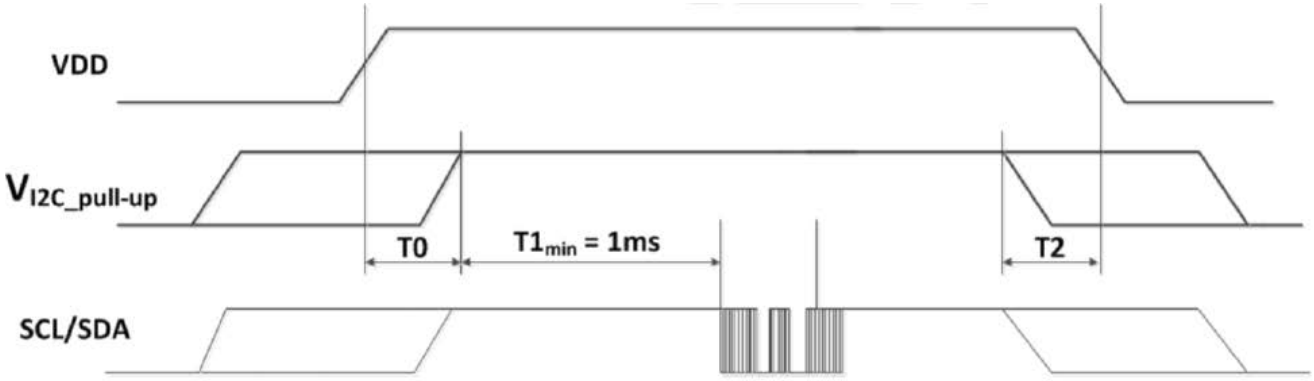
Table 5: I²C SCL/SCA Power-up/down Sequence

Electrical Conditions		Max Leakage (µA)
$V_{I2C\_pull-up}$	VDD	MLAX-0X
0 V	0 V	No leakage
1.8 V	0 V	No Leakage
0	3 V	60 µA
1.8 V	3 V	15 µA

2.2.2 Power-up and power-down Sequence

Figure 14 below shows the RFD77402 power up and power down sequence. Please note that the module itself has no restrictions in terms of VDD and VI²C_pull-up sequencing, but in the case of VDD ON while VI²C_pull-up supply unit offers a path to GND. The value of such leakage current depends on the power supply impedance to GND. Therefore, unless the power supply unit offers a significantly high impedance to GND limiting such leakage, the application designer should avoid keeping VDD ON while VI²C_pull-up Is OFF for a long time (steady state).

Figure 14: I²C SCL/SDA Power-up/down Sequence



2.3 Module Programming Interface

The I²C Interface registers defined in this section remain powered when in standby mode. For this reason, these registers are accessible at any time through the I²C direct address scheme.

Note that the addresses of these registers are provided as 16-bit addresses according to the internal MCPU memory map. The external user must use the least significant byte of the address to access these registers through the I²C direct addressing scheme.

Table 6: Host Interface Registers

Name	I2C Address	Type	Size [Bytes]	Description
ICSR	0x00	R/W	1	Interrupt Control Status Register
IER	0x02	R/W	1	*Interrupt Enable Register*
Cmd_R	0x04	R/W	1	Command Register
Dev_Status_R	0x06	R/O	2	Device Status Register
Rslt_R	0x08	R/O	2	Result Register
RsltCnfdR	0x0A	R/O	2	Result Confidence Register
Cmd_CfgR_A	0x0C	R/W	2	Command Configuration Register A
Cmd_CfgR_B	0x0E	R/W	2	Command Configuration Register B
H2M_mbx	0x10	R/W	2	Host to MCPU Mailbox Register
M2H_mbx	0x12	R/O	2	: MCPU to Host Mailbox Register
PMU_Cfg	0x14	R/W	2	: PMU Configuration Register
I2C_Ad_ptr	0x18	R/W	2	I2C Address Pointer Register
I2C_Data_port	0x1A	R/W	1	I2C Data Port Register
I2C_Init_cfg	0x1C	R/W	1	I2C Init Configuration Register
MCPU_PM_Ctrl	0x1E	R/W	1	MCPU Power Management Control Register
HFCfg_0	0x20	R/W	2	HW/FW Configuration Register 0
HFCfg_1	0x22	R/W	2	HW/FW Configuration Register 1
HFCfg_2	0x24	R/W	2	HW/FW Configuration Register 2
HFCfg_3	0x26	R/W	2	HW/FW Configuration Register 3
Mod_Chip_ID	0x28	R/O	2	Module Chip ID Register
Ptch_MCfg	0x2A	R/W	2	Patch Memory Configuration Control Register

2.3.1 Configuration Parameters

Table 7: Configuration Parameters Used to Configure the Module

Parameter Name	Field	Suggested Value	Register	Description
Refresh Rate Continuous Measurement	Cmd-CfgR-A	0x01	Cmd_CfgR_A [6:0] @ 0x0C	Refresh Rate for continuous measurement in 100s of milliseconds
HFCfg_0	HFCfg_0 (11:0)	0x7D0	HFCfg_0[11:0] @ 0x20	HW/FW Configuration Register 0
HFCfg_1	HFCfg_1 (11:0)	0x008	HFCfg_1[11:0] @ 0x22	HW/FW Configuration Register 1
HFCfg_2	HFCfg_2 [3:0]	0xA	HFCfg_2[15:12] @ 0x24	HW/FW Configuration Register 2
HFCfg_3	HFCfg_3	1	HFCfg_3[4] @ 0x26	HW/FW Configuration Register 3
HFCfg_3b	HFCfg_3b	1	HFCfg_3b [7] @ 0x26	HW/FW Configuration Register 3b
Conditional Measurement	Cond_measurement_ready_ev	0	HFCfg_3[11] @ 0x26	A '1' enables conditional measurement ready event.

2.3.2 Module Interface Registers

The following registers are used by the system host for module configuration and for operational communication. The user should not attempt to modify reserved fields as this could cause unpredictable behavior.

Table 8: Interrupt Control Status Register

Name: ICSR
Address: 0x00
Size: 1 Byte

General Description:
This register is used by the I2C host to configure, gain status information and clear the interrupts.

Bit	Name	Type	Detailed Description
0	Int_Clr_cfg	R/W	Interrupt clear mechanism. A '1' causes the Int_status(0) to be cleared by the Host reading the Result Register. A '0' causes the same interrupt to be cleared by a host read of the *Interrupt Control Status Register*. Typical setting is '1'.
1	Int_clr_type	R/W	A '1' in this register disables the clearing of interrupt upon reading. In such condition interrupts are clearing by writing a '1' to the proper "Int_Clr" bit in the Interrupt Enable Register.
2	INT_MODE	R/W	PAD INT_mode. When '0' the interrupt pad is open drain. When '1' it is in push-pull mode.
3	INT_Polarity	R/W	INT_polarity. When '0' interrupts are active low. When '1' interrupts are active high.
7:4	Int_status(3:0)	R/O	These bits are used to indicate the source of the interrupt. Note that the functionality of these bits is independent from the interrupts being enabled or not. If interrupts are disabled the I2C Host system will need to poll on these bits. Note that interrupts are generated by MCPU write/read activities. Bit 0: A '1' indicates the presence of an active interrupt related to newly available data in the Result Register. This bit can be cleared by the Host reading the ICSR or the Result Register depending on the setting of bit 0 (int_clr_cfg) Bit1: A '1' indicates an active interrupt related to a newly available message in the M2H mailbox register. This bit is cleared by the Host reading the M2H mailbox register. Bit 2: A '1' indicates that the MCPU have read the H2M mailbox register and that the Host can write it again without the risk to overwrite the previous data. This bit is cleared by Host reading the ICSR. Bit 3: A '1' indicates that a device HW reset has happen and is completed.

Table 9: Interrupt Enable Register

Name: IER
Address: 0x02
Size: 1 Byte

General Description:
This register is used to enable the individual source of interrupt to the I2C host system.

Bit	Name	Type	Detailed Description
3:0	Int_En(3:0)	R/W	Interrupt Enable: A '1' in any of these bits enables the notification/interrupt correspondent to associated Int_status bit in the ICSR register.
7:4	Int_Clr(3:0)	W/O	When the *int_rdclr_dis* bit is active, the Host needs to use these bits to clear interrupts. A '1' written to any of these bits clears the associated interrupt.

Table 10: Command Register

Name: Cmd_R
Address: 0x04
Size: 1 Byte

General Description:
This register is used by the host to issue predefined commands. A write to this register will generate an interrupt. A particular opcode is also reserved for reset or standby. If MCPU is in sleep mode, any write to this register should cause the HW to take the necessary actions (turn on oscillator) required for MCPU to be able to respond to the command.

Bit	Name	Type	Detailed Description
5:0	Cmd_Opcode(5:0)	R/W	Command Opcode: 0x01 - Single measure 0x10 - Go Standby 0x11 - Go MCPU off state 0x12 - Wake up MCPU to ON mode
6	Reset	R/W	Reset. A transition from 0 to 1 will be interpreted by the hardware as a reset to initial power-up state (standby).
7	Valid	R/W	This bit is written as '1' to indicate a valid command. An MCPU read of this register causes this bit to be cleared (command acknowledge indication to host). If the Host writes '1' to this bit (indicating need for acknowledge) it should also refrain from writing a new Cmd_Opcode until this bit is cleared by MCPU.

Table 11: Device Status Register

Name: Dev_Status_R
Address: 0x06
Size: 2 Bytes

General Description:
This register is used to report general status information.

Bit	Name	Type	Detailed Description
4:0	PM_status(4:0)	R/O	These bits are used to report module status: 0x00 – Standby (lowest module power mode) 0x10 – MCPU off (SRAM init) 0x18 – MCPU on
5	Osc_status	R/O	A '1' indicates that the oscillator is enable and running.
6	CPU_status	R/O	A '1' indicates that the MCPU is in WFI (power on, clock freeze). A '0' indicates that it is in normal mode
7	Pwr_status	R/O	A '1' indicates that main VDD is on and good. If '0' bandgap or main VDD is not enabled or not good.
15:8	Reserved	R/O	Reserved

Table 12: Result Register

Name: Rslt_R
Address: 0x08
Size: 2 Bytes

General Description:
This register is used to report the measured distance result.

Bit	Name	Type	Detailed Description
1:0	Reserved	R/O	Reserved
12:2	Distance	R/O	This 11-bit value represents the distance in number of mm (0 to 2047mm). In case of error code different from '00' this field cannot be considered valid. Special conditions: a. Actual distance is greater or equal to 2047mm (max value) b. Error code not equal to 0b00=> distance field set to 0x000. Error code = 0b00 and Distance field = 0x7FF =>
14:13	Err_code	R/O	This 2-bit value represents the error code. This field should be always checked to determine the validity of the distance field. '00' - Distance field valid (no error) '01' - Near target indication (not enough pixels valid) '10' - Far field (not enough signal) '11' - General Error (sensor pixels saturated)
15	Valid	R/O	A '1' indicates that values loaded in this register are the result of a new calculation reported by the internal MCPU. This event will generate an interrupt to the host system also indicated through the interrupt status register.

Table 13: Result Confidence Register

Name: RsIt_CnfdR
Address: 0x0A
Size: 2 Bytes

General Description:
This register provides a measure of the confidence of the result that depends on the detected signal amplitude.

Bit	Name	Type	Detailed Description
3:0	Val_pixels	R/O	Number of valid pixels. If this is 0 also the no FOV will be set indicating the measure is not valid.
14:4	Vec_ampl	R/O	This signal represents the average vector amplitude as a measure of the quality of the measure. Definition of this field depends on internal firmware and can be changed as needed.
15	Reserved	R/O	Reserved

Table 14: Command Configuration Register A

Name: Cmd_CfgR_A
Address: 0x0C
Size: 2 Bytes

General Description:
This is used to configure internal parameters.

Bit	Name	Type	Detailed Description
6:0	Reserved	R/W	Reserved
7	Reserved	R/W	Reserved
11:8	Reserved	R/W	Reserved
15:12	Reserved	R/W	Reserved

Table 15: Command Configuration Register B

Name: Cmd_CfgR_B
Address: 0x0E
Size 2 Bytes

General Description:
This is used to configure internal parameters.

Bit	Name	Type	Detailed Description
7:0	Reserved	R/W	Reserved
11:8	Reserved	R/W	Reserved
15:12	Reserved	R/W	Reserved

Table 16: Host to MCPU Mailbox Register

Name:	**H2M_mbx**	**General Description:** This is a mailbox that can be written from the Host and read by the internal MCPU. The MCPU can enable an interrupt indicating that the Host has written a message to this mailbox. The notification / interrupt is trigger by the Host writing the byte at address 0x011 (high byte of the mailbox). If MCPU is in sleep mode, any write to this register should cause the HW to take the necessary actions (turn on oscillator …) required for MCPU to be able to respond to the command.
Address:	**0x10**	
Size:	**2 Bytes**	

Bit	Name	Type	Detailed Description
15:0	H2M_data(15:0)	R/W	Host to MCPU message

Table 17: MCPU to Host Mailbox Register

Name:	**M2H_mbx**	**General Description:** This is a mailbox that can be written (and also read back) from the MCPU and read by external Host. The Host can enable an interrupt to be notified when the MCPU writes a message to this mailbox. The notification / interrupt is triggered by the MCPU writing the byte at address 0x013 (high byte of the mailbox).
Address:	**0x12**	
Size:	**2 Bytes**	

Bit	Name	Type	Detailed Description
15:0	M2H_data(15:0)	R/O	MCPU to Host mailbox

Table 18: PMU Configuration Register

Name: **PMU_Cfg**

Address: **0x14**

Size: **2 Bytes**

Bit	Name	Type	Detailed Description		
3:0	Reserved	R/W	Reserved		
7:4	Patch_mem_dvd(3:0)	R/W	Used to configure Patch memory ddvd. This portion of programming SRAM can be programmed not to lose power in standby.		
			Bit	Description	
			2:0	'0' - 1.15 V	'4' - 0.95 V
				'1' - 1.10 V	'5' - 0.90 V
				'2' - 1.05 V	'6' - 0.85 V
				'3' - 1.00 V	'7' - 0.80 V
			3	A '1' enables low DVDD mode;	
8	Patch_code_ld_en	R/W	A '1' enables loading of patch code (patch code is otherwise read only). When load is finished clear to 0. Patch code can be done only when in CPU off mode.		
9	MCPU_init_state	R/W	A '1' enables MCPU to run coming out of standby. A '0' will hold MCPU off and for external initialization to complete.		
10	Reserved	R/W	Reserved		
11	Reserved	R/W	Reserved		
15:12	Reserved	R/W	Reserved		

Table 19: I²C Address Pointer Register

Name: **I2C_Ad_Ptr**

Address: **0x18**

Size: **2 Bytes**

General Description:
This is the I2C address register with auto increment capabilities. The Host will write to this register the 16-bit address of the location that it wants to access and then read or write the I2C Data port. During a burst read/write, this register is automatically incremented. This feature allows read/write of data in burst from/to consecutive locations.

Bit	Name	Type	Detailed Description
15:0	I2C_addr_reg(15:0)	R/W	I2C port Address register with auto increment capabilities

Table 20: I²C Data Port Register

Name: I2C_Data_port
Address: 0x1A
Size: 1 Byte

General Description
Writing or reading to this port is equivalent to write and read the location addressed by the combination of the I2C Address pointer

Bit	Name	Type	Detailed Description
7:0	I2C_data_p(7:0)	R/W	I2C indirect access Data port. MCPU or debug I2C does not see this port.

Table 21: I²C Init Configuration Register

Name: I2C_Init_cfg
Address: 0x1C
Size: 1 Byte

General Description:
Used for miscellaneous I2C access configuration.

Bit	Name	Type	Detailed Description	
7:0	I2C_acc_cfg(7:0)	R/W	These bits are used to configure I2C access.	
			Bit	**Functional Description**
			0	A '1' enables address to increment.
			1	A '1' enables 16-bit word access mode (bit 0 should be 1 if this is set. The least significant address bit toggles 0,1,0 ...).
			2	A '1' enables auto increment feature when accessing the data port.
			3	A '1' enables 16-bit word access mode when accessing the data port (bit 2 should be 1 when using this feature).
			4	A '1' enables MCPU debug I2C.
			5	A '1' enables Host debug access.
			6	A '1' enables MCPU debug access.
			7	Reserved