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RFM65W ISM RECEIVER MODULE V1.2

GENERAL DESCRIPTION

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The RFM65W is a low cost receiver module capable of operation in 315,433,868 and 915 MHz license-free ISM (Industry Scientific and Medical) frequency bands. All major RF communication parameters are programmable and most of them can be dynamically set. The RFM65W offers the unique advantage of programmable narrow-band and wide-band communication modes. The RFM65W is optimized for low power consumption while offering high sensitivity and channelized operation. Compliance ETSI and FCC regulations.

In order to better use RFM65W modules, this specification also involves a large number of the parameters and functions of its core chip RF65's, including those IC pins which are not leaded out. All of these can help customers gain a better understanding of the performance of RFM65W modules, and enhance the application skills.

RFM65W

KEY PRODUCT FEATURES

- High Sensitivity: down to -120 dBm at 1.2 kbps
- High Selectivity: 16-tap FIR Channel Filter
- Bullet-proof front end: IIP3 = -18 dBm, IIP2 = +35 dBm, 80 dB Blocking Immunity, no Image Frequency response
- Low current: Rx = 16 mA, 100nA register retention
- Constant RF performance over voltage range of module
- FSK Bit rates up to 300 kb/s
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK demodulation
- Built-in Bit Synchronizer performing Clock Recovery
- Incoming Sync Word Recognition
- 115 dB+ Dynamic Range RSSI
- Automatic RF Sense with ultra-fast AFC
- Packet engine with CRC, AES-128 encryption and 66-byte FIFO
- Built-in temperature sensor and Low Battery indicator
- Module size:19.7X16mm

APPLICATIONS

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control

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Acronyms

BOM	Bill Of Materials
BR	Bit Rate
BW	Bandwidth
CCITT	Comité Consultatif International Téléphonique et Télégraphique - ITU
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
Fdev	Frequency Deviation
FIFO	First In First Out
FIR	Finite Impulse Response
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
ID	IDentificator
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
ITU	International Telecommunication Union
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non Return to Zero
OOK	On Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
POR	Power On Reset
RBW	Resolution BandWidth
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
Rx	Receiver
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SR	Shift Register
Stby	Standby
Tx	Transmitter
uC	Microcontroller
VCO	Voltage Controlled Oscillator
XO	Crystal Oscillator
XOR	eXclusive OR

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This product datasheet contains a detailed description of the RFM65W performance and functionality.
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1. General Description

The RFM65W is a receiver module ideally suited for today's high performance ISM band RF applications. It is intended for use as high-performance, low-cost FSK and OOK RF receiver for robust frequency agile RF links, and where stable and constant RF performance is required over the full operating range of the device down to 1.8V.

The RFM65W is intended for applications over a wide frequency range, including the 315MHz,433 MHz ,868 MHz and 915 MHz ISM bands. Coupled with a very aggressive sensitivity, the advanced system features of the RFM65W include a 66 byte RX FIFO, configurable automatic packet handler, listen mode, temperature sensor and configurable DIOs which greatly enhance system flexibility whilst at the same time significantly reducing MCU requirements.

The RFM65W complies with both ETSI and FCC regulatory requirements

1.1. Simplified Block Diagram

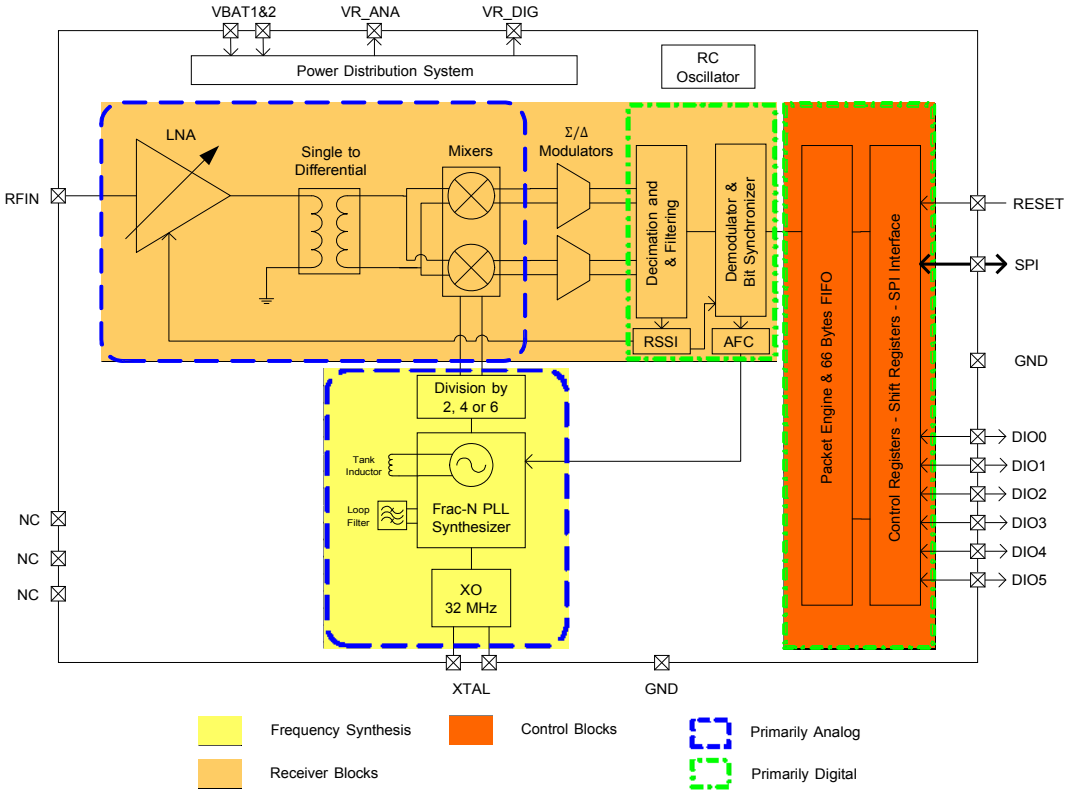

Figure 1. Block Diagram

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1.2. Pin Diagram

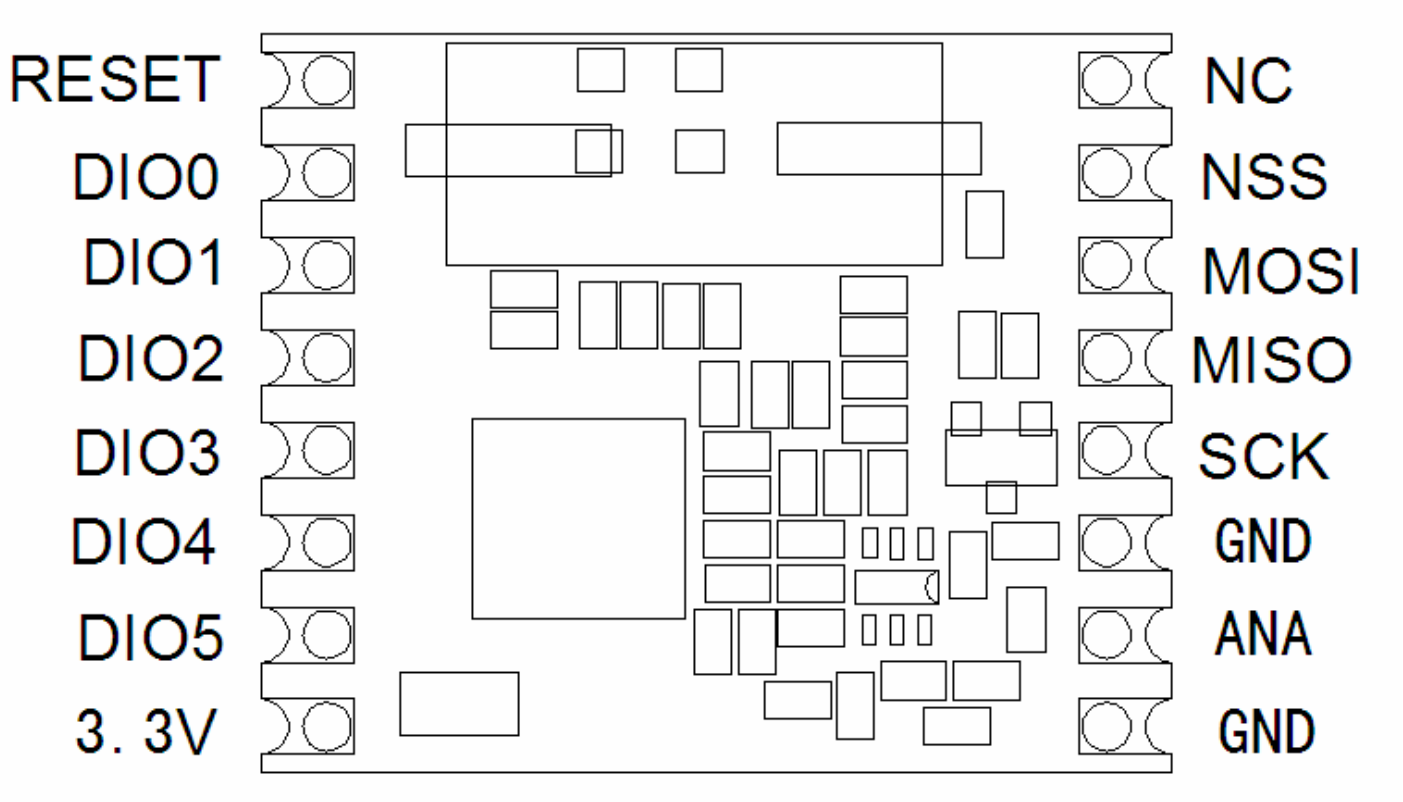

Figure 2. Pin Diagram

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1.3. Pin Description

Table 1 RFM65W Pinouts

Number	Name	Type	Description
1	RESET	I/O	Reset trigger input
2	DIO0	I/O	Digital I/O, software configured
3	DIO1	I/O	Digital I/O, software configured
4	DIO2	I/O	Digital I/O, software configured
5	DIO3	I/O	Digital I/O, software configured
6	DIO4	I/O	Digital I/O, software configured
7	DIO5	I/O	Digital I/O, software configured
8	3.3V	-	Supply voltage
9	GND	-	Ground
10	ANA		RF signal output/input.
11	GND	-	Ground
12	SCK	I	SPI Clock input
13	MISO	O	SPI Data output
14	MOSI	I	SPI Data input
15	NSS	I	SPI Chip select input
16	NC	_	Connect to GND

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2. Electrical Characteristics

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	+115	° C
Tj	Junction temperature	-	+125	° C
Pmr	RF Input Level	-	+6	dBm

2.3. Operating Range

Table 3 Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	1.8	3.6	V
Top	Operational temperature range	-40	+85	°C
Clop	Load capacitance on digital ports	-	25	pF
ML	RF Input Level	-	0	dBm

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2.4. Chip Specification

The tables below give the electrical specifications of the receiver under the following conditions: Supply voltage VBAT1= VBAT2=VDD=3.3 V, temperature = 25 °C, 2-level FSK modulation without pre-filtering, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified.

Note Unless otherwise specified, the performances in the other frequency bands are similar or better.

2.4.1. Power Consumption

Table 4 Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.1	1	uA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.2	-	uA
IDDST	Supply current in standby mode	Crystal oscillator enabled	-	1.25	1.5	mA
IDDFS	Supply current in synthesizer mode		-	9	-	mA
IDDR	Supply current in receive mode		-	16	-	mA

2.4.2. Frequency Synthesis

Table 5 Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer Frequency Range	315MHz Module 433MHz Module 868MHz Module 915MHz Module	290 424 862 890		340 510 890 1020	MHz MHz MHz MHz
FXOSC	Crystal oscillator frequency	For All Module	-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time		-	250	500	us
TS_FS	Frequency synthesizer wake-up time to PllLock signal	From Standby mode	-	80	150	us
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 80 80 80	- - - - - - -	us us us us us us us
FSTEP	Frequency synthesizer step	FSTEP = FXOSC/2^{19}	-	61.0	-	Hz
FRC	RC Oscillator frequency	After calibration	-	62.5	-	kHz
BRF	Bit rate, FSK	Programmable	1.2	-	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps

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2.4.3. Receiver

All receiver tests are performed with *RxBw* = 10 kHz (Single Side Bandwidth) as programmed in *RegRxBw*, receiving a PN15 sequence with a BER of 0.1% (Bit Synchronizer is enabled), unless otherwise specified. The LNA impedance is set to 200 Ohms, by setting bit *LnaZin* in *RegLna* to 1. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the nominal sensitivity level.

Table 6 Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s	- - -	-118 -114 -105	- - -	dBm dBm dBm
		FDA = 5 kHz, BR = 1.2 kb/s*	-	-120	-	dBm
RFS_O	OOK sensitivity, highest LNA gain	BR = 4.8 kb/s	-	-112	-109	dBm
CCR	Co-Channel Rejection		-13	-10	-	dB
ACR	Adjacent Channel Rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	- 37	42 42	- -	dB dB
BI	Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	-45 -40 -32	- - -	dBm dBm dBm
	Blocking Immunity Wanted signal at sensitivity +16dB	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	-36 -33 -25	- - -	dBm dBm dBm
AMR	AM Rejection , AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	-45 -40 -32	- - -	dBm dBm dBm
IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Lowest LNA gain Highest LNA gain	- -	+75 +35	- -	dBm dBm
IIP3	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Lowest LNA gain Highest LNA gain	- -23	+20 -18	- -	dBm dBm
BW_SSB	Single Side channel filter BW	Programmable	2.6	-	500	kHz
IMR_OOK	Image rejection in OOK mode	Wanted signal level = -106 dBm	27	30	-	dB
TS_RE	Receiver wake-up time, from PLL locked state to *RxReady*	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	- -	1.7 96	- -	ms us
TS_RE_AGC	Receiver wake-up time, from PLL locked state, AGC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	-	3.0 163		ms us
TS_RE_AGC &AFC	Receiver wake-up time, from PLL lock state, AGC and AFC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s		4.8 265		ms us

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TS_FEI	FEI sampling time	Receiver is ready	-	$4.T_{bit}$	-	-
TS_AFC	AFC Response Time	Receiver is ready	-	$4.T_{bit}$	-	-
TS_RSSI	RSSI Response Time	Receiver is ready	-	$2.T_{bit}$	-	-
DR_RSSI	RSSI Dynamic Range	AGC enabled Min Max	- -	-115 0	- -	dBm dBm

** Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver*

2.4.4. Digital Specification

Conditions: Temp = 25°C, VDD = 3.3V, FXOSC = 32 MHz, unless otherwise specified.

Table 7 Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VDD
V_{IL}	Digital input level low		-	-	0.2	VDD
V_{OH}	Digital output level high	Imax = 1 mA	0.9	-	-	VDD
V_{OL}	Digital output level low	Imax = -1 mA	-	-	0.1	VDD
F_{SCK}	SCK frequency		-	-	10	MHz
t_{ch}	SCK high time		50	-	-	ns
t_{cl}	SCK low time		50	-	-	ns
t_{rise}	SCK rise time		-	5	-	ns
t_{fall}	SCK fall time		-	5	-	ns
t_{setup}	MOSI setup time	from MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI hold time	from SCK rising edge to MOSI change	60	-	-	ns
t_{nsetup}	NSS setup time	from NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS hold time	from SCK falling edge to NSS rising edge, normal mode	30	-	-	ns
t_{nhigh}	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

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3. Chip Description

This section describes in depth the architecture of the RFM65W low-power, highly integrated receiver.

3.1. Power Supply Strategy

The RFM65W employs an advanced power supply scheme, which provides stable operating characteristics over the full temperature and voltage range of operation.

The RFM65W can be powered from any low-noise voltage source via pins VBAT1 and VBAT2. Decoupling capacitors should be connected, as suggested in the reference design on VR_DIG and VR_ANA pins to ensure a correct operation of the built-in voltage regulators.

3.2. Low Battery Detector

A low battery detector is also included allowing the generation of an interrupt signal in response to passing a programmable threshold adjustable through the register *RegLowBat*. The interrupt signal can be mapped to any of the DIO pins, through the programmation of *RegDioMapping*.

3.3. Frequency Synthesis

The LO generation on the RFM65W is based on a state-of-the-art fractional-N PLL. The PLL is fully integrated with automatic calibration.

3.3.1. Reference Oscillator

The crystal oscillator is the main timing reference of the RFM65W. It is used as a reference for the frequency synthesizer and as a clock for the digital processing.

The XO startup time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. When using the built-in sequencer, the RFM65W optimizes the startup time and automatically triggers the PLL when the XO signal is stable. To manually control the startup time, the user should either wait for TS_OSC max, or monitor the signal CLKOUT which will only be made available on the output buffer when a stable XO oscillation is achieved.

An external clock can be used to replace the crystal oscillator, for instance a tight tolerance TCXO. To do so, bit 4 at address 0x59 should be set to 1, and the external clock has to be provided on XTA. XTB should be left open. The peak-peak amplitude of the input signal must never exceed 1.8 V. Please consult your TCXO supplier for an appropriate value of decoupling capacitor, C_D.

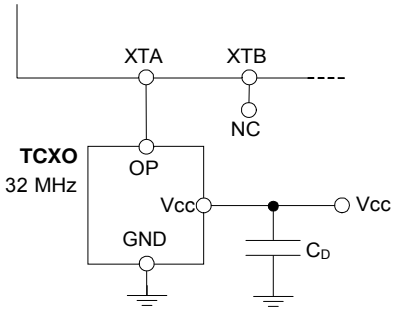

Figure 4. TCXO Connection

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3.3.2. CLKOUT Output

The reference frequency, or a fraction of it, can be provided on DIO5 pin by modifying bits *ClkOut* in *RegDioMapping2*. Two typical applications of the CLKOUT output include:

- To provide a clock output for a companion processor, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode except Sleep mode and is automatically enabled at power on reset.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note *to minimize the current consumption of the RFM65W, please ensure that the CLKOUT signal is disabled when not required.*

3.3.3. PLL Architecture

The frequency synthesizer generating the LO frequency for the receiver is a fractional-N sigma-delta PLL. The PLL incorporates a third order loop capable of fast auto-calibration, and it has a fast switching-time. The VCO and the loop filter are both fully integrated, removing the need for an external tight-tolerance, high-Q inductor in the VCO tank circuit.

3.3.3.1. VCO

The VCO runs at 2, 4 or 6 times the RF frequency (respectively in the 915, 434 and 315 MHz bands) to reduce any LO leakage in receiver mode, to improve the quadrature precision of the receiver.

The VCO calibration is fully automated. A coarse adjustment is carried out at power on reset, and a fine tuning is performed each time the RFM65W PLL is activated. Automatic calibration times are fully transparent to the end-user, as their processing time is included in the *TS_RE* specifications.

3.3.3.2. PLL Bandwidth

The bandwidth of the RFM65W Fractional-N PLL is wide enough to allow for very fast PLL lock times, enabling both short startup and fast hop times required for frequency agile applications.

3.3.3.3. Carrier Frequency and Resolution

The RFM65W PLL embeds a 19-bit sigma-delta modulator and its frequency resolution, constant over the whole frequency range, and is given by:

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The carrier frequency is programmed through *RegFrf*, split across addresses 0x07 to 0x09:

$$F_{RF} = F_{STEP} \times Frf(23,0)$$

Note *The Frf setting is split across 3 bytes. A change in the center frequency will only be taken into account when the least significant byte FrfLsb in RegFrfLsb is written.*

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3.3.4. Lock Time

PLL lock time *TS_FS* is a function of a number of technical factors, such as synthesized frequency, frequency step, etc. When using the built-in sequencer, the RFM65W optimizes the startup time and automatically starts the receiver when the PLL has locked. To manually control the startup time, the user should either wait for *TS_FS* max given in the specification, or monitor the signal PLL lock detect indicator, which is set when the PLL has is within its locking range.

When performing an AFC, which usually corrects very small frequency errors, the PLL response time is approximately:

$$T_{PLLAFC} = \frac{5}{PLLBW}$$

In a frequency hopping scheme, the timings *TS_HOP* given in the table of specifications give an order of magnitude for the expected lock times.

3.3.5. Lock Detect Indicator

A lock indication signal can be made available on some of the DIO pins, and is toggled high when the PLL reaches its locking range. Please refer to Table 17 and Table 18 to map this interrupt to the desired pins.

3.4. Receiver Description

The RFM65W features a digital receiver with the analog to digital conversion process being performed directly following the LNA-Mixers block. The zero-IF receiver is able to handle (G)FSK and (G)MSK modulation. ASK and OOK modulation is, however, demodulated by a low-IF architecture. All the filtering, demodulation, gain control, synchronization and packet handling is performed digitally, which allows a very wide range of bit rates and frequency deviations to be selected. The receiver is also capable of automatic gain calibration in order to improve precision on RSSI measurements.

3.4.1. Block Diagram

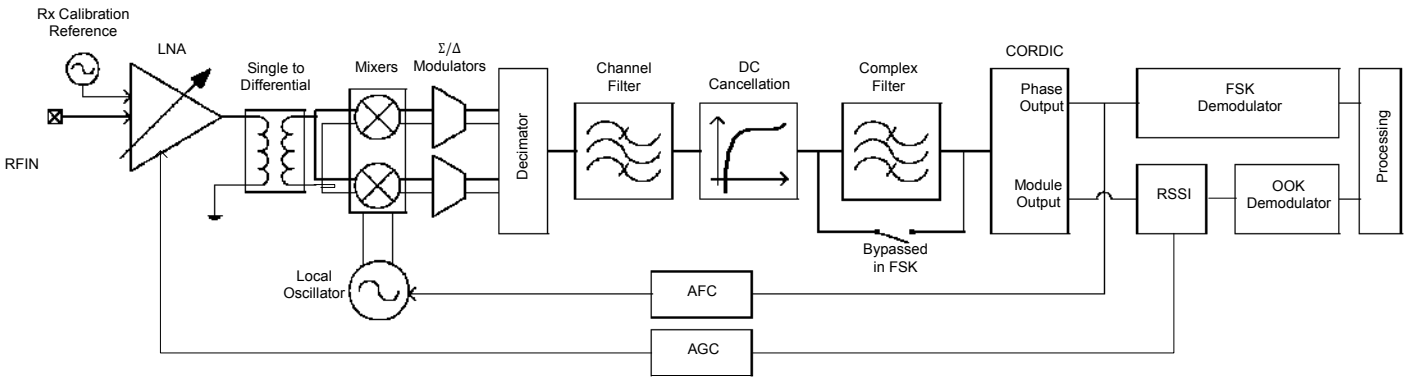

Figure 5. Receiver Block Diagram

The following sections give a brief description of each of the receiver blocks.

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3.4.2. LNA - Single to Differential Buffer

The LNA uses a common-gate topology, which allows for a flat characteristic over the whole frequency range. It is designed to have an input impedance of 50 Ohms or 200 Ohms (as selected with bit *LnaZin* in *RegLna)*, and the parasitic capacitance at the LNA input port is cancelled with the external RF choke. A single to differential buffer is implemented to improve the second order linearity of the receiver.

The LNA gain, including the single-to-differential buffer, is programmable over a 48 dB dynamic range, and control is either manual or automatic with the embedded AGC function.

Note *In the specific case where the LNA gain is manually set by the user, the receiver will not be able to properly handle FSK signals with a modulation index smaller than 2 at an input power greater than the 1dB compression point, tabulated in section 3.4.3.*

Table 8 LNA Gain Settings

LnaGainSelect	LNA Gain	Gain Setting
000	Any of the below, set by the AGC loop	-
001	Max gain	G1
010	Max gain - 6 dB	G2
011	Max gain - 12 dB	G3
100	Max gain - 24 dB	G4
101	Max gain - 36 dB	G5
110	Max gain - 48 dB	G6
111	Reserved	-

3.4.3. Automatic Gain Control

By default (*LnaGainSelect = 000*), the LNA gain is controlled by a digital AGC loop in order to obtain the optimal sensitivity/ linearity trade-off.

Regardless of the data transfer mode (Packet or Continuous), the following series of events takes place when the receiver is enabled:

- The receiver stays in WAIT mode, until *RssiValue* exceeds *RssiThreshold* for two consecutive samples. Its power consumption is the receiver power consumption.
- When this condition is satisfied, the receiver automatically selects the most suitable LNA gain, optimizing the sensitivity/ linearity trade-off.
- The programmed LNA gain, read-accessible with *LnaCurrentGain* in *RegLna*, is carried on for the whole duration of the packet, until one of the following conditions is fulfilled:
- Packet mode: if *AutoRxRestartOn = 0,* the LNA gain will remain the same for the reception of the following packet. If *AutoRxRestartOn = 1*, after the controller has emptied the FIFO the receiver will re-enter the WAIT mode described above, after a delay of *InterPacketRxDelay*, allowing for the distant transmitter to ramp down, hence avoiding a false RSSI detection. In both cases (AutoRxRestartOn=0 or AutoRxRestartOn=1), the receiver can also re-enter the WAIT mode by setting RestartRx bit to 1. The user can decide to do so, to manually launch a new AGC procedure.
- Continuous mode: upon reception of valid data, the user can decide to either leave the receiver enabled with the same LNA gain, or to restart the procedure, by setting *RestartRx* bit to 1, resuming the WAIT mode of the receiver, described above.

Notes *- the AGC procedure must be performed while receiving preamble in FSK mode*

- in OOK mode, the AGC will give better results if performed while receiving a constant "1" sequence

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The following figure illustrates the AGC behavior:*:*

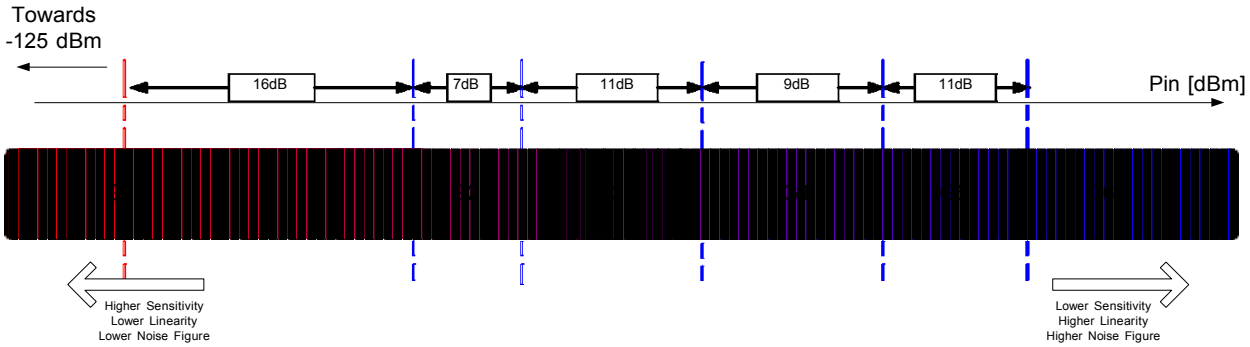

Figure 6. AGC Thresholds Settings

The following table summarizes the performance (typical figures) of the complete receiver:

Table 9 Receiver Performance Summary

Input Power Pin	**Gain Setting**	**Receiver Performance (typ)**			
		P_{-1dB} [dBm]	**NF [dB]**	**IIP3 [dBm]**	**IIP2 [dBm]**
Pin < AgcThresh1	G1	-37	7	-18	+35
AgcThresh1 < Pin < AgcThresh2	G2	-31	13	-15	+40
AgcThresh2 < Pin < AgcThresh3	G3	-26	18	-8	+48
AgcThresh3 < Pin < AgcThresh4	G4	-14	27	-1	+62
AgcThresh4 < Pin < AgcThresh5	G5	>-6	36	+13	+68
AgcThresh5 < Pin	G6	>0	44	+20	+75

3.4.3.1. RssiThreshold Setting

For correct operation of the AGC, *RssiThreshold* in *RegRssiThresh* must be set to the sensitivity of the receiver. The receiver will remain in WAIT mode until *RssiThreshold* is exceeded.

Note *When AFC is enabled and performed automatically at the receiver startup, the channel filter used by the receiver during the AFC and the AGC is RxBwAfc instead of the standard RxBw setting. This may impact the sensitivity of the receiver, and the setting of RssiThreshold accordingly*

3.4.3.2. AGC Reference

The AGC reference level is automatically computed in the RFM65W, according to:

AGC Reference [dBm] = -174 + NF + DemodSnr +10.log(2**RxBw***) + FadingMargin [dBm]**

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With:

- *NF* = 7dB : LNA's Noise Figure at maximum gain
- *DemodSnr* = 8 dB : SNR needed by the demodulator
- *RxBw* : Single sideband channel filter bandwidth
- *FadingMargin* = 5 dB : Fading margin

3.4.4. Continuous-Time DAGC

In addition to the automatic gain control described in section 3.4.3, the RFM65W is capable of continuously adjusting its gain in the digital domain, after the analog to digital conversion has occured. This feature, named DAGC, is fully transparent to the end user. The digital gain adjustment is repeated every 2 bits, and has the following benefits:

- Fully transparent to the end user
- Improves the fading margin of the receiver during the reception of a packet, even if the gain of the LNA is frozen
- Improves the receiver robustness in fast fading signal conditions, by quickly adjusting the receiver gain (every 2 bits)
- Works in Continuous, Packet, and unlimited length Packet modes

The DAGC is enabled by setting *RegTestDagc* to 0x10 for low modulation index systems (i.e. when *AfcLowBetaOn*=1, refer to section 3.4.17), and 0x30 for other systems. See section 9.5 for details. It is recommended to always enable the DAGC.

3.4.5. Quadrature Mixer - ADCs - Decimators

The mixer is inserted between output of the RF buffer stage and the input of the analog to digital converter (ADC) of the receiver section. This block is designed to translate the spectrum of the input RF signal to base-band, and offer both high IIP2 and IIP3 responses.

In the lower bands of operation (290 to 510 MHz), the multi-phase mixing architecture with weighted phases improves the rejection of the LO harmonics in receiver mode, hence increasing the receiver immunity to out-of-band interferers.

The I and Q digitalization is made by two 5^{th} order continuous-time Sigma-Delta Analog to Digital Converters (ADC). Their gain is not constant over temperature, but the whole receiver is calibrated before reception, so that this inaccuracy has no impact on the RSSI precision. The ADC output is one bit per channel. It needs to be decimated and filtered afterwards. This ADC can also be used for temperature measurement, please refer to section 3.4.18 for more details.

The decimators decrease the sample rate of the incoming signal in order to optimize the area and power consumption of the following receiver blocks.

3.4.6. Channel Filter

The role of the channel filter is to filter out the noise and interferers outside of the channel. Channel filtering on the RFM65W is implemented with a 16-tap Finite Impulse Response (FIR) filter, providing an outstanding Adjacent Channel Rejection performance, even for narrowband applications.

Note *to respect oversampling rules in the decimation chain of the receiver, the Bit Rate cannot be set at a higher value than 2 times the single-side receiver bandwidth (BitRate < 2 x RxBw)*

The single-side channel filter bandwidth *RxBw* is controlled by the parameters *RxBwMant* and *RxBwExp* in *RegRxBw:*

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- When FSK modulation is enabled:

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp+2}}$$

- When OOK modulation is enabled:

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp+3}}$$

The following channel filter bandwidths are accessible (oscillator is mandated at 32 MHz):

Table 10 Available RxBw Settings

RxBwMant **(binary/value)**	***RxBwExp*** **(decimal)**	***RxBw (kHz)***	
		FSK ***ModulationType=00***	**OOK** ***ModulationType=01***
10b / 24	7	2.6	1.3
01b / 20	7	3.1	1.6
00b / 16	7	3.9	2.0
10b / 24	6	5.2	2.6
01b / 20	6	6.3	3.1
00b / 16	6	7.8	3.9
10b / 24	5	10.4	5.2
01b / 20	5	12.5	6.3
00b / 16	5	15.6	7.8
10b / 24	4	20.8	10.4
01b / 20	4	25.0	12.5
00b / 16	4	31.3	15.6
10b / 24	3	41.7	20.8
01b / 20	3	50.0	25.0
00b / 16	3	62.5	31.3
10b / 24	2	83.3	41.7
01b / 20	2	100.0	50.0
00b / 16	2	125.0	62.5
10b / 24	1	166.7	83.3
01b / 20	1	200.0	100.0
00b / 16	1	250.0	125.0
10b / 24	0	333.3	166.7
01b / 20	0	400.0	200.0
00b / 16	0	500.0	250.0

3.4.7. DC Cancellation

DC cancellation is required in zero-IF architecture receivers to remove any DC offset generated through self-reception. It is built-in the RFM65W and its adjustable cutoff frequency *fc* is controlled in *RegRxBw*:

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$$fc = \frac{4 \times RxBw}{2\pi \times 2^{DccFreq+2}}$$

The default value of *DccFreq* cutoff frequency is typically 4% of the RxBw (channel filter BW). The cutoff frequency of the DCC can however be increased to slightly improve the sensitivity, under wider modulation conditions. It is advised to adjust the DCC setting while monitoring the receiver sensitivity.

3.4.8. Complex Filter - OOK

In OOK mode the RFM65W is modified to a low-IF architecture. The IF frequency is automatically set to half the single side bandwidth of the channel filter (F_{IF} = 0.5 x *RxBw*). The Local Oscillator is automatically offset by the IF in the OOK receiver. A complex filter is implemented on the chip to attenuate the resulting image frequency by typically 30 dB.

Note this filter is automatically bypassed when receiving FSK signals (ModulationType = 00 in *RegDataModul).*

3.4.9. RSSI

The RSSI block evaluates the amount of energy available within the receiver channel bandwidth. Its resolution is 0.5 dB, and it has a wide dynamic range to accommodate both small and large signal levels that may be present. Its acquisition time is very short, taking only 2 bit periods. The RSSI sampling must occur during the reception of preamble in FSK, and constant "1" reception in OOK.

Note - The receiver is capable of automatic gain calibration, in order to improve the precision of its RSSI measurements. This function injects a known RF signal at the LNA input, and calibrates the receiver gain accordingly. This calibration is automatically performed during the PLL start-up, making it a transparent process to the end-user.

- RssiValue can only be read when it exceeds RssiThreshold

3.4.10. Cordic

The Cordic task is to extract the phase and the amplitude of the modulation vector (I+j.Q). This information, still in the digital domain is used:

- Phase output: used by the FSK demodulator and the AFC blocks.
- Amplitude output: used by the RSSI block, for FSK demodulation, AGC and automatic gain calibration purposes.

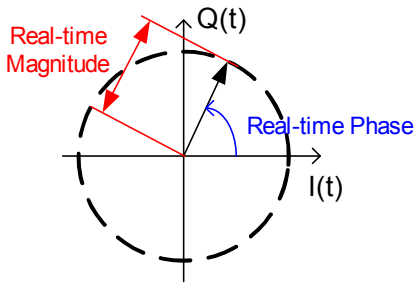

Figure 7. Cordic Extraction

3.4.11. Bit Rate Setting

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The Bit Rate (BR) is controlled by bits *BitRate* in *RegBitrate*:

$$BR = \frac{F_{XOSC}}{BitRate}$$

Amongst others, the following Bit Rates are accessible:

Table 11 Bit Rate Examples

Type	BitRate (15:8)	BitRate (7:0)	(G)FSK (G)MSK	OOK	Actual BR (b/s)
Classical modem baud rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps		38415.36
	0x01	0xA1	76.8 kbps		76738.60
	0x00	0xD0	153.6 kbps		153846.1
Classical modem baud rates (multiples of 0.9 kbps)	0x02	0x2C	57.6 kbps		57553.95
	0x01	0x16	115.2 kbps		115107.9
Round bit rates (multiples of 12.5, 25 and 50 kbps)	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x02	0x80	50 kbps		50000.00
	0x01	0x40	100 kbps		100000.0
	0x00	0xD5	150 kbps		150234.7
	0x00	0xA0	200 kbps		200000.0
	0x00	0x80	250 kbps		250000.0
	0x00	0x6B	300 kbps		299065.4
Watch Xtal frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

3.4.12. FSK Demodulator

The FSK demodulator of the RFM65W is designed to demodulate FSK, GFSK, MSK and GMSK modulated signals. It is most efficient when the modulation index of the signal is greater than 0.5 and below 10:

$$0.5 \leq \beta = \frac{2 \times F_{DEV}}{BR} \leq 10$$

The output of the FSK demodulator can be fed to the Bit Synchronizer (described in section 3.4.14), to provide the companion processor with a synchronous data stream in Continuous mode.

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3.4.13. OOK Demodulator

The OOK demodulator performs a comparison of the RSSI output and a threshold value. Three different threshold modes are available, configured through bits *OokThreshType* in *RegOokPeak*.

The recommended mode of operation is the "Peak" threshold mode, illustrated in Figure 8:

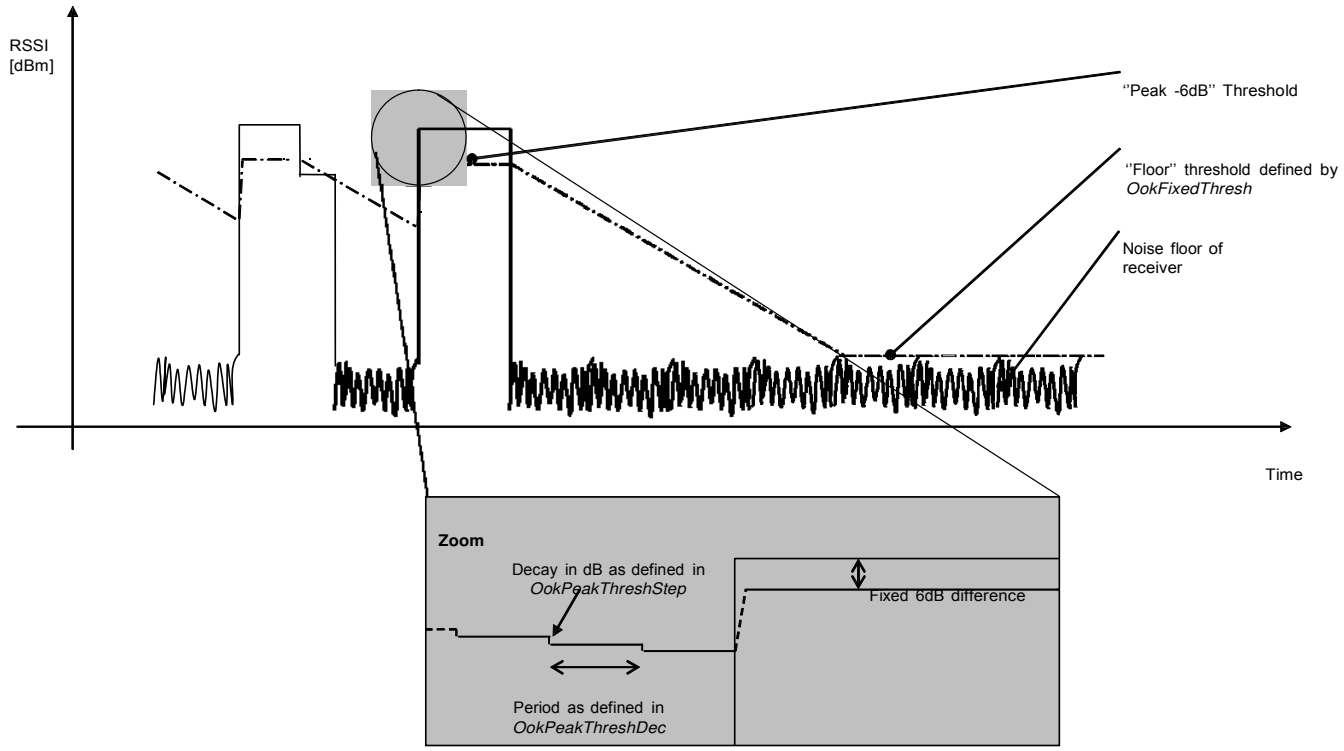

Figure 8. OOK Peak Demodulator Description

In peak threshold mode the comparison threshold level is the peak value of the RSSI, reduced by 6dB. In the absence of an input signal, or during the reception of a logical "0", the acquired peak value is decremented by one *OokPeakThreshStep* every *OokPeakThreshDec* period.

When the RSSI output is null for a long time (for instance after a long string of "0" received, or if no transmitter is present), the peak threshold level will continue falling until it reaches the "Floor Threshold", programmed in *OokFixedThresh*.

The default settings of the OOK demodulator lead to the performance stated in the electrical specification. However, in applications in which sudden signal drops are awaited during a reception, the three parameters should be optimized accordingly.

3.4.13.1. Optimizing the Floor Threshold

OokFixedThresh determines the sensitivity of the OOK receiver, as it sets the comparison threshold for weak input signals (i.e. those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

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Note that the noise floor of the receiver at the demodulator input depends on:

- The noise figure of the receiver.
- The gain of the receive chain from antenna to base band.
- The matching - including SAW filter if any.
- The bandwidth of the channel filters.

It is therefore important to note that the setting of *OokFixedThresh* will be application dependant. The following procedure is recommended to optimize *OokFixedThresh*.

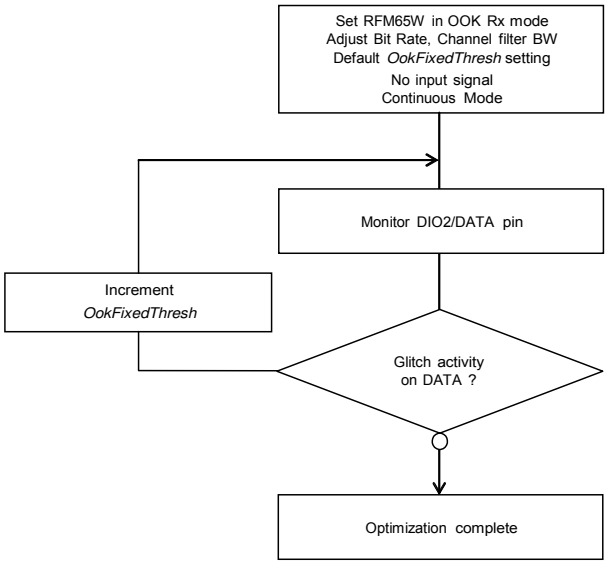

Figure 9. Floor Threshold Optimization

The new floor threshold value found during this test should be used for OOK reception with those receiver settings.

3.4.13.2. Optimizing OOK Demodulator for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications where the expected signal drop can be estimated, the following OOK demodulator parameters *OokPeakThreshStep* and *OokPeakThreshDec* can be optimized as described below for a given number of threshold decrements per bit. Refer to *RegOokPeak* to access those settings.

3.4.13.3. Alternative OOK Demodulator Threshold Modes

In addition to the Peak OOK threshold mode, the user can alternatively select two other types of threshold detectors:

- Fixed Threshold: The value is selected through *OokFixedThresh*
- Average Threshold: Data supplied by the RSSI block is averaged, and this operation mode should only be used with DC-free encoded data.

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