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rfRXD0420/0920

UHF ASK/FSK/FM Receiver

Features:

- Low cost single conversion superheterodyne receiver architecture
- Compatible with rfPIC™ and rfHCS series of RF transmitters
- Easy interface to PICmicro® microcontroller (MCU) and KEELOQ® decoders
- VCO phase locked to quartz crystal reference:
  - Narrow receiver bandwidth
  - Maximizes range and interference immunity
- Selectable LNA gain control for improved dynamic range
- Selectable IF bandwidth via external ceramic IF filter
- Received Signal Strength Indicator (RSSI) for signal strength indication (FSK, FM) and ASK demodulation
- FSK/FM quadrature (phase coincidence) detector demodulator
- 32-Lead LQFP package

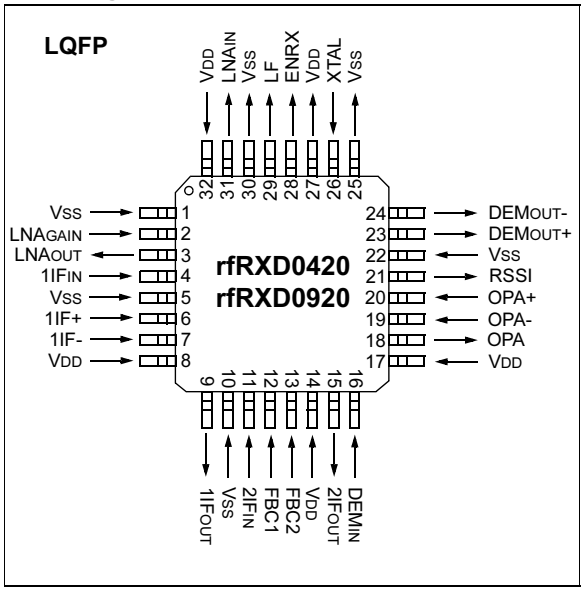
UHF ASK/FSK Receiver:

- Single frequency receiver set by crystal frequency
- Receive frequency range:

Device	Frequency Range
rfRXD0420	300 MHz to 450 MHz
rfRXD0920	800 MHz to 930 MHz

- Maximum data rate:
  - ASK: 80 Kbps NRZ
  - FSK: 40 Kbps NRZ
- IF frequency range: 455 kHz to 21.4 MHz
- RSSI range: 70 dB
- Frequency deviation range: ±5 kHz to ±120 kHz
- Maximum FM modulation frequency: 15 kHz

Pin Diagram:



Applications:

- Wireless remote command and control
- Wireless security systems
- Remote Keyless Entry (RKE)
- Low power telemetry
- Low power FM receiver
- Home automation
- Remote sensing

Bi-CMOS Technology:

- Wide operating voltage range
- Low current consumption in Active and Standby modes
  - rfRXD0420
    - 8.2 mA (typical, LNA High Gain mode)
    - <100 nA standby
  - rfRXD0920
    - 9.2 mA (typical, LNA High Gain mode)
    - <100 nA standby
- Wide temperature range:
  - Industrial: -40°C to +85°C

1.0 DEVICE OVERVIEW

The rfRXD0420/0920 are low cost, compact single frequency short-range radio receivers requiring only a minimum number of external components for a complete receiver system. The rfRXD0420 covers the receive frequency range of 300 MHz to 450 MHz and the rfRXD0920 covers 800 MHz to 930 MHz. The rfRXD0420 and rfRXD0920 share a common architecture. They can be configured for Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), or FM modulation. The rfRXD0420/0920 are compatible with rfPIC™ and rfHCS series of RF transmitters.

- High frequency stability over temperature and power supply variations
- Low spurious signal emission
- High large-signal handling capability with selectable LNA gain control for improved dynamic range
- Selectable IF bandwidth via external low cost ceramic IF filter. The IF Frequency range is selectable between 455 kHz to 21.4 MHz. This facilitates the use of readily available low cost 10.7 MHz ceramic IF filters in a variety of bandwidths.
- ASK or FSK for digital data reception
- FM modulation for analog signal reception
- FSK/FM demodulation using quadrature detector (phase coincidence detector)
- Received Signal Strength Indication (RSSI) for signal strength indication and ASK detection
- Wide supply voltage range
- Low active current consumption
- Very low standby current

The rfRXD0420/0920 is a single conversion superheterodyne architecture. A block diagram is illustrated in Figure 1-1. The rfRXD0420/0920 consists of:

- Low-noise amplifier (LNA) - Gain selectable
- Mixer for down-conversion of the RF signal to the Intermediate Frequency (IF) followed by an IF preamplifier
- Fully integrated Phase-Locked Loop (PLL) frequency synthesizer for generation of the Local Oscillator (LO) signal. The frequency synthesizer consists of:
  - Crystal oscillator
  - Phase-frequency detector and charge pump
  - High-frequency Voltage Controlled Oscillator (VCO)
  - Fixed feedback divider
    - rfRXD0420 = divide by 16
    - rfRXD0920 = divide by 32
- IF limiting amplifier to amplify and limit the IF signal and for Received Signal Strength Indication (RSSI) generation
- Demodulator (DEMOD) section consists of a phase detector (MIXER2) and amplifier creating a quadrature detector (also known as a phase coincidence detector) to demodulate the IF signal in FSK and FM modulation applications
- Operational amplifier (OPA) that can be configured as a comparator for ASK or FSK data decision or as a filter for FM modulation.
- Bias circuitry for bandgap biasing and circuit shutdown

FIGURE 1-1: rfRXD0420/0920 BLOCK DIAGRAM

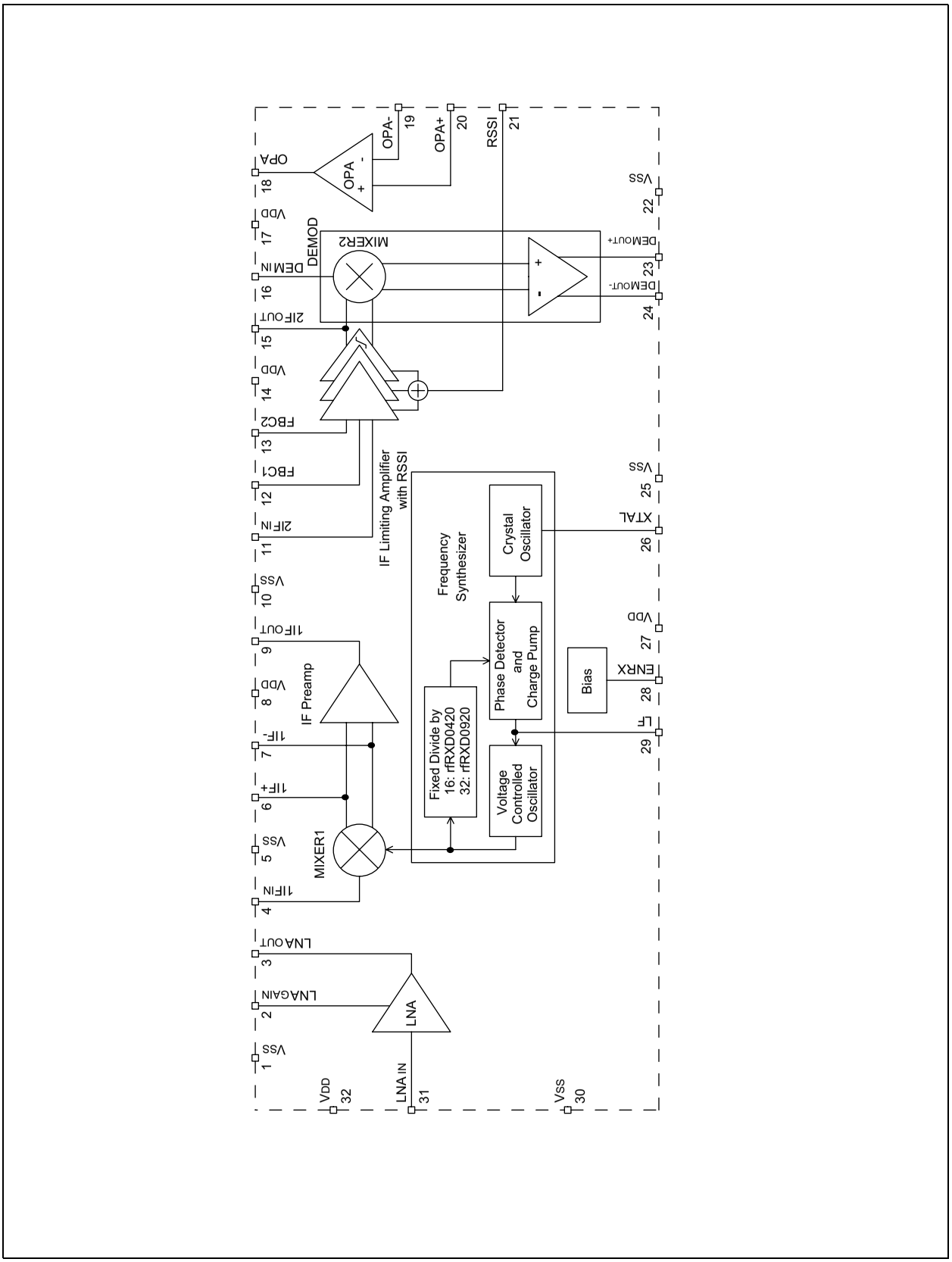


TABLE 1-1: rfRXD0420/0920 PINOUT I/O DESCRIPTION

Pin Name	Pin Number	Pin Type	Buffer Type	Description
LNAGAIN	2	I	CMOS	LNA gain control (with hysteresis)
LNAOUT	3	O	Analog	LNA output (open collector)
1IFIN	4	I	Analog	1st IF stage input
1IF+	6	--	Analog	MIXER1 bias (open collector)
1IF-	7	--	Analog	MIXER1 bias (open collector)
1IFOUT	9	O	Analog	1st IF stage output
2IFIN	11	I	Analog	2nd IF stage input
FBC1	12	--	Analog	Limiter IF Amplifier external feedback capacitor
FBC2	13	--	Analog	Limiter IF Amplifier external feedback capacitor
2IFOUT	15	O	Analog	2nd IF stage output
DEMIN	16	I	Analog	Demodulator input
OPA	18	O	Analog	Operational amplifier output
OPA-	19	I	Analog	Operational amplifier input (negative)
OPA+	20	I	Analog	Operational amplifier input (positive)
RSSI	21	O	Analog	Received signal strength indicator output
DEMOUT+	23	O	Analog	Demodulator output (positive)
DEMOUT-	24	O	Analog	Demodulator output (negative)
XTAL	26	I	Analog	Crystal oscillator input
ENRX	28	I	CMOS	Receiver enable input
LF	29	I	Analog	External loop filter connection. Common node of charge pump output and VCO tuning input.
LNAIN	31	I	Analog	LNA input
VDD	8, 14, 17, 27, 32	P		Positive supply
VSS	1, 5, 10, 25, 30	P		Ground reference

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, CMOS = CMOS compatible input or output

2.0 CIRCUIT DESCRIPTION

This section gives a circuit description of the internal circuitry of the rfRXD0420/0920 receiver. External connections and components are given in the APPLICATION CIRCUITS section.

2.1 Bias Circuitry

Bias circuitry provides bandgap biasing and circuit shutdown capabilities. The ENRX (Pin 28) modes are summarized in Table 2-1. The ENRX pin is a CMOS compatible input and is internally pulled down to Vss.

TABLE 2-1: BIAS CIRCUITRY CONTROL

ENRX(1)	Description
0	Standby mode
1	Receiver enabled
Note 1: ENRX has internal pull-down to Vss	

2.2 Frequency Synthesizer

The Phase-locked Loop (PLL) frequency synthesizer generates the Local Oscillator (LO) signal. It consists of:

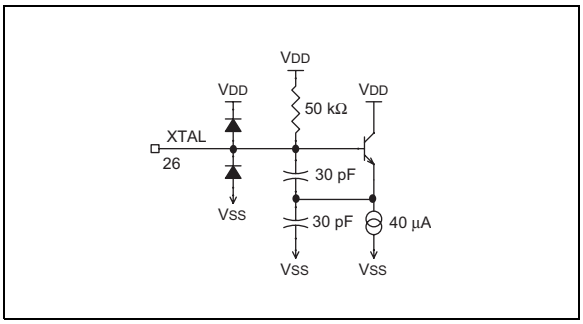
- Crystal oscillator
- Phase-frequency detector and charge pump
- Voltage Controlled Oscillator (VCO)
- Fixed feedback divider:
  - rfRXD0420 = divide by 16
  - rfRXD0920 = divide by 32

2.2.1 CRYSTAL OSCILLATOR

The internal crystal oscillator is a Colpitts type oscillator. It provides the reference frequency to the PLL. A crystal is normally connected to the XTAL (Pin 26) and ground. The internal capacitance of the crystal oscillator is 15 pF. Alternatively, a signal can be injected into the XTAL pin from a signal source. The signal should be AC coupled via a series capacitor at a level of approximately 600 mV_{pp}.

The XTAL pin is illustrated in Figure 2-1.

FIGURE 2-1: BLOCK DIAGRAM OF XTAL PIN



The PLL consists of a phase-frequency detector, charge pump, voltage-controlled oscillator (VCO), and fixed divide-by-16 (rfRXD0420) or divide-by-32 (rfRXD0920) divider. The rfRXD0420/0920 employs a charge pump PLL that offers many advantages over the classical voltage phase detector PLL: infinite pull-in range and zero steady state phase error. The charge pump PLL allows the use of passive loop filters that are lower cost and minimize noise. Charge pump PLLs have reduced flicker noise thus limiting phase noise.

An external loop filter is connected to pin LF (Pin 29). The loop filter controls the dynamic behavior of the PLL, primarily lock time and spur levels. The application determines the loop filter requirements.

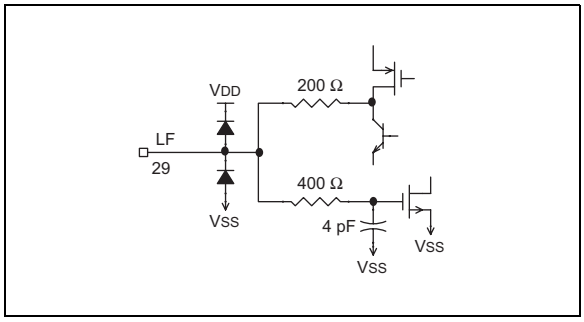
The VCO gain for the rfRXD0420/0920 receivers are listed in Table 2-2.

TABLE 2-2: PLL PARAMETERS

Device	Kvco(1)	Icp(1)	Divider
rfRXD0420	250 MHz/V at 433 MHz	60 μA	16
rfRXD0920	300 MHz/V at 868 MHz	60 μA	32
Note 1: Typical value			

The LF pin is illustrated in Figure 2-2.

FIGURE 2-2: BLOCK DIAGRAM OF LOOP FILTER PIN



2.3 Low Noise Amplifier

The Low-Noise Amplifier (LNA) is a high-gain amplifier whose primary purpose is to lower the overall noise figure of the entire receiver thus enhancing the receiver sensitivity. The LNA is an open-collector cascode design. The benefits of a cascode design are:

- high gain with low noise
- high-frequency
- wide bandwidth
- low effective input capacitance with stable input impedance
- high output resistance
- high reverse isolation that provides improved stability and reduces LO leakage

Approximate LNA noise figures are listed in Table 2-3.

TABLE 2-3: LNA NOISE FIGURES

Device	Noise Figure(1)
rfRXD0420	TBD
rfRXD0920	TBD
Note 1: Approximate value	

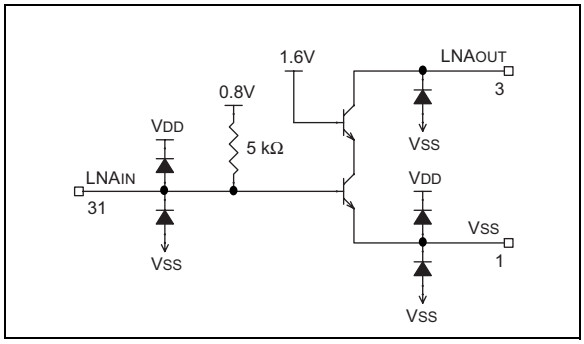
LNAIN (Pin 31) has an input impedance of approximately 26 Ω || 2 pF single-ended.

LNAOUT (Pin 3) has an open-collector output and is pulled up to VDD via a tuned circuit.

Important: To ensure LNA stability the VSS pin (Pin 1) must be connected to a low impedance ground.

The LNA pins are illustrated in Figure 2-3.

FIGURE 2-3: BLOCK DIAGRAM OF LNA PINS



The gain of the LNA can be selected between High and Low Gain modes by the LNAGAIN pin (Pin 2). LNAGAIN is a CMOS input with hysteresis. Table 2-4 summarizes the voltage levels and modes for LNA gain.

In the High Gain mode the LNA operates normally. In Low Gain mode the gain of the LNA is reduced approximately 25 dB, reduces total supply current, and increases maximum input signal levels (see Electrical Characteristics section for values).

TABLE 2-4: LNA GAIN CONTROL

LNAGAIN	Description
< 0.8 V	High Gain mode
> 1.4 V	Low Gain mode

2.4 MIXER1 and IF Preamp

MIXER1 performs down-conversion of the RF signal to the Intermediate Frequency (IF) and is followed by an IF preamplifier.

1IFIN (Pin 4) has an approximately 33 Ω single-ended input impedance. The 1IFIN pin is illustrated in Figure 2-4.

The 1IF+ (Pin 6) and 1IF- (Pin 7) are bias connections to the MIXER1 balanced collectors. Both pins are open-collector outputs and are individually pulled up to VDD by a load resistor. The MIXER1 bias pins are illustrated in Figure 2-5.

1IFOUT (Pin 9) has an approximately 330 Ω single-ended output impedance. The 330 Ω impedance provides a direct match to low cost ceramic IF filters. The 1IFOUT pins is illustrated in Figure 2-6.

FIGURE 2-4: BLOCK DIAGRAM OF MIXER1 PIN

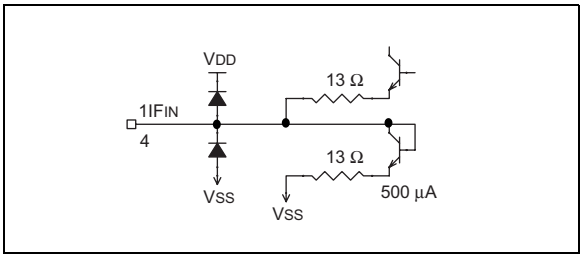


FIGURE 2-5: BLOCK DIAGRAM OF MIXER1 BIAS PINS

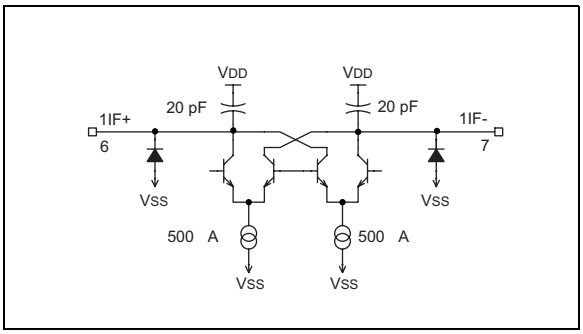
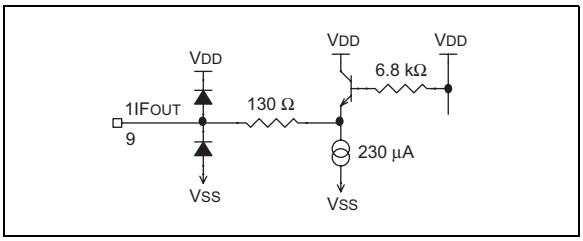


FIGURE 2-6: BLOCK DIAGRAM OF IF PREAMP PIN



2.5 IF Limiting Amplifier with RSSI

The IF Limiting Amplifier amplifies and limits the IF signal at the 2IFIN pin (Pin 11). It also generates the Received Signal Strength Indicator (RSSI) signal (Pin 21).

2.5.1 IF LIMITING AMPLIFIER

Magnitude control circuitry is used in the last stage of the receiver to keep the signal constant for demodulation. It can consist of a limiting or Automatic Gain Control (AGC) amplifier. A limiting amplifier is

employed in this design because it can handle a larger dynamic range while consuming less power with simple circuitry than AGC circuitry.

The internal resistance of the 2IFIN pin is approximately 2.2 kΩ. In order to terminate ceramic IF filters whose output impedance is 330 Ω, a 390 Ω resistor can be paralleled to the 2IFIN and FBC2 pins.

FBC1 (Pin 12) and FBC2 (Pin 13) are connected to external feedback capacitors.

The IF Limiting Amplifier pins are illustrated in Figures 2-7 and 2-8.

FIGURE 2-7: BLOCK DIAGRAM OF IF LIMITING AMPLIFIER INPUT PINS

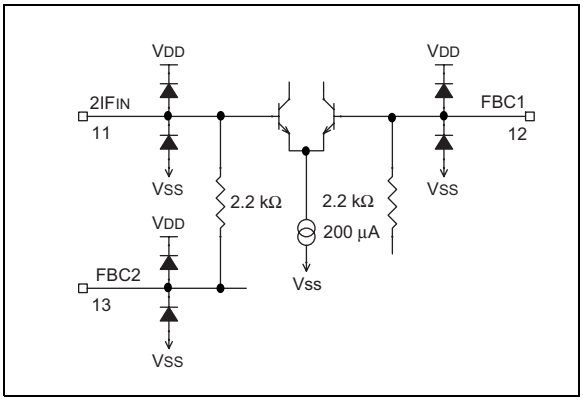
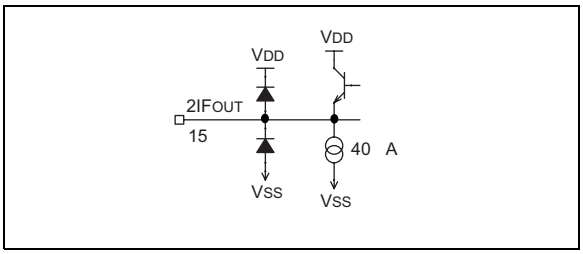


FIGURE 2-8: BLOCK DIAGRAM OF IF LIMITING AMPLIFIER OUTPUT PIN



2.5.2 RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

The RSSI signal is proportional to the log of the signal at 2IFIN. The 2IFIN input RSSI range is approximately 40 µV to 160 mV. The slope of the RSSI output is approximately 26 mV/dB of RF signal.

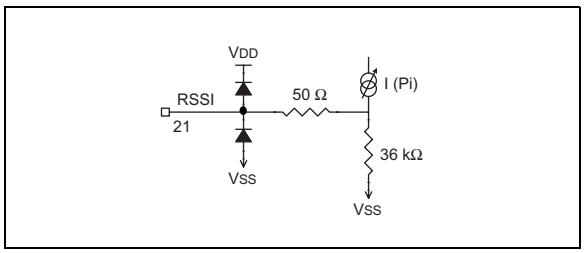
The RSSI output has an internal 36 kΩ resister to Vss fed by a current source. This resistor converts the RSSI current to voltage.

For Amplitude Shift Keying (ASK) demodulation, RSSI is compared to a reference voltage (static or dynamic). Post detector filtering is easily implemented by connecting a capacitor to ground from the RSSI pin effectively creating an RC filter with the internal 36 kΩ resistor.

For FSK and FM demodulation, the RSSI represents the received signal strength of the incoming RF signal.

The RSSI pin is illustrated in Figure 2-9.

FIGURE 2-9: BLOCK DIAGRAM OF RSSI PIN



2.6 Demodulator

The demodulator (DEMOD) section consists of a phase detector (MIXER2) and amplifier creating a quadrature detector (also known as a phase coincidence detector) to demodulate the IF signal in FSK and FM modulation applications. The quadrature detector provides all the IF functions required for FSK and FM demodulation with only a few external parts.

The in-phase signal comes directly from the output of the IF limiting amplifier to MIXER2. The quadrature signal is created by an external tuned circuit from the output of the IF limiting amplifier (2IFOUT, Pin 15) AC-coupled to the MIXER2 DEMIN (Pin 16) input. The input impedance of the DEMIN pin is approximately 47 kΩ.

The external tuned circuit can be constructed from simple inductor-capacitor (LC) components but will require one of the elements to be tunable. A no-tune solution can be constructed with a ceramic discriminator.

The output voltage of the DEMOD amplifier (DEMout+ and DEMout-, Pins 23 and 24) depends on the peak deviation of the FSK or FM signal and the Q of the external tuned circuit. DEMout+ and DEMout- are high impedance outputs with only a 20 µA current capability.

The Demodulator pins are illustrated in Figures 2-10 and 2-11.

FIGURE 2-10: BLOCK DIAGRAM OF DEMODULATOR INPUT PIN

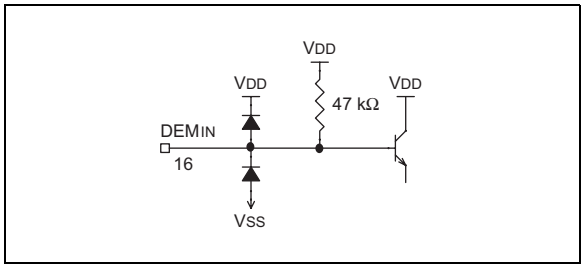
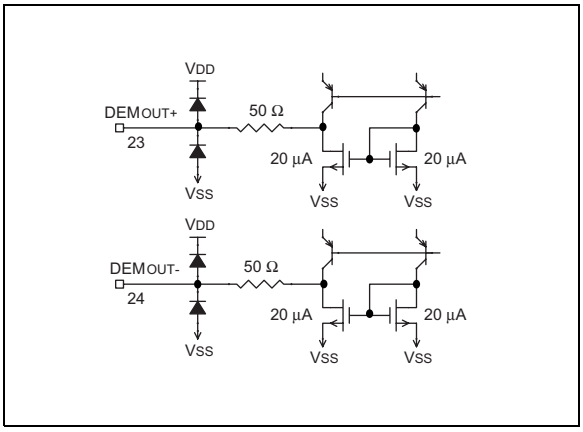


FIGURE 2-11: BLOCK DIAGRAM OF DEMODULATOR OUTPTUT PINS



2.7 Operational Amplifier

The internal operational amplifier (OPA) can be configured as a comparator for ASK or FSK or as a filter for FM modulation applications.

The Op Amp pins are illustrated in Figures 2-12 and 2-13.

FIGURE 2-12: BLOCK DIAGRAM OF OP AMP INPUT PINS

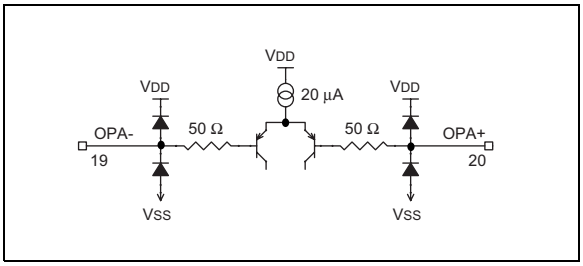
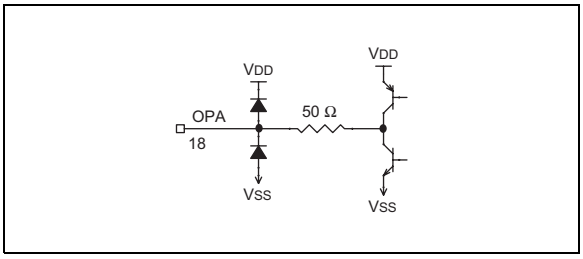


FIGURE 2-13: BLOCK DIAGRAM OF OP AMP OUTPUT PIN



3.0 APPLICATION CIRCUITS

This section provides general information on application circuits for the rfRXD0420/0920 receiver. The following connections and external components provide starting points for designs and list the minimum circuitry recommended for general purpose applications.

Performance of the radio system (transmitter and receiver) is affected by component selection and the environment in which it operates. Each system design has its own unique requirements. Specifications for a particular design requires careful analysis of the application and compromises for a practical implementation.

3.1 General

This subsection lists connections and components that are common between applications. The following subsections give specific circuit connections and components for ASK, FSK and FM applications.

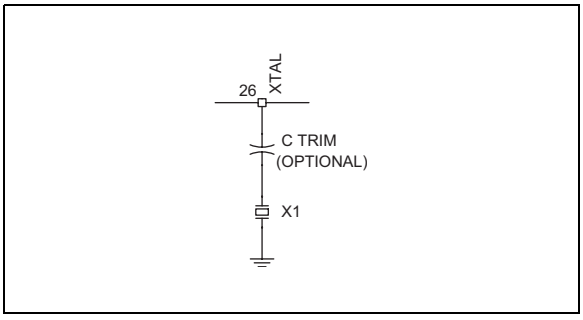
3.1.1 BYPASS CAPACITORS

Bypass capacitors should be placed as physically close as possible to V_{DD} pins 8, 14, 17, 27 and 32 respectively. Additional bypassing and board level low-pass filtering of the power supply may be required depending on the application.

3.1.2 FREQUENCY PLANNING

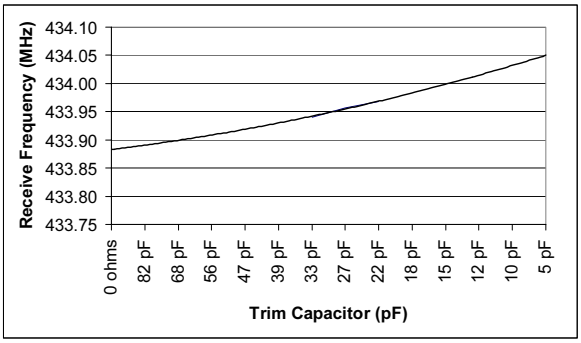
The rfRXD0420/0920 receivers are single-conversion superheterodyne architecture with a single IF frequency. The receive frequency is set by the crystal frequency (f_{XTAL}) and intermediate frequency (f_{if}). For a majority of applications an external crystal is connected to XTAL (Pin 26). Figure 3-1 illustrates an example circuit with an optional trim capacitor.

FIGURE 3-1: XTAL EXAMPLE CIRCUIT WITH OPTIONAL TRIM CAPACITOR



The crystal load capacitance should be specified to include the internal load capacitance of the XTAL pin of 15 pF plus PCB stray capacitance (approximately 2 to 3 pF). A trim capacitor can be used to trim the crystal on frequency within the limitations of the crystal's trim sensitivity and pullability. Figure 3-2 illustrates the effect the trim capacitor has on the receive frequency for the rfRXD0420 at 433.92 MHz. Keep in mind that this graph represents one example circuit and the actual results depends on the crystal and PCB layout.

FIGURE 3-2: RECEIVE FREQUENCY VS. TRIM CAPACITANCE



Note that a 0 Ω resistor, in the lower left of the graph, represents an infinite capacitance. This will be the lowest frequency obtainable for the crystal and PCB combination.

Calculation of the crystal frequency requires knowledge of the receive frequency (f_{rf}) and intermediate frequency (f_{if}). Figure 3-3 is a worksheet to assist the designer in calculating the crystal frequency. Table 3-1 lists crystal frequencies for popular receive frequencies. Table 3-2 lists crystal parameters required for ordering crystals. For background information on crystal selection see Application Note AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices.

TABLE 3-1: CRYSTAL FREQUENCIES FOR POPULAR RECEIVE FREQUENCIES

Receive Frequency	Crystal Frequency
rfRXD0420	
315 MHz	20.35625 MHz (2)
433.92 MHz	26.45125 MHz (1)
rfRXD0920	
868.3 MHz	26.8 MHz (1)
915 MHz	28.259375 MHz (1)
(1) Low-side injection (2) High-side injection	

TABLE 3-2: CRYSTAL PARAMETERS

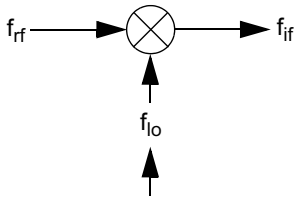
Parameter	Value
Frequency:	(see Figure 3-1)
Mode:	Fundamental
Load Capacitance:	15-20 pF
ESR:	60 Ω Maximum
These values are for design guidance only.	

FIGURE 3-3: FREQUENCY PLANNING WORKSHEET

Step 1: Identify receive (f_{rf}) and IF frequency (f_{if}).

f_{rf} = _____

f_{if} = _____



Step 2: Calculate crystal frequencies for high- and low-side injection:

High-side Injection

$$f_{XTAL\text{-}HIGH} = \frac{(f_{rf} + f_{if})}{\text{PLL divide ratio}} = \frac{(\_\_\_\_\_ + \_\_\_\_\_)}{\begin{matrix}\text{16 if rfRXD0420}\\ \text{32 if rfRXD0920}\end{matrix}} = \_\_\_\_\_$$

Low-side Injection

$$f_{XTAL\text{-}LOW} = \frac{(f_{rf} - f_{if})}{\text{PLL divide ratio}} = \frac{(\_\_\_\_\_ - \_\_\_\_\_)}{\begin{matrix}\text{16 if rfRXD0420}\\ \text{32 if rfRXD0920}\end{matrix}} = \_\_\_\_\_$$

Step 3: Calculate Local Oscillator (LO) frequencies (f_{lo}) using $f_{XTAL\text{-}HIGH}$ and $f_{XTAL\text{-}LOW}$:

High-side Injection

$f_{lo\text{-}HIGH}$ = $f_{XTAL\text{-}HIGH}$ x PLL Divide Ratio = _____ x $\begin{matrix}\text{16 if rfRXD0420}\\ \text{32 if rfRXD0920}\end{matrix}$ = _____

Low-side Injection

$f_{lo\text{-}LOW}$ = $f_{XTAL\text{-}LOW}$ x PLL Divide Ratio = _____ x $\begin{matrix}\text{16 if rfRXD0420}\\ \text{32 if rfRXD0920}\end{matrix}$ = _____

Step 4: Select high-side injection ($f_{lo\text{-}HIGH}$) or low-side injection ($f_{lo\text{-}LOW}$) that corresponds to the LO frequency that is between the ranges of:

Device	LO Frequency Range
rfRXD0420	300 to 430 MHz
rfRXD0920	800 to 915 MHz

Step 5: From the chosen injection mode in Step 4, write the selected crystal frequency (f_{XTAL}) and circle injection mode.

(circle one)

f_{XTAL} = _____ High-side Injection Low-side Injection

Step 6: Calculate image frequency ($f_{rf\text{-}image}$) for the Injection mode chosen:

if High-side Injection

$f_{rf\text{-}image}$ = f_{rf} + (2 x f_{if}) = _____ + (2 x _____) = _____

if Low-side Injection

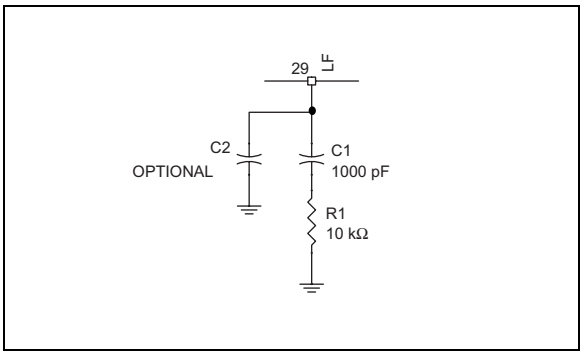
$f_{rf\text{-}image}$ = f_{rf} - (2 x f_{if}) = _____ - (2 x _____) = _____

Note: Image frequency should be sufficiently filtered by the preselector for the application.

3.1.3 PLL LOOP FILTER

An external PLL loop filter is connected to pin LF (Pin 29). The loop filter controls the dynamic behavior of the PLL, primarily lock time and spur levels. Generally, the PLL lock time is a small fraction of the overall receiver start-up time (see Electrical Characteristics Section). The crystal oscillator is the largest contributor to start-up time. Thus, for the majority of applications, design loop filter values for a wide loop bandwidth to suppress noise. Figure 3-4 illustrates an example filter circuit for a wide frequency range suitable for a majority of applications.

FIGURE 3-4: PLL LOOP FILTER EXAMPLE CIRCUIT



3.1.4 PRESELECTOR

Receiver performance is heavily influenced by the preselector (also known as the front-end filter). The purpose of the preselector is to filter unwanted signals and noise from entering the receiver.

The most important unwanted signal is the image frequency ($f_{rf\text{-}image}$). Pay particular attention to the image frequency calculated in Figure 3-3 as this will be the frequency that needs to be filtered out by the preselector.

The preselector can be designed using a simple LC filter or a Surface Acoustic Wave (SAW) filter. A simple LC filter provides a low cost solution but will have the least effect filtering the image frequency. A SAW filter can effectively filter the image frequency with a minimum of 40 dB attenuation.

The SAW filter has the added advantage of filtering wide-band noise and improving the signal-to-noise ratio (SNR) of the receiver.

SAW filters require impedance matching. Refer to the manufacturers' data sheet and application notes for SAW filter pinouts, specified impedances and recommended matching circuits. Figure 3-5 shows a SAW filter example circuit.

A secondary purpose of the preselector is to provide impedance matching between the antenna and LNAIN (Pin 31).

3.1.5 ANTENNA

Receiver performance and device packaging influence antenna selection. There are many third-party antennas to choose from. Third-party antennas typically have an impedance of 50 Ω. The preselector components should be chosen to match the impedance of the antenna to the LNAIN (Pin 31) impedance of 26 Ω || 2 pF.

The designer can chose to use a simple wire antenna. The length of the wire should be one-quarter the wavelength (λ) of the receive frequency. For example, the wavelength of 433.92 MHz is:

$\lambda = c / f_{rf}$ where $c = 3 \times 10^8$ m/s

$\lambda = 3 \times 10^8$ m/s / 433.92×10^6 Hz

$\lambda = 0.69$ m

therefore

$0.25\lambda = 17.3$ cm or 6.8 inches

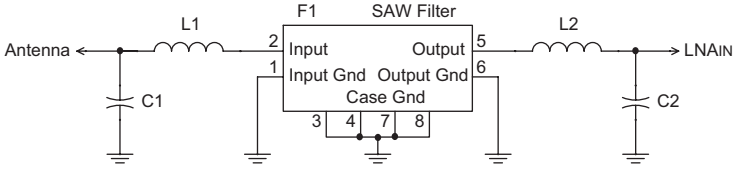
Finally, the wire antenna should be impedance matched to the preselector. The typical impedance of a one-quarter wavelength wire antenna is 36 Ω.

3.1.6 LNA GAIN

For a majority of applications, LNAGAIN can be tied to Vss (ground) enabling High Gain mode. If the application requires short range communications, LNAGAIN can be tied to VDD (pulled up) enabling Low Gain mode.

More Information on LNAGAIN operation can be found in the Circuit Description section.

FIGURE 3-5: SAW FILTER EXAMPLE CIRCUIT



Note: Refer to SAW filter manufacturer's data sheet for pin outs and values for impedance matching components.

3.1.7 LNA TUNED CIRCUIT

The LNAOUT (Pin 3) has an open-collector output. It is pulled up to VDD via a tuned circuit. It is also connected to 1IFIN (Pin 4) via a series decoupling capacitor. The 1IFIN input impedance is approximately 33 Ω || 1.5 pF.

Important: To ensure LNA stability the VSS pin (Pin 1) must be connected to a low impedance ground.

As shown in Figure 3-6, components C1 and L1 make up the tuned circuit and provide collector current via pull-up. Together with decoupling capacitor C2, they provided impedance matching between the LNA and MIXER1. To a lesser extent, C1, L1, and C2 provide band-pass filtering at the receive frequency (f_{rf}).

Component values depend on the selected receive frequency. The challenge is to design the circuit with the fewest components setting Q as high as possible as limited by component tolerances. For a majority of applications it is best to design a wide bandwidth tuned circuit to account for manufacturing and component tolerances. The best approach is to design the tuned circuit using a filter simulation program. Table 3-3 lists example component values for popular receive frequencies.

FIGURE 3-6: LNA OUTPUT TO MIXER1 EXAMPLE CIRCUIT.

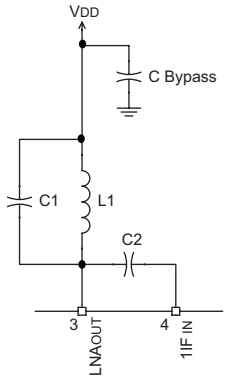


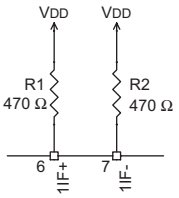
TABLE 3-3: LNA TUNED CIRCUIT EXAMPLE COMPONENT VALUES

f_{rf}	C1	L1	C2
315 MHz	7.0 pF	22 nH	6.0 pF
433.92 MHz	3.0 pF	15 nH	6.0 pF
868.3 MHz	2.0 pF	7.6 nH	3.0 pF
915 MHz	2.0 pF	6.8 nH	3.0 pF
These values are for design guidance only.			

3.1.8 MIXER1 BIAS

The 1IF+ (Pin 6) and 1IF- (Pin 7) are bias connections to the MIXER1 balanced collectors. Both pins are open-collector outputs and are individually pulled up to VDD by a load resistor. Figure 3-7 shows a MIXER1 bias example circuit.

FIGURE 3-7: MIXER1 BIAS EXAMPLE CIRCUIT



3.1.9 INTERMEDIATE FREQUENCY (IF) FILTER

The IF filter defines the overall adjacent signal selectivity of the receiver. For a majority of applications, low-cost 10.7 MHz ceramic IF filters are used. These are available in a variety of bandwidths and packages.

IF filter bandwidth selection is a function of:

- modulation (ASK, FSK or FM)
- signal bandwidth
- frequency and temperature tolerances of the transmitter and receiver components

The typical input and output impedance of ceramic filters is 330 Ω. 1IFOUT (Pin 9) has an approximately 330 Ω single-ended output impedance and provides a direct match to the ceramic IF filter. The internal resistance of the 2IFIN (Pin 11) is approximately 2.2 kΩ. In order to terminate ceramic IF filters a 390 Ω resistor can be paralleled to the 2IFIN and FBC2 (Pin 13). Figure 3-8 shows an example circuit schematic using a 10.7 MHz ceramic IF filter.

3.1.10 IF LIMITING AMPLIFIER EXTERNAL FEEDBACK CAPACITORS

FBC1 (Pin 12) and FBC2 (Pin 13) are connected to external feedback capacitors. Figure 3-8 shows component values and connections for these capacitors.

FIGURE 3-8: IF FILTER, LIMITING AMPLIFIER AND DEMODULATOR BLOCK DIAGRAM

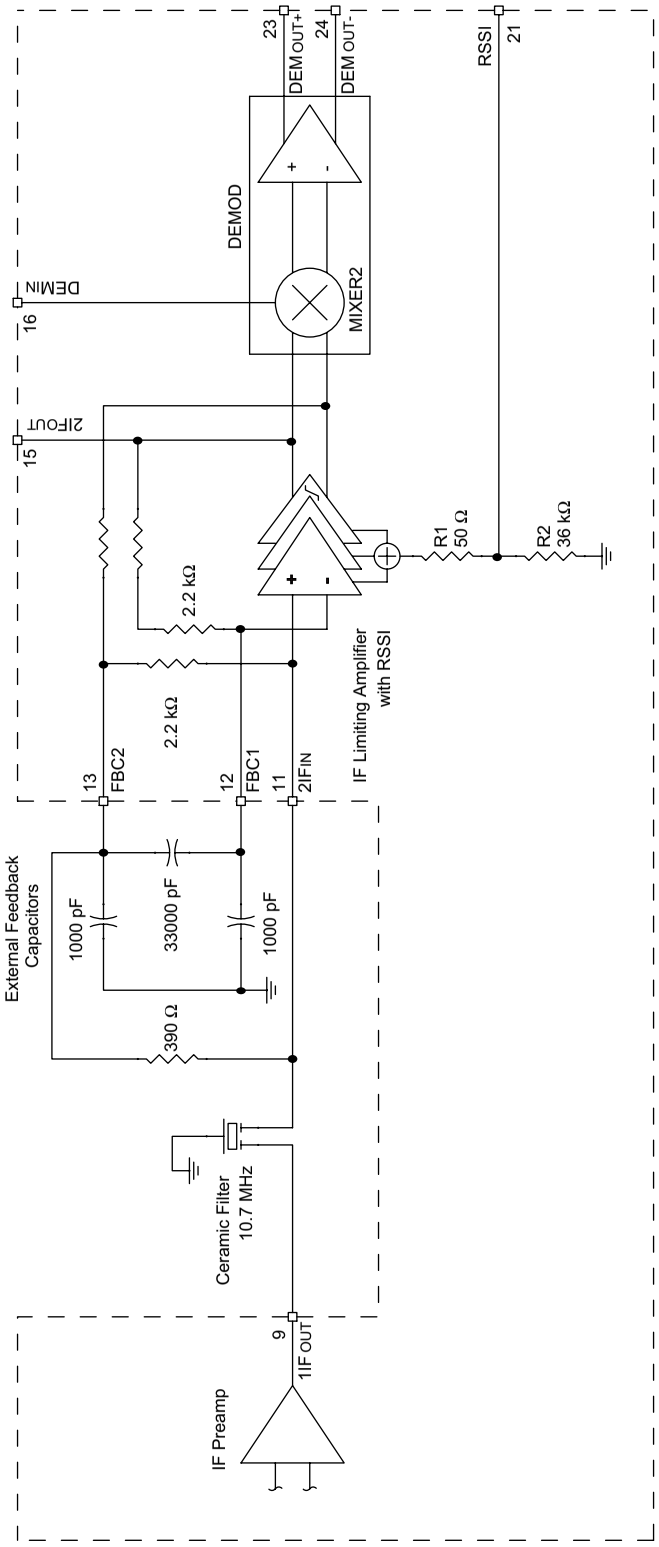
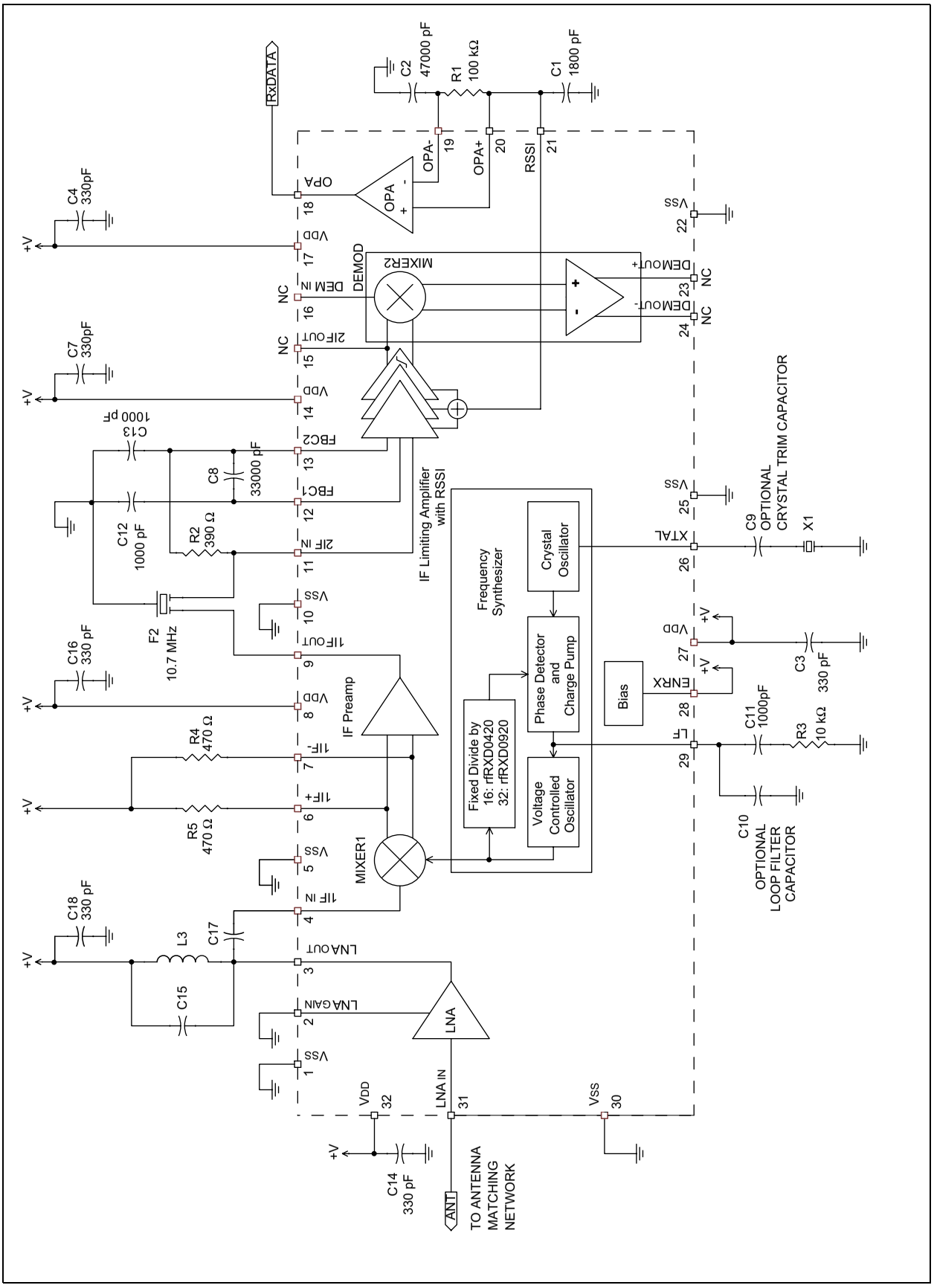


FIGURE 3-9: ASK APPLICATION CIRCUIT



3.2 Amplitude Shift Keying (ASK)

Figure 3-9 illustrates an example ASK applications circuit.

The IF Limiting Amplifier with RSSI is used as an ASK detector. The RSSI signal is post detector filtered and then compared to a reference voltage to determine if the incoming RF signal is a logical one or zero. The reference voltage can be configured as a dynamic voltage level determined by the incoming RF signal strength or by a predetermined fixed level.

3.2.1 RSSI POST DETECTOR FILTERING

The RSSI signal is low-passed filtered to remove high frequency and pulse noise to aid the decision making process of the comparator and increase the sensitivity of the receiver. The RSSI signal low-pass filter is a RC filter created by the RSSI output impedance of 36 kΩ and capacitor C1. Setting the time constant (RC = τ) of the RC filter depends on the signal period and when the signal decision will be made.

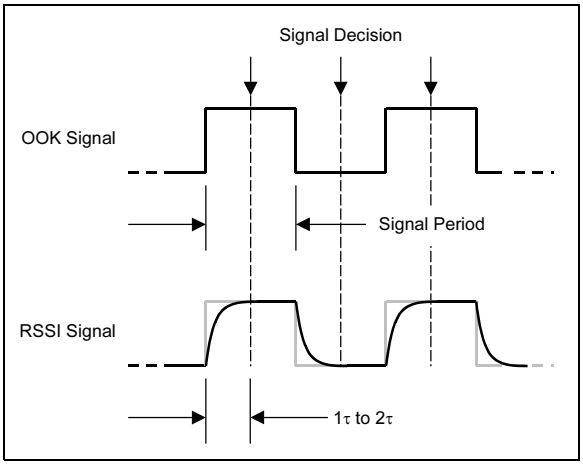
3.2.1.1 Signal Period

Optimum sensitivity of the receiver with reasonable pulse distortion occurs when the RC filter time constant is between 1 and 2 times the signal period. If the time constant of the RC filter is set too short, there is little noise filtering benefit. However, if the time constant of the RC filter is set too long, the data pulses will become elongated causing inter-symbol interference.

3.2.1.2 Signal Decision

If the bit decision occurs in the center of the signal period (such as KEELOQ decoders), then one or two times the RC filter time constant should be set at less than or equal to half the signal period. Figure 3-10 illustrates this method. The top trace represents the received on-off keying (OOK) signal. The bottom trace shows the RSSI signal after the RC low-pass filter.

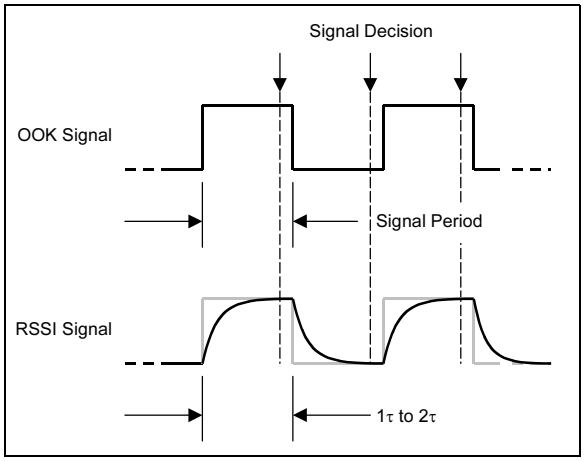
FIGURE 3-10: CENTER SIGNAL PERIOD DECISION RSSI LOW-PASS FILTERED



If the bit decision occurs near the end of the signal period, then the time constant should be set at less than or equal to the signal period. Figure 3-11 illustrates this method.

Once the signal decision time and time period of the signal period are known, then capacitor C1 can be selected. Once C1 is selected, the designer should observe the RSSI signal with an oscilloscope and perform operational and/or bit error rate testing to confirm receiver performance.

FIGURE 3-11: NEAR END OF THE SIGNAL PERIOD DECISION RSSI LOW-PASS FILTERED



3.2.2 COMPARATOR

The internal operational amplifier is configured as a comparator. The RSSI signal is applied to OPA+ (Pin 20) and compared with a reference voltage on OPA- (Pin 19) to determine the logic level of the received signal. The reference voltage can be dynamic or static.

The choice of dynamic versus static reference voltage depends in part on the ratio of logical ones versus zeros of the data (this can also be thought of as the AC content of the data). Provided the ratio has an even number of logical ones versus zeros, a dynamic reference voltage can be generated with a simple low-pass filter. The advantage of the dynamic reference voltage is the increased receiver sensitivity compared to a fixed reference voltage. However, the comparator will output random data. The decoder (for example, a programmed PICmicro MCU or KEELOQ decoder) must distinguish between random noise and valid data.

The choice of a static reference voltage depends in part on the DC content of the data. That is, the data has an uneven number of logical ones versus zeros. The disadvantage of the static reference voltage is decreased receiver sensitivity compared to a dynamic reference voltage. In this case, the comparator will output data without random noise.

3.2.2.1 DYNAMIC REFERENCE VOLTAGE

A dynamic reference voltage can be derived by averaging the received signal with a low-pass filter. The example ASK application circuit shown in Figure 3-9, the low-pass filter is formed by R1 and C2. The output of the low-pass filter is then fed to OPA-.

The setting of the R1-C2 time constant depends on the ratio of logical ones versus zeros and a trade off in stability versus receiver reaction time. If the received signal has an even number of logical ones versus zeros, the time constant can be set relatively short. Thus the reference voltage can react quickly to changes in the received signal amplitude and differences in transmitters. However, it may not be as stable and can fluctuate with the ratio of logical ones and zeros. If the time constant is set long, the reference voltage will be more stable. However, the receiver cannot react as quickly upon the reception of a received signal.

Selection of component values for R1 and C2 is an iterative process. First start with a time constant between 10 to 100 times the signal rate. Second, view the reference voltage against the RSSI signal to determine if the values are suitable. Figure 3-12 is an oscilloscope screen capture of an incoming RF square wave modulated signal (ASK on-off keying). The top trace is the data output of OPA (Pin 18). The two bottom traces are the RSSI signal (Pin 21, bottom square wave) and generated reference voltage (Pin 19, bottom trace centered in the RSSI square wave). The goal is to select values for R1 and C2 such that the reference voltage is in the middle of the RSSI signal. This reference voltage level provides the optimum data comparison of the incoming data signal.

3.2.2.2 STATIC REFERENCE VOLTAGE

A static reference voltage can be derived by a voltage divider network.

FIGURE 3-12: RSSI AND REFERENCE VOLTAGE COMPARISON

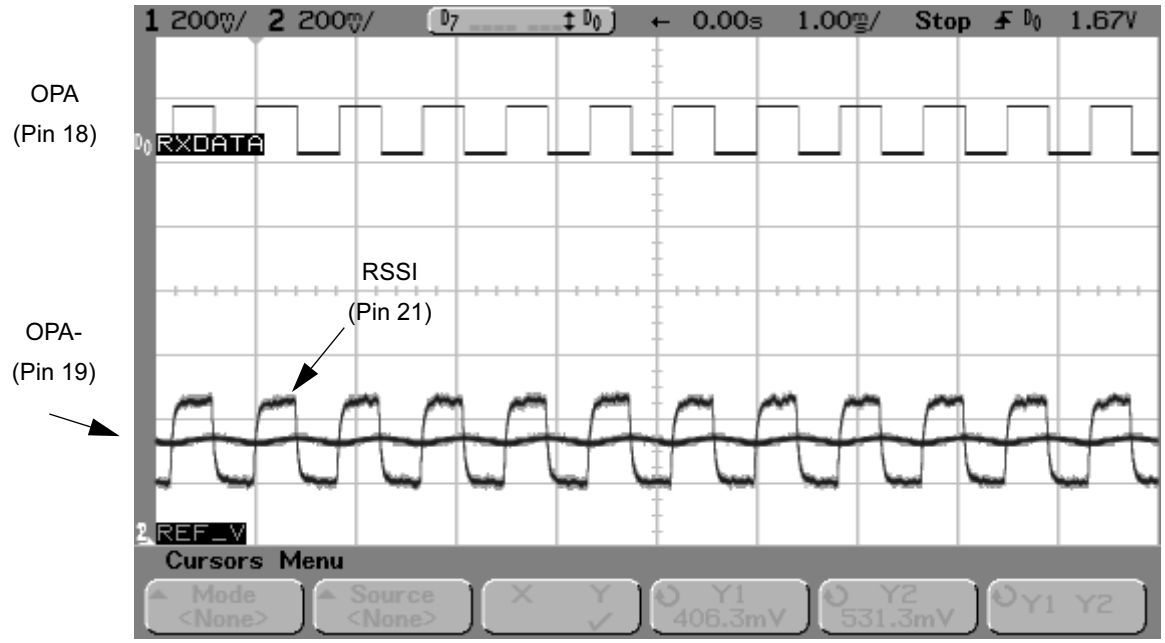
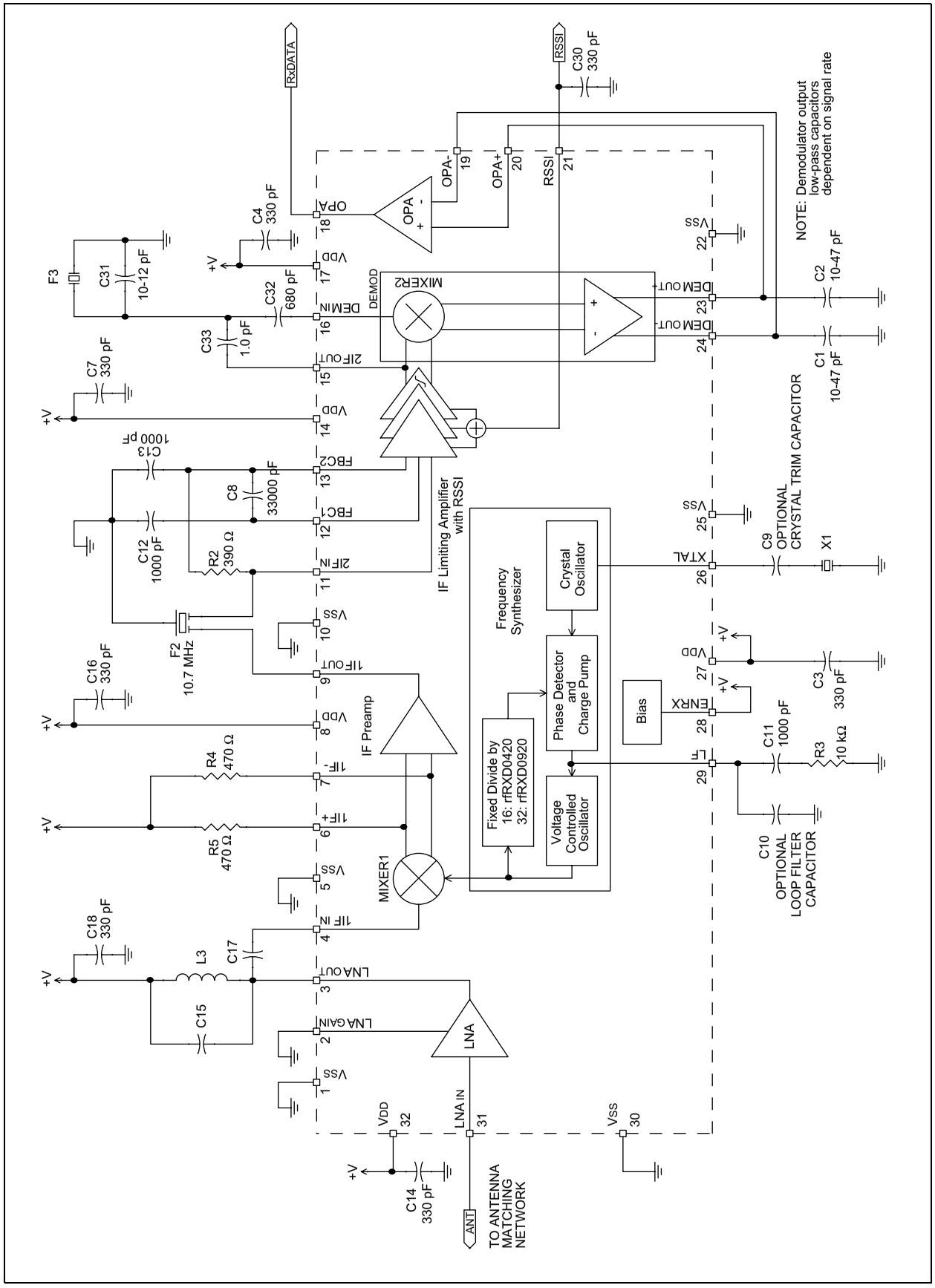


FIGURE 3-13: FSK APPLICATION CIRCUIT



3.3 Frequency Shift Keying (FSK)

Figure 3-13 illustrates an example FSK application circuit.

3.3.1 IF FILTER CONSIDERATIONS

As mentioned in the Section 3.1 above, IF filter bandwidth selection is a function of:

- modulation (ASK, FSK or FM)
- signal bandwidth
- frequency and temperature tolerances of the transmitter and receiver components

The occupied bandwidth of binary FSK signals is 2 times the peak frequency deviation plus 2 times the signal bandwidth. For example, if the data rate is 2400 bits per second Manchester encoded, the signal bandwidth is 4800 baud or 1200 Hz, and if the peak frequency deviation is 24 kHz, the minimum bandwidth of the IF filter is:

$$IF\ BW_{min} = (2 \times 2400) + (2 \times 24000)$$

$$IF\ BW_{min} = 52800\ Hz$$

Add to this value the frequency and temperature tolerances of the transmitter and receiver components.

FSK signals are more sensitive to group delay variations of the IF filter. Therefore, a filter with a low group delay variation should be used. As an alternative, a filter with wider than required bandwidth can be used because the group delay variation in the center of the bandpass will be relatively constant.

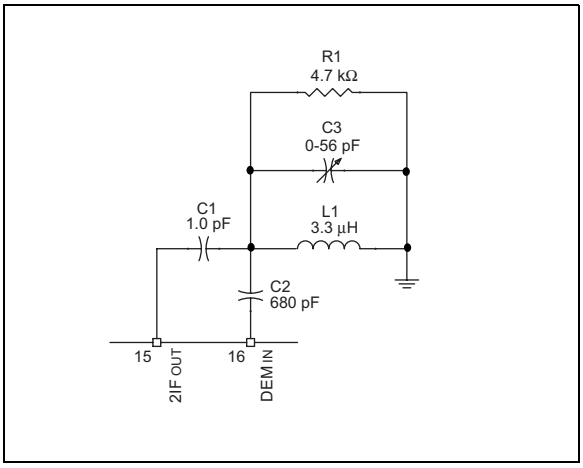
3.3.2 FSK DETECTOR

The demodulator (DEMOD) section consists of a phase detector (MIXER2) and amplifier creating a quadrature detector (also known as a phase coincidence detector) to demodulate the IF signal in FSK and FM modulation applications. The in-phase signal comes directly from the output of the IF limiting amplifier to MIXER2. The quadrature signal is created by an external tuned circuit from the output of the IF limiting amplifier (2IFOUT, Pin 15) AC-coupled to the MIXER2 DEMIN (Pin 16) input.

3.3.2.1 LC Discriminator

The external tuned circuit can be constructed from simple inductor-capacitor (LC) components. This type circuit produces and excellent output. However, one of the elements (L or C) must be tunable. Figure 3-14 illustrates an example LC discriminator circuit using a tunable capacitor. A similar circuit with a tunable inductor is also possible. Resistor R1 = 4.7 kΩ reduces the Q of the circuit so that frequency deviations of up to 75 kHz can be demodulated.

FIGURE 3-14: LC DISCRIMINATOR EXAMPLE CIRCUIT



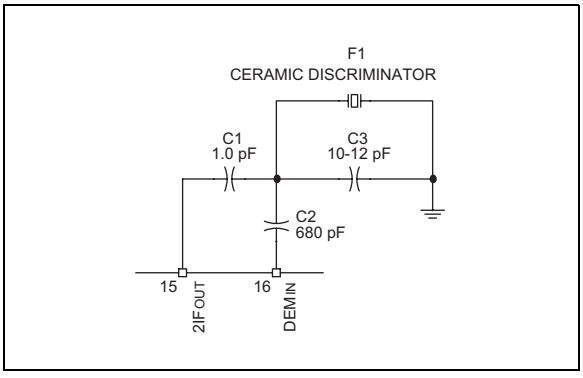
3.3.2.2 Ceramic Discriminator

A no-tune solution can be constructed with a ceramic discriminator. Figure 3-15 illustrates an example ceramic discriminator circuit.

The ceramic discriminator acts as a parallel tuned circuit at the IF frequency (for example, 10.7 MHz). The parallel capacitor C3 tunes the ceramic resonator. The high Q of this circuit enables higher output of the detector for small frequency deviations. However, smaller frequency deviations require better frequency tolerances at the transmitter and receiver.

In order to detect wider deviation or off-frequency signals, the detector bandwidth has to be increased. This can be accomplished by reducing the Q of the tuned circuit. One method is to parallel a resistor across the ceramic discriminator. A second is to increase the value of the coupling capacitor C1 increasing the load on the detector. The result of reducing the Q of the discriminator will be that the detector output will be smaller.

FIGURE 3-15: CERAMIC DISCRIMINATOR EXAMPLE CIRCUIT



3.3.3 POST DETECTOR FILTERING

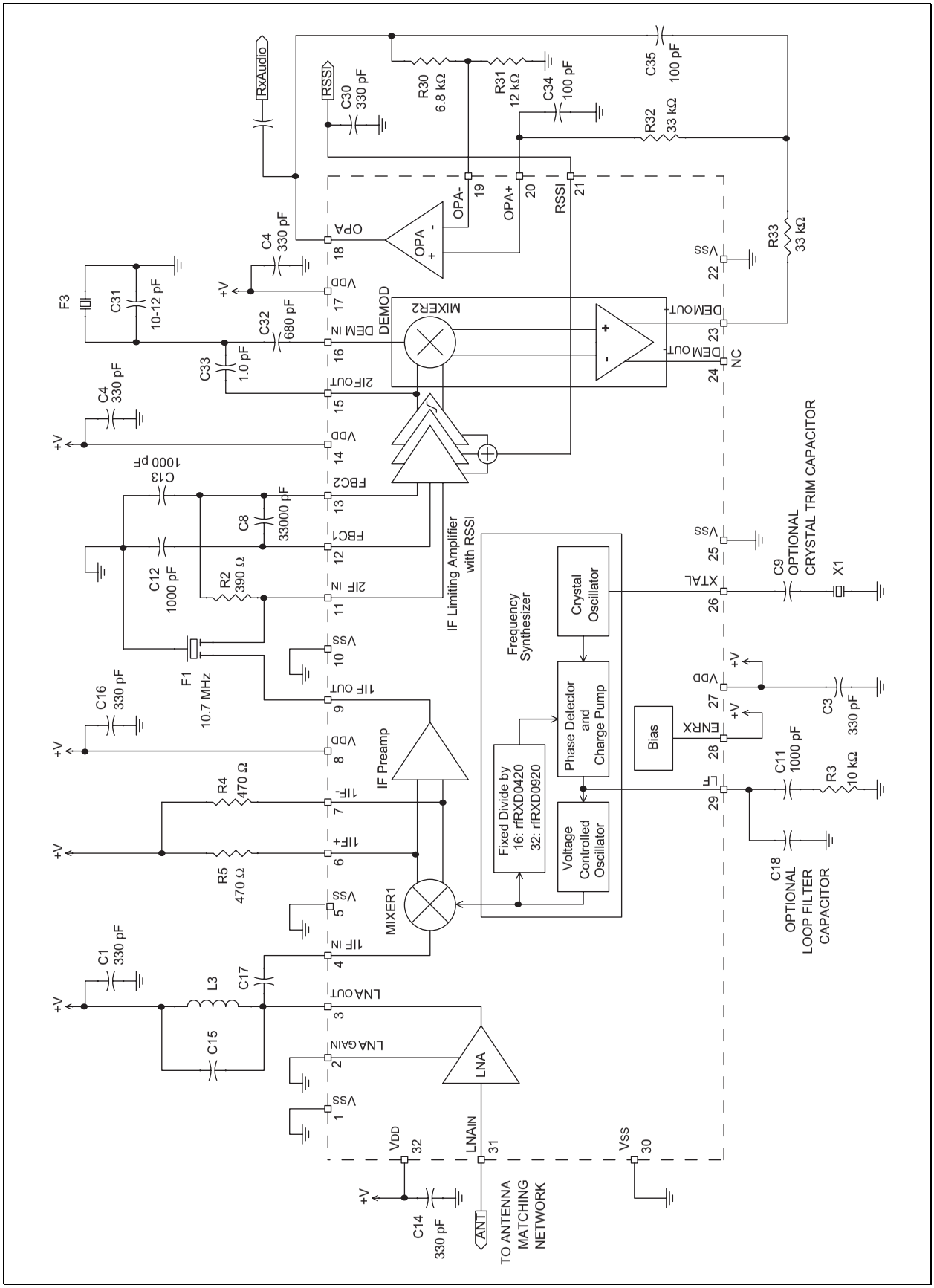
Care should be taken in selecting the values of capacitors C1 and C2 (Figure 3-13) so that the output of the detector is not distorted and receiver sensitivity improved. These values are chosen depending on the data signal rate.

Generally, if the data signal rate is fast then the filter time constant can be set short. Conversely, if the signal rate is slow, the filter time constant can be set long. The designer should observe the output of the detector with an oscilloscope and perform operational and/or bit error rate testing to confirm receiver performance.

3.3.4 COMPARATOR

The output of the DEMOD amplifier (DEMOUT+ and DEMOUT-, Pins 23 and 24) depends on the peak deviation of the FSK or FM signal and the Q of the external tuned circuit. DEMout+ and DEMout- are high impedance outputs with only a 20 μA current capability. The capacitance on these pins limit the maximum data signal rate. The nominal output voltage of these pins is 1.23V.

FIGURE 3-16: FM APPLICATION CIRCUIT



3.4 Frequency Modulation (FM)

Figure 3-16 illustrates an example FM application circuit.

3.4.1 FSK DETECTOR

FM demodulation is performed in the same manner as described in the FSK section above.

3.4.2 OPERATIONAL AMPLIFIER

The internal operational amplifier is configured as an active low-pass filter.

FM audio is typically de-emphasized. It is recommended that de-emphasis circuitry be connected at the output of the operational amplifier rather than the output of the detector.

4.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply voltage ..... 0 to +7.0V

Input voltage ..... -0.3 to VCC+0.3V

Input RF level 10dBm

Storage temperature ..... -40 to +125C

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.1 DC Characteristics: rfRXD0420 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VCC	Supply Voltage	2.5	—	5.5	V	f_{rf} < 400 MHz
			2.7	—	5.5	V	f_{rf} > 400 MHz
	ISTBY	Standby Current			100	nA	ENRX = 0
	ICC	Supply Current	5.0	6.5	8.0	mA	LNAGAIN = 1
			6.5	8.2	10.0	mA	LNAGAIN = 0
	VOPA	Op Amp input voltage offset	-20	—	20	mV	
	IOPA	Op Amp input current offset	-50	—	50	nA	
	IBIAS	Op Amp input bias current	-100		100	nA	
	VRSSI	RSSI voltage	0.5	1.0	1.5	V	LNAGAIN = 1
			1.25	1.9	2.45	V	LNAGAIN = 0

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3V, 23°C unless otherwise stated. These parameters are for design guidance only and are not tested.

4.2 AC Characteristics: rfRXD0420 (Industrial)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	TFSK	Start-up time - FSK/FM			0.9	ms	ENRX = 0 to 1
	TASK	Start-up time - ASK			R1xC1 +TFSK	ms	**Note 1**
		Sensitivity - Narrowband FSK		-111		dBm	**Note 2**
		Sensitivity - Wideband FSK		-104		dBm	**Note 3**
		Sensitivity - Narrowband ASK		-109		dBm	**Note 4**
		Sensitivity - Wideband ASK		-106		dBm	**Note 5**
		Input RF level maximum FSK/ FM		0		dBm	LNAGAIN = 1
		Input RF level maximum ASK		-10		dBm	LNAGAIN = 1

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3V, 23°C, f_{rf} = 433.6 MHz, IF = 10.7 MHz unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Dependant on ASK detector time constant.

2: IF bandwidth = 40 kHz, Δf = +/- 15 kHz, BER <= 3 x 10^{-3}

3: IF bandwidth = 150 kHz, Δf = +/- 50 kHz, BER <= 3 x 10^{-3}

4: IF bandwidth = 40 kHz, BER <= 3 x 10^{-3}

5: IF bandwidth = 150 kHz, BER <= 3 x 10^{-3}

4.3 DC Characteristics: rfRXD0920 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VCC	Supply Voltage	2.5	—	5.5	V	f_{rf} < 900 MHz
			3.3	—	5.5	V	f_{rf} > 900 MHz
	ISTBY	Standby Current			100	nA	ENRX = 0
	ICC	Supply Current	6.0	7.5	9.0	mA	LNAGAIN = 1
			7.5	9.2	11.0	mA	LNAGAIN = 0
	VOPA	Op Amp input voltage offset	-20	—	20	mV	
	IOPA	Op Amp input current offset	-50	—	50	nA	
	IBIAS	Op Amp input bias current	-100		100	nA	
	VRSSI	RSSI voltage	0.5	1.0	1.5	V	LNAGAIN = 1
			1.25	1.9	2.45	V	LNAGAIN = 0

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3V, 23°C unless otherwise stated. These parameters are for design guidance only and are not tested.

4.4 AC Characteristics: rfRXD0920 (Industrial)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	TFSK	Start-up time - FSK/FM			0.9	ms	ENRX = 0 to 1
	TASK	Start-up time - ASK			R1xC1 + TFSK	ms	**Note 1**
		Sensitivity - Narrowband FSK		-109		dBm	**Note 2**
		Sensitivity - Wideband FSK		-102		dBm	**Note 3**
		Sensitivity - Narrowband ASK		-108		dBm	**Note 4**
		Sensitivity - Wideband ASK		-104		dBm	**Note 5**
		Input RF level maximum FSK/ FM		0		dBm	LNAGAIN = 1
		Input RF level maximum ASK		-10		dBm	LNAGAIN = 1

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3V, 23°C, f_{rf} = 433.6 MHz, IF = 10.7 MHz unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Dependant on ASK detector time constant.

2: IF bandwidth = 40 kHz, Δf = +/- 15 kHz, BER <= 3 x 10^{-3}

3: IF bandwidth = 150 kHz, Δf = +/- 50 kHz, BER <= 3 x 10^{-3}

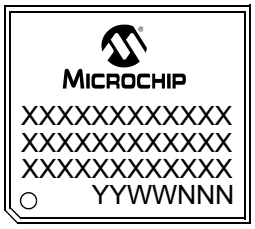
4: IF bandwidth = 40 kHz, BER <= 3 x 10^{-3}

5: IF bandwidth = 150 kHz, BER <= 3 x 10^{-3}

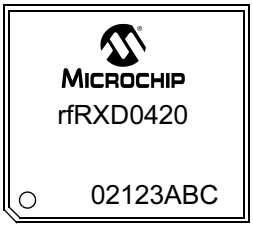
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

32-Lead LQFP



Example



Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.