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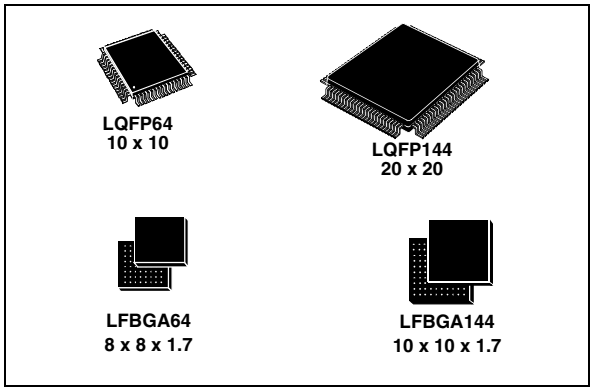
STR71xFxx STR710RZ

ARM7TDMI™ 32-bit MCU with Flash, USB, CAN, 5 timers, ADC, 10 communication interfaces

Features

- **Core**
  - ARM7TDMI 32-bit RISC CPU
  - 59 MIPS @ 66 MHz from SRAM
  - 45 MIPS @ 50 MHz from Flash
- **Memories**
  - Up to 256 Kbytes Flash program memory (10 kcycles endurance, 20 years retention @ 85 ° C)
  - 16 Kbytes Flash data memory (100 kcycles endurance, 20 years retention@ 85 ° C)
  - Up to 64 Kbytes RAM
  - External Memory Interface (EMI) for up to 4 banks of SRAM, Flash, ROM
  - Multi-boot capability
- **Clock, reset and supply management**
  - 3.0 to 3.6 V application supply and I/Os
  - Internal 1.8 V regulator for core supply
  - Clock input from 0 to 16.5 MHz
  - Embedded RTC osc. running from external 32 kHz crystal
  - Embedded PLL for CPU clock
  - Realtime Clock for clock-calendar function
  - 5 power saving modes: SLOW, WAIT, LPWAIT, STOP and STANDBY modes
- **Nested interrupt controller**
  - Fast interrupt handling with multiple vectors
  - 32 vectors with 16 IRQ priority levels
  - 2 maskable FIQ sources
- **Up to 48 I/O ports**
  - 30/32/48 multifunctional bidirectional I/Os Up to 14 ports with interrupt capability



- **5 timers**
  - 16-bit watchdog timer
  - 3 16-bit timers with 2 input captures, 2 output compares, PWM and pulse counter
  - 16-bit timer for timebase functions
- **10 communication interfaces**
  - 2 I^2C interfaces (1 multiplexed with SPI)
  - 4 UART asynchronous serial interfaces
  - Smartcard ISO7816-3 interface on UART1
  - 2 BSPI synchronous serial interfaces
  - CAN interface (2.0B Active)
  - USB Full Speed (12 Mbit/s) Device Function with Suspend and Resume
  - HDLC synchronous communications
- **4-channel 12-bit A/D converter**
  - Sampling frequency up to 1 kHz
  - Conversion range: 0 to 2.5 V
- **Development tools support**
  - Atomic bit SET and RES operations

Table 1. Device summary

Reference	Root part number
STR71xFxx	STR710FZ1, STR710FZ2 STR711FR0, STR711FR1, STR711FR2, STR712FR0, STR712FR1, STR712FR2, STR715FR0
STR710RZ	STR710RZ

Contents

List of tables

List of figures

1 Introduction

This datasheet provides the STR71x pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STR71x microcontroller memory, registers and peripherals. please refer to the STR71x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

Table 2. Device overview

Features	STR710 FZ1	STR710 FZ2	STR710 RZ	STR711 FR0	STR711 FR1	STR711 FR2	STR712 FR0	STR712 FR1	STR712 FR2	STR715 FRx
Flash - Kbytes	128+16	256+16	0	64+16	128+16	256+16	64+16	128+16	256+16	64+16
RAM - Kbytes	32	64	64	16	32	64	16	32	64	16
Peripheral Functions	CAN, EMI, USB, 48 I/Os			USB, 30 I/Os			CAN, 32 I/Os			32 I/Os
Operating Voltage	3.0 to 3.6 V									
Operating Temperature	-40 to +85°C or 0 to 70° C									
Packages	**T**=LQFP144 20 x 20 **H**=LFBGA144 10 x10			**T**=LQFP64 10 x10						

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2 Description

ARM® core with embedded Flash and RAM

The STR71x series is a family of ARM-powered 32-bit microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. STR71xF devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. STR710R devices have high-speed RAM but no internal Flash. The STR71x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs. The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

3 System architecture

Package choice: low pin-count 64-pin or feature-rich 144-pin LQFP or BGA

The STR71x family is available in 5 main versions.

The 144-pin versions have the full set of all features including CAN, USB and External Memory Interface (EMI).

- **STR710F:** 144-pin BGA or LQFP with CAN, USB and EMI
- **STR710R:** Flashless 144-pin BGA or LQFP with CAN, USB and EMI (no internal Flash memory)

The three 64-pin versions (LQFP) do not include External Memory Interface.

- **STR715F:** 64-pin LQFP without CAN or USB
- **STR711F:** 64-pin LQFP with USB
- **STR712F:** 64-pin LQFP with CAN

High speed Flash memory (STR71xF)

The Flash program memory is organized in two banks of 32-bit wide Burst Flash memories enabling true read-while-write (RWW) operation. Device Bank 0 is up to 256 Kbytes in size, typically for the application program code. Bank 1 is 16 Kbytes, typically used for storing data constants. Both banks are accessed by the CPU with zero wait states @ 33 MHz

Bank 0 memory endurance is 10K write/erase cycles and Bank 1 endurance is 100K write/erase cycles. Data retention is 20 years at 85°C on both banks. The two banks can be accessed independently in read or write. Flash memory can be accessed in two modes:

- Burst mode: 64-bit wide memory access at up to 50 MHz.
- Direct 32-bit wide memory access for deterministic operation at up to 33 MHz.

The STR7 embedded Flash memory can be programmed using In-Circuit Programming or In-Application programming.

IAP (in-application programming): The IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (in-circuit programming): The ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector Write Protection
- Flash Debug Protection (locks JTAG access)

Refer to the STR7 Flash Programming Reference manual for details.

Optional external memory (STR710)

The non-multiplexed 16-bit data/24-bit address bus available on the STR710 (144-pin) supports four 16-Mbyte banks of external memory. Wait states are programmable individually for each bank allowing different memory types (Flash, EPROM, ROM, SRAM etc.) to be used to store programs or data.

Figure 1 shows the general block diagram of the device family.

Flexible power management

To minimize power consumption, you can program the STR71x to switch to SLOW, WAIT, LPWAIT (low power wait), STOP or STANDBY mode depending on the current system activity in the application.

Flexible clock control

Two external clock sources can be used, a main clock and a 32 kHz backup clock. The embedded PLL allows the internal system clock (up to 66 MHz) to be generated from a main clock frequency of 16 MHz or less. The PLL output frequency can be programmed using a wide selection of multipliers and dividers. The microcontroller core, APB1 and APB2 peripherals are in separate clock domains and can be programmed to run at different frequencies during application runtime. The clock to each peripheral is gated with an individual control bit to optimize power usage by turning off peripherals any time they are not required.

Voltage regulators

The STR71x requires an external 3.0-3.6V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply for the core and peripherals. The main VR is switched off during low power operation.

Low voltage detectors

Both the Main Voltage Regulator and the Low Power Voltage Regulator contain each a low voltage detection circuitry which keep the device under reset when the corresponding controlled voltage value (V_{18} or V_{18BKP}) falls below 1.35V (+/- 10%). This enhances the security of the system by preventing the MCU from going into an unpredictable state.

An external reset circuit must be used to provide the RESET at V_{33} power-up. It is not sufficient to rely on the RESET generated by the LVD in this case. This is because LVD operation is guaranteed only when V_{33} is within the specification.

3.1 On-chip peripherals

CAN interface (STR710 and STR712)

The CAN module is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

USB interface (STR710 and STR711)

The full-speed USB interface is USB V2.0 compliant and provides up to 16 bidirectional/32 unidirectional endpoints, up to 12 Mb/s (full-speed), support for bulk transfer, isochronous transfers and USB Suspend/Resume functions.

Standard timers

Each of the four timers have a 16-bit free-running counter with 7-bit prescaler

Three timers each provide up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

The fourth timer is not connected to the I/O ports. It can be used by the application software for general timing functions.

Realtime clock (RTC)

The RTC provides a set of continuously running counters driven by the 32 kHz external crystal. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR71x is in Standby mode the RTC can be kept running, powered by the low power voltage regulator and driven by the 32 kHz external crystal.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 1.25 Mb/s.

Smartcard interface

UART1 is configurable to function either as a general purpose UART or as an asynchronous Smartcard interface as defined by ISO 7816-3. It includes Smartcard clock generation and provides support features for synchronous cards.

Buffered serial peripheral interfaces (BSPI)

Each of the two SPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 5.5 Mb/s in Master mode and 4 Mb/s in Slave mode.

I^2C interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

One I^2C Interface is multiplexed with one SPI, so either 2xSPI+1x I^2C or 1xSPI+2x I^2C may be used at a time.

HDLC interface

The High Level Data Link Controller (HDLC) unit supports full duplex operation and NRZ, NRZI, FM0 or MANCHESTER protocols. It has an internal 8-bit baud rate generator.

A/D converter

The Analog to Digital Converter, converts in single channel or up to 4 channels in single-shot or round robin mode. Resolution is 12-bit with a sampling frequency of up to 1 kHz. The input voltage range is 0-2.5V.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

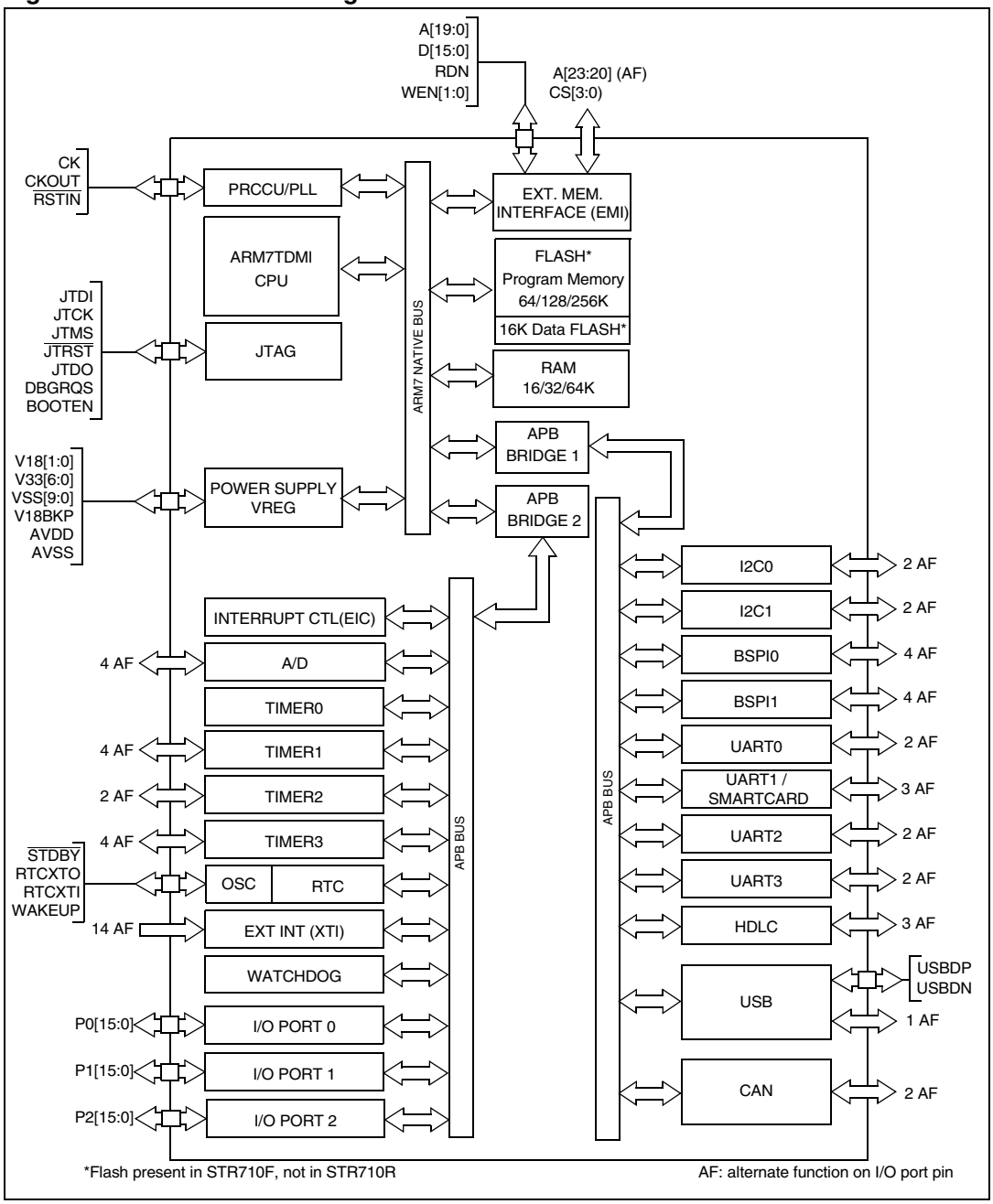
I/O ports

The 48 I/O ports are programmable as Inputs or Outputs.

External interrupts

Up to 14 external interrupts are available for application use or to wake up the application from STOP mode.

Figure 1. STR71x block diagram



3.2 Related documentation

Available from www.arm.com:

ARM7TDMI Technical reference manual

Available from http://www.st.com:

STR71x Reference manual

STR7 Flash programming manual

AN1774 - STR71x Software development getting started

AN1775 - STR71x Hardware development getting started

AN1776 - STR71x Enhanced interrupt controller

AN1777 - STR71x memory mapping

AN1780 - Real time clock with STR71x

AN1781 - Four 7 segment display drive using the STR71x

The above is a selected list only, a full list STR71x application notes can be viewed at http://www.st.com.

3.3 Pin description for 144-pin packages

Figure 2. STR710 LQFP pinout

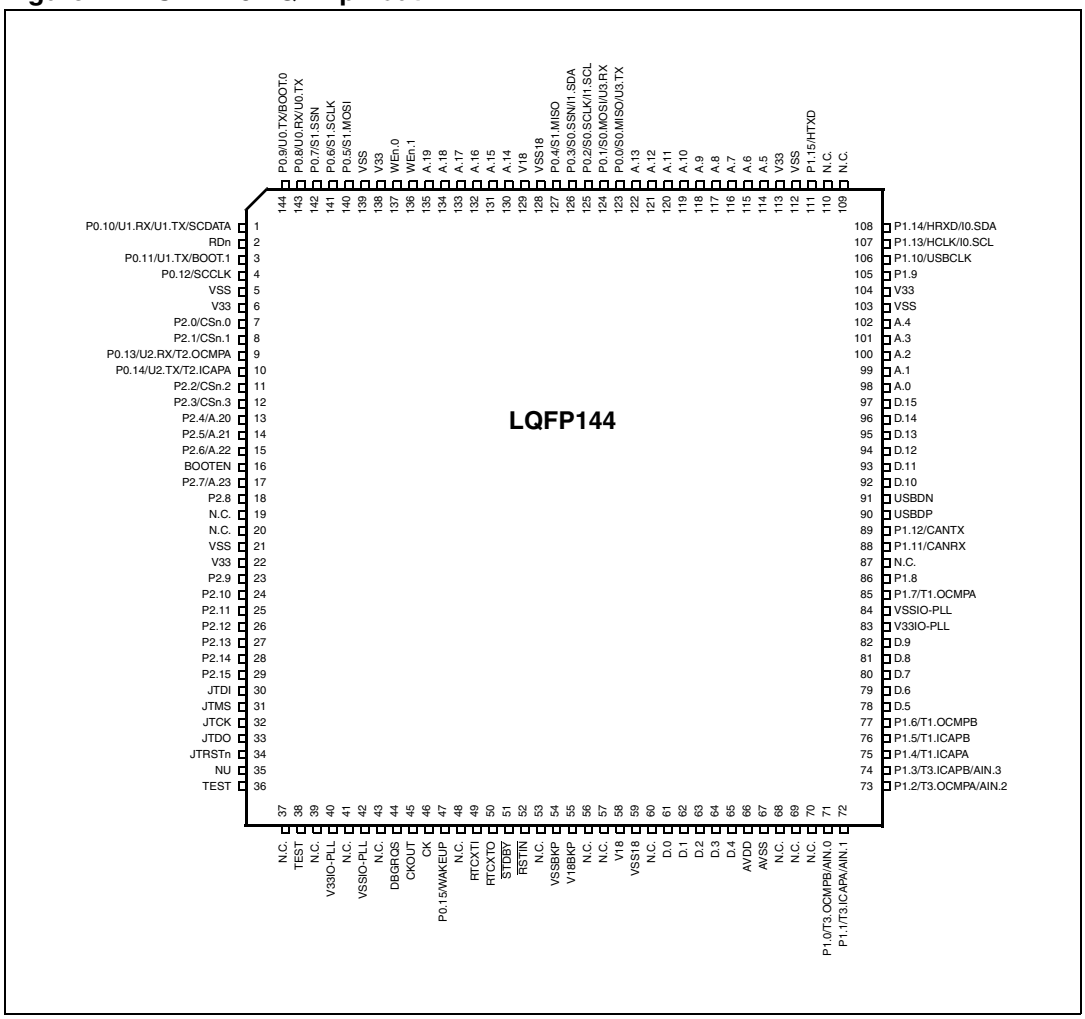


Table 3. STR710 BGA ball connections

	A	B	C	D	E	F	G	H	J	K	L	M
1	P0.10	P2.0	P2.1	VSS	P2.2	P2.6	BOOT EN	P2.12	P2.13	P2.15	JTDI	N.C.
2	VSS	RDn	P0.11	V33	P2.3	P2.8	P2.9	JTMS	JTRSTn	TEST	TEST	N.C.
3	V33	P0.9	P0.12	P0.13	P2.4	N.C.	P2.10	JTCK	NU	V33	N.C.	DBG RQS
4	P0.6	P0.7	P0.8	P0.14	P2.5	N.C.	P2.11	JTDO	CK	CKOUT	VSSIO-PLL	N.C.
5	A.19	WEn.1	WEn.0	P0.5	P2.7	VSS	P2.14	N.C.	RTCX-TO	RTCXTI	N.C.	P0.15
6	P0.3	A.15	A.16	A.17	A.18	V33	V18	N.C.	N.C.	V18BKP	VSS BKP	$\overline{\text{STDBY}}$
7	P0.2	P0.1	P0.4	VSS18	V18	A.14	D.12	D.1	D.0	nc	VSS18	$\overline{\text{RSTIN}}$
8	A.9	A.10	A.11	A.13	P0.0	A.0	D.11	P1.12/ CANTX	N.C.	AVSS	D.3	D.2
9	VSS	V33	A.5	A.6	V33	D.15	D.10	P1.8	D.9	P1.0	N.C.	N.C.
10	A.8	N.C.	P1.15	P1.13	VSS	D.14	USBDN	P1.7	D.8	P1.5	P1.1	D.4
11	A.7	N.C.	P1.14	P1.10	A.2	D.13	USBDP	VSS	D.5	P1.4	P1.3	AVDD
12	A.12	A.4	A.3	P1.9	A.1	P1.11/ CANRX	N.C.	V33IO-PLL	P1.6	D.7	D.6	P1.2

Legend / abbreviations for *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8 V/2 V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8 V / 2 V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5 V tolerant.

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
1	A1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
												Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	B2	$\overline{RD}$	O	5)					X		External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components.		
3	C2	P0.11/BOOT.1 /U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
4	C3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
5	D1	V_{SS}	S								Ground voltage for digital I/Os[4]		
6	D2	V_{33}	S								Supply voltage for digital I/Os[4]		
7	B1	P2.0/$\overline{CS}$.0	I/O	8)	C_T		8mA	X	X		Port 2.0	External Memory Interface: Select Memory Bank 0 output **Note:** This pin is forced to output push-pull 1 mode at reset to allow boot from external memory	
8	C1	P2.1/$\overline{CS}$.1	I/O	pu 2)	C_T		8mA	X	X		Port 2.1	External Memory Interface: Select Memory Bank 1 output	
9	D3	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
10	D4	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
11	E1	P2.2/$\overline{CS}$.2	I/O	pu 2)	C_T		8mA	X	X		Port 2.2	External Memory Interface: Select Memory Bank 2 output	
12	E2	P2.3/$\overline{CS}$.3	I/O	pu 2)	C_T		8mA	X	X		Port 2.3	External Memory Interface: Select Memory Bank 3 output	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP			
13	E3	P2.4/A.20	I/O	pd[3]	C_T		8mA	X	X		Port 2.4	External Memory Interface: address bus
14	E4	P2.5/A.21	I/O	pd[3]	C_T		8mA	X	X		Port 2.5	
15	F1	P2.6/A.22	I/O	pd[3]	C_T		8mA	X	X		Port 2.6	
16	G1	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins	
17	E5	P2.7/A.23	I/O	pd[3]	C_T		8mA	X	X		Port 2.7	External Memory Interface: address bus
18	F2	P2.8	I/O	pu	C_T	X	4mA	X	X		Port 2.8	External interrupt INT2
19	F3	N.C.									Not connected (not bonded)	
20	F4	N.C.									Not connected (not bonded)	
21	F5	V_{SS}	S								Ground voltage for digital I/Os[4]	
22	F6	V_{33}	S								Supply voltage for digital I/Os[4]	
23	G2	P2.9	I/O	pu	C_T	X	4mA	X	X		Port 2.9	External interrupt INT3
24	G3	P2.10	I/O	pu	C_T	X	4mA	X	X		Port 2.10	External interrupt INT4
25	G4	P2.11	I/O	pu	C_T	X	4mA	X	X		Port 2.11	External interrupt INT5
26	H1	P2.12	I/O	pu	C_T		4mA	X	X		Port 2.12	
27	J1	P2.13	I/O	pu	C_T		4mA	X	X		Port 2.13	
28	G5	P2.14	I/O	pu	C_T		4mA	X	X		Port 2.14	
29	K1	P2.15	I/O	pu	C_T		4mA	X	X		Port 2.15	
30	L1	JTDI	I		T_T						JTAG Data input. External pull-up required.	
31	H2	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.	
32	H3	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.	
33	H4	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.	
34	J2	JTRST	I		T_T						JTAG Reset Input. External pull-up required.	
35	J3	NU									Reserved, must be forced to ground.	
36	K2	TEST									Reserved, must be forced to ground.	
37	M1	N.C.									Not connected (not bonded)	
38	L2	TEST									Reserved, must be forced to ground.	
39	L3	N.C.									Not connected (not bonded)	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP			
40	K3	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference	
41	M4	N.C.									Not connected (not bonded)	
42	L4	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4]	
43	M2	N.C.									Not connected (not bonded)	
44	M3	DBGRQS	I		C_T						Debug Mode request input (active high)	
45	K4	CKOUT	O				8mA		X		Clock output (f_{PCLK2}) **Note:** Enabled by CKDIS register in APB Bridge 2	
46	J4	CK	I		C						Reference clock input	
47	M5	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input. **Note:** This port is input only.
48	L5	N.C.									Not connected (not bonded)	
49	K5	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit	
50	J5	RTCXTO									Output of 32 kHz oscillator amplifier circuit	
51	M6	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby	
52	M7	$\overline{RSTIN}$	I		C_T					X	Reset input	
53	H5	N.C.									Not connected (not bonded)	
54	L6	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.	
55	K6	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.	
56	J6	N.C.									Not connected (not bonded)	
57	H6	N.C.									Not connected (not bonded)	
58	G6	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
59	L7	V_{SS18}	S								Stabilization for main voltage regulator.		
60	K7	N.C.									Not connected (not bonded)		
61	J7	D.0	I/O	6)			8mA				External Memory Interface: data bus		
62	H7	D.1	I/O	6)			8mA						
63	M8	D.2	I/O	6)			8mA						
64	L8	D.3	I/O	6)			8mA						
65	M10	D.4	I/O	6)			8mA						
66	M11	V_{DDA}	S								Supply voltage for A/D Converter		
67	K8	V_{SSA}	S								Ground voltage for A/D Converter		
68	J8	N.C.									Not connected (not bonded)		
69	M9	N.C.									Not connected (not bonded)		
70	L9	N.C.									Not connected (not bonded)		
71	K9	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
72	L10	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
73	M12	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
74	L11	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
75	K11	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input
76	K10	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
77	J12	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
78	J11	D.5	I/O	6)			8mA				External Memory Interface: data bus		
79	L12	D.6	I/O	6)			8mA						
80	K12	D.7	I/O	6)			8mA						
81	J10	D.8	I/O	6)			8mA						
82	J9	D.9	I/O	6)			8mA						

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
83	H12	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[4]		
84	H11	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4]		
85	H10	P1.7/T1.OCMPA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
86	H9	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
87	G12	N.C.									Not connected (not bonded)		
88	F12	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
89	H8	P1.12/CANTX	I/O	pu	C_T		4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
90	G11	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
91	G10	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
92	G9	D.10	I/O	6)			8mA				External Memory Interface: data bus		
93	G8	D.11	I/O	6)			8mA						
94	G7	D.12	I/O	6)			8mA						
95	F11	D.13	I/O	6)			8mA						
96	F10	D.14	I/O	6)			8mA						
97	F9	D.15	I/O	6)			8mA						
98	F8	A.0	O	7)			8mA		X		External Memory Interface: address bus		
99	E12	A.1	O	7)			8mA		X				
100	E11	A.2	O	7)			8mA		X				
101	C12	A.3	O	7)			8mA		X				
102	B12	A.4	O	7)			8mA		X				
103	E10	V_{SS}	S								Ground voltage for digital I/O circuitry[4]		
104	E9	V_{33}	S								Supply voltage for digital I/O circuitry[4]		
105	D12	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
106	D11	P1.10/ USBCLK	I/O	pd	C/ T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
107	D10	P1.13/HCLK/ I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
108	C11	P1.14/HRXD/ I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
109	B11	N.C.									Not connected (not bonded)		
110	B10	N.C.									Not connected (not bonded)		
111	C10	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
112	A9	V_{SS}	S								Ground voltage for digital I/O circuitry[4]		
113	B9	V_{33}	S								Supply voltage for digital I/O circuitry[4]		
114	C9	A.5	O	[7]			8mA		X		External Memory Interface: address bus		
115	D9	A.6	O	[7]			8mA		X				
116	A11	A.7	O	[7]			8mA		X				
117	A10	A.8	O	[7]			8mA		X				
118	A8	A.9	O	[7]			8mA		X				
119	B8	A.10	O	[7]			8mA		X				
120	C8	A.11	O	[7]			8mA		X				
121	A12	A.12	O	[7]			8mA		X				
122	D8	A.13	O	[7]			8mA		X				
123	E8	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
124	B7	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
125	A7	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
126	A6	P0.3/S0.$\overline{SS}$/ I1.SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
127	C7	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
128	D7	V_{SS18}	S								Stabilization for main voltage regulator.		
129	E7	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
130	F7	A.14	O	7)			8mA		X		External Memory Interface: address bus		
131	B6	A.15	O	7)			8mA		X				
132	C6	A.16	O	7)			8mA		X				
133	D6	A.17	O	7)			8mA		X				
134	E6	A.18	O	7)			8mA		X				
135	A5	A.19	O	7)			8mA		X				
136	B5	$\overline{WE}$.1	O	5)			8mA		X		External Memory Interface: active low MSB write enable output		
137	C5	$\overline{WE}$.0	O	5)			8mA		X		External Memory Interface: active low LSB write enable output		
138	A3	V_{33}	S								Supply voltage for digital I/Os[4]		
139	A2	V_{SS}	S								Ground voltage for digital I/Os[4]		
140	D5	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
141	A4	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
142	B4	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

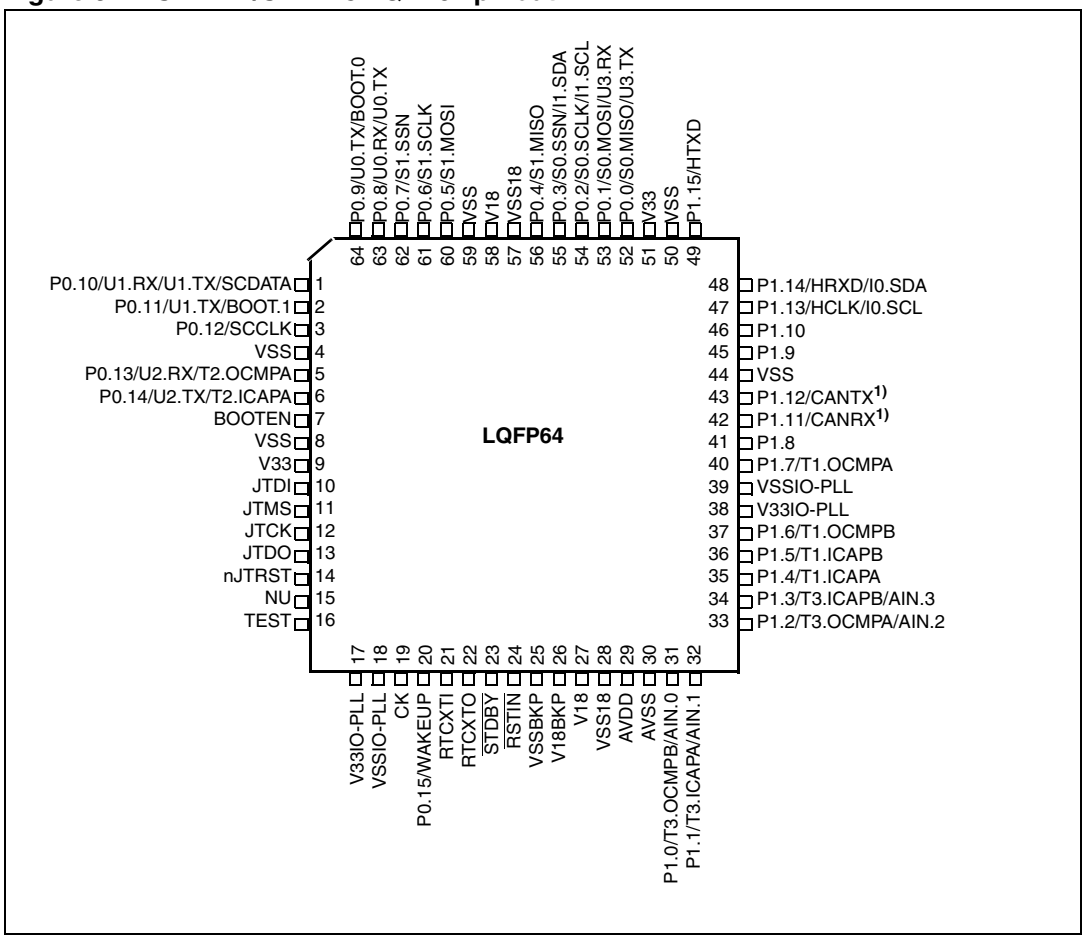
Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
143	C4	P0.8/U0.RX/ U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
											Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
144	B3	P0.9/U0.TX/ BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*) to be used by the External Memory Interface.
3. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*).
4. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.
5. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Output Push-Pull.
6. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Hi-Z.
7. During the reset phase, these pins are in input pull-down state. When reset is released, they are configured as Output Push-Pull.
8. During the reset phase, this pin is in input floating state. When reset is released, it is configured as Output Push-Pull.

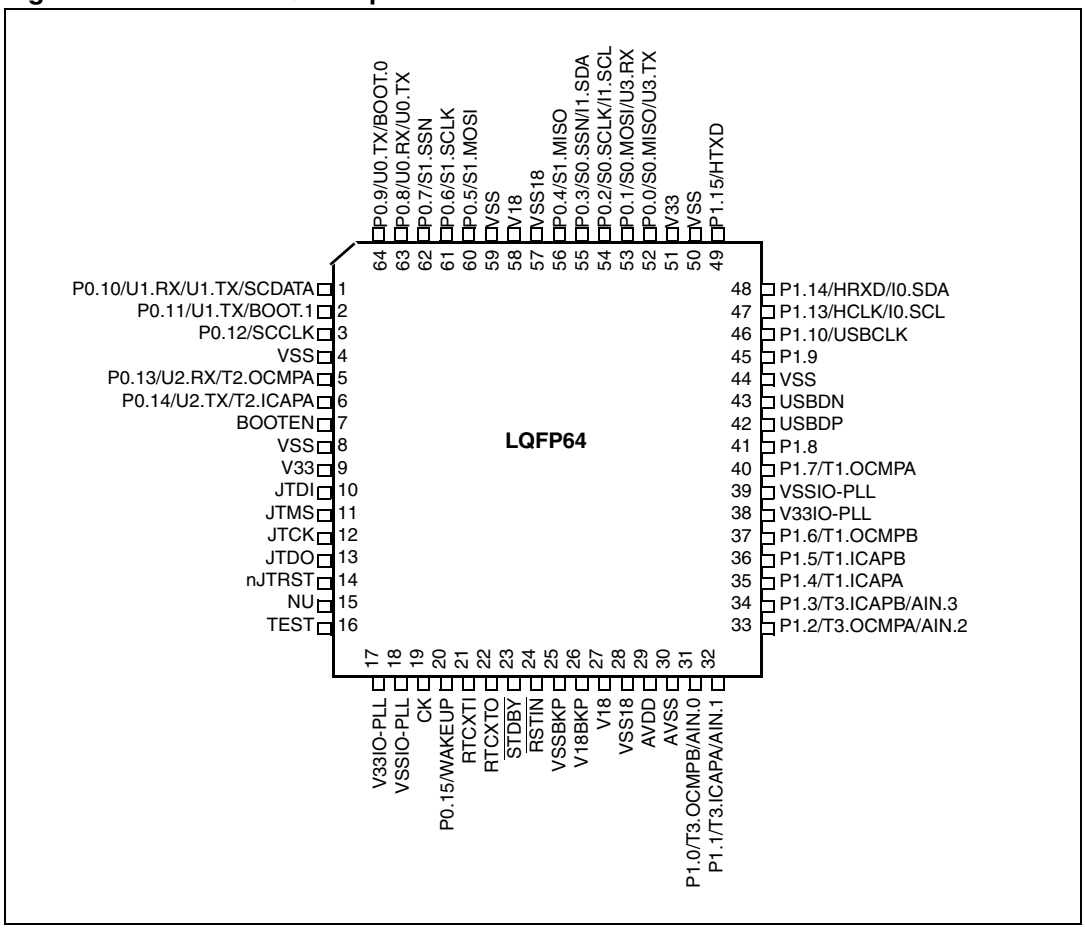
3.4 Pin description for 64-pin packages

Figure 3. STR712/STR715 LQFP64 pinout



1. CANTX and CANRX in STR712F only, in STR715F they are general purpose I/Os.

Figure 4. STR711 LQFP64 pinout



Legend / abbreviations for *Table 5*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8V / 2V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8V / 2V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Table 5. STR711/STR712/STR715 pin description

Pin n°	Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
											Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	P0.11/BOOT.1 /U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
4	V_{SS}	S								Ground voltage for digital I/Os[2]		
5	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
6	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
7	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins		
8	V_{SS}	S								Ground voltage for digital I/Os[2]		
9	V_{33}	S								Supply voltage for digital I/Os[2]		
10	JTDI	I		T_T						JTAG Data input. External pull-up required.		
11	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.		
12	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.		
13	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.		
14	JTRST	I		T_T						JTAG Reset Input. External pull-up required.		
15	NU									Reserved, must be forced to ground.		
16	TEST									Reserved, must be forced to ground.		
17	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
18	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
19	CK	I		C						Reference clock input		