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RM25C128A

128Kbit 2.7V Minimum Boot Memory SPI Bus

Preliminary Datasheet

Features

- Memory array: 128Kbit EEPROM-compatible boot memory
- Single supply voltage: 2.7V - 3.6V
- Serial peripheral interface (SPI) compatible
- Supports SPI modes 0 and 3
- 1.6MHz maximum clock rate for normal read
- 5MHz maximum clock rate for fast read
- Page size: 64 byte
  -Byte and Page Write from 1 to 64 bytes
  -Byte Write within 25µs
  -Page Write within 1ms
- Self-timed erase and write cycles
- Page or chip erase capability
- 1mA read current, 1.5mA write current, 5µA power-down current
- 8-lead packages
- RoHS-compliant and halogen-free packaging
- Data Retention: 10 years

Description

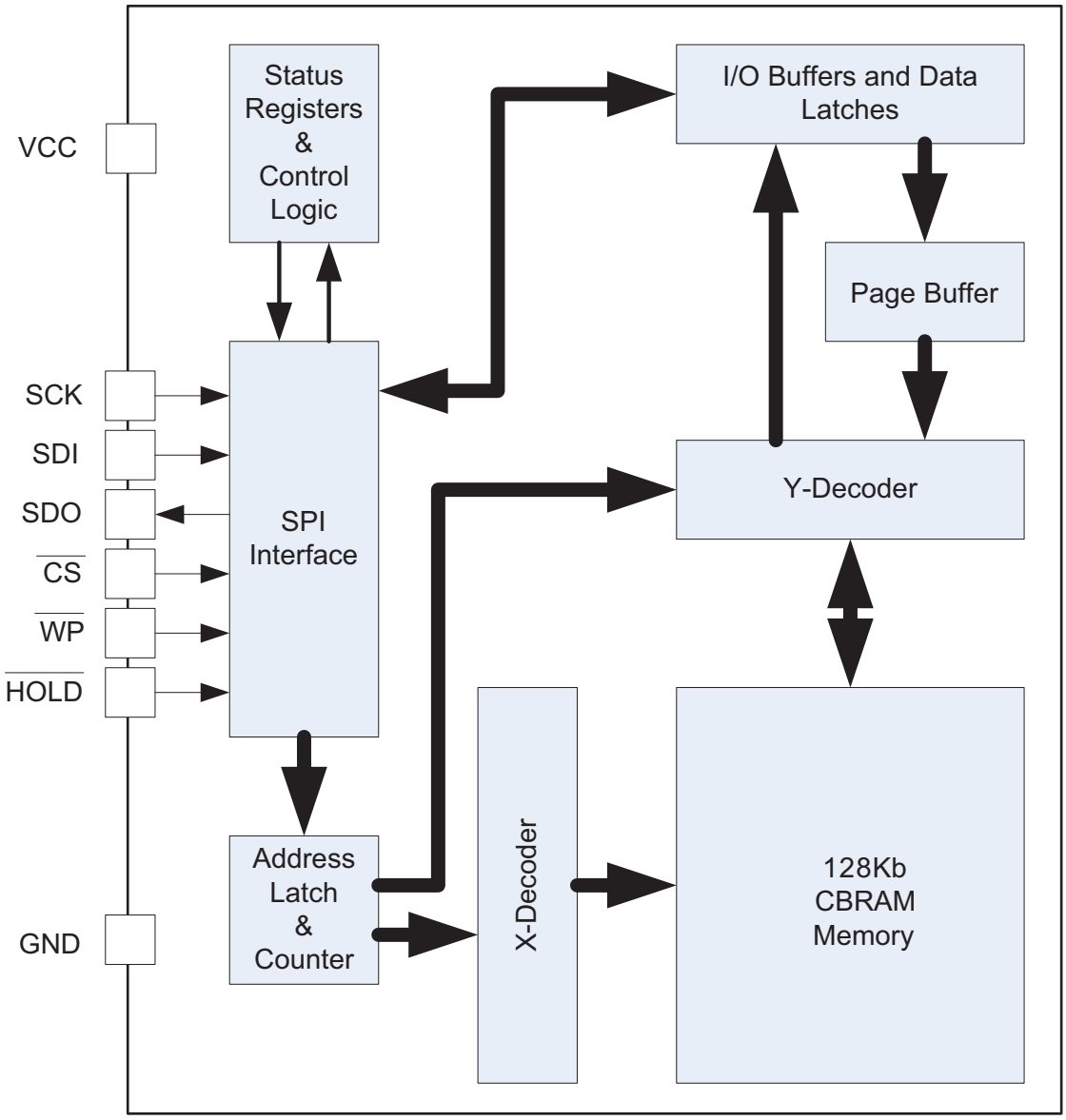
The RM25C128A is an EEPROM-compatible, 128Kbit non-volatile boot memory utilizing Adesto's serial memory technology. The memory device uses a single low-voltage supply ranging from 2.7V to 3.6V.

The Adesto® RM25C128A is accessed through a 4-wire SPI interface consisting of a Serial Data Input (SDI), Serial Data Output (SDO), Serial Clock (SCK), and Chip Select ($\overline{CS}$). The maximum clock (SCK) frequency in normal read mode is 1.6MHz. In fast read mode the maximum clock frequency is 5MHz.

Writing into the device can be done from one to 64 bytes at a time. All writing is internally self-timed. The device also features an Erase which can be performed on 64-byte pages, or the whole chip. Writing a single byte to the RM25C32C device consumes only 10% of the energy required by a Byte Write operation of EEPROM devices of similar size.

1. Block Diagram

Figure 1-1. Block Diagram



2. Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings[1]

Parameter	Specification
Operating ambient temp range	0°C to +70° C
Storage temperature range	-20°C to +100°C
Input supply voltage, VCC to GND	- 0.3V to 3.6V
Voltage on any pin with respect to GND	-0.3V to (VCC + 0.3)
ESD protection on all pins (Human Body Model)	>2kV
Junction temperature	85°C
DC output current	5mA

1. CAUTION: Stresses greater than Absolute Maximum Ratings may cause permanent damage to the devices. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in other sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may reduce device reliability

3. Electrical Characteristics

3.1 DC Operating Characteristics

Applicable over recommended operating range: TA = 0°C to +70° C, VCC = 2.7V to 3.6V

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Supply Range		2.7		3.6	V
V_{VCCI}	VCC Inhibit				2.4	V
I_{CC1}	Supply current, Fast Read	V_{CC}= 3.6V SCK at 5 MHz SDO = Open, Read		1.2	3	mA
I_{CC2}	Supply Current, Read Operation	V_{CC}= 3.6V SCK at 1.6 MHz SDO = Open, Read		1	2	mA
I_{CC3}	Supply Current, Program or Erase	V_{CC}= 3.6V SCK at 5 MHz		1.5	3	mA
I_{CC4}	Supply Current, Standby	V_{CC}= 3.6V $\overline{CS}$ = V_{CC}		100	200	µA
I_{CC5}	Supply Current, Power Down	V_{CC}= 3.6V Power Down		5	20	µA
I_{IL}	Input Leakage	SCK, SDI, $\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$ V_{IN}=0V to V_{CC}			1	µA
I_{LO}	Output Leakage	SDO , $\overline{CS}$ = V_{CC} V_{IN}=0V to V_{CC}			1	µA
V_{IL}	Input Low Voltage	SCK, SDI, $\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$	-0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage	SCK, SDI, $\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$	V_{CC} x 0.7		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{CC} - 0.2			V

3.2 AC Operating Characteristics

Applicable over recommended operating range: TA = 0°C to +70° C, VCC = 2.7V to 3.6V
CL = 1 TTL Gate plus 10pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCKF}	SCK Clock Frequency for Fast Read Mode	0		5	MHz
f_{SCK}	SCK Clock Frequency for Normal Read Mode	0		1.6	MHz
t_{RI}	SCK Input Rise Time			1	µs
t_{FL}	SCK Input Fall Time			1	µs
t_{SCKH}	SCK High Time	7.5			ns
t_{SCKL}	SCK Low Time	7.5			ns
t_{CS}	$\overline{CS}$ High Time	100			ns
t_{CSS}	$\overline{CS}$ Setup Time	10			ns
t_{CSH}	$\overline{CS}$ Hold Time	10			ns
t_{DS}	Data In Setup Time	4			ns
t_{DH}	Data In Hold Time	4			ns
t_{HS}	$\overline{HOLD}$ Setup Time	30			ns
t_{HD}	$\overline{HOLD}$ Hold Time	30			ns
t_{OV}	Output Valid			6.5	ns
t_{OH}	Output Hold Time Normal Mode	0			ns
t_{LZ}	$\overline{HOLD}$ to output Low Z	0		200	ns
t_{HZ}	$\overline{HOLD}$ to output High Z			200	ns
t_{DIS}	Output Disable Time			100	ns
t_{PW}	Page Write Cycle Time		1	3	ms
t_{BP}	Byte Write Cycle Time		25	100	µs
t_{PUD}	V_{cc} Power-up Delay(1)			75	µs
t_{RPD}	Return from Power-Down Time	50			µs
C_{IN}	SCK, SDI, $\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$ V_{IN}=0V			6	pf
C_{OUT}	SDO V_{IN}=0V			8	pf
Endurance		100			Write Cycles
Retention	70°C	10			Years

Notes: 1. VCC must be within operating range.

3.3 AC Test Conditions

AC Waveform	Timing Measurement Reference Level	
VLO = 0.2V	Input Output	0.5 V_{cc} 0.5 V_{cc}
VHI = 3.4V		
CL = 30pF (for 1.6MHz SCK)		
CL = 10pF (for 5MHz SCK)		

4. Timing Diagrams

Figure 4-1. Synchronous Data Timing with HOLD high

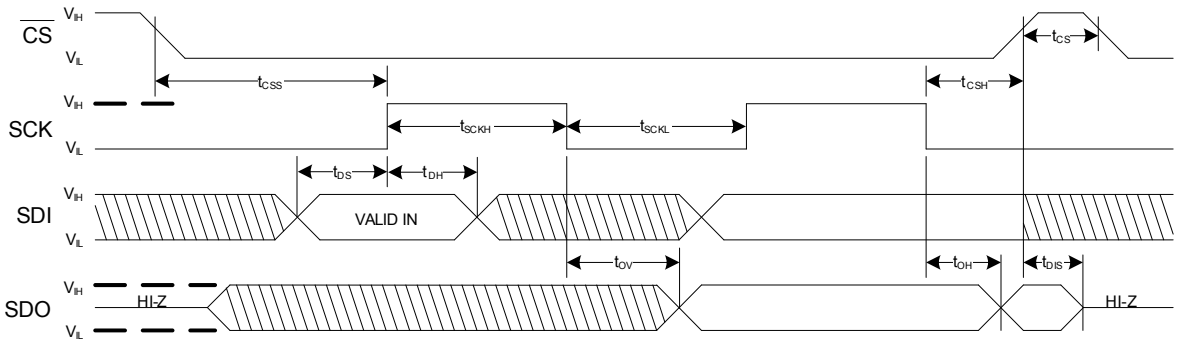


Figure 4-2. Hold Timing

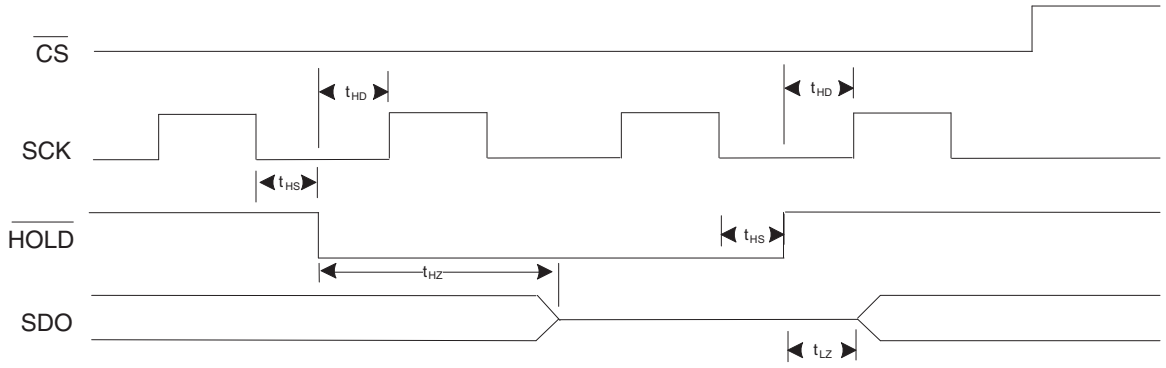
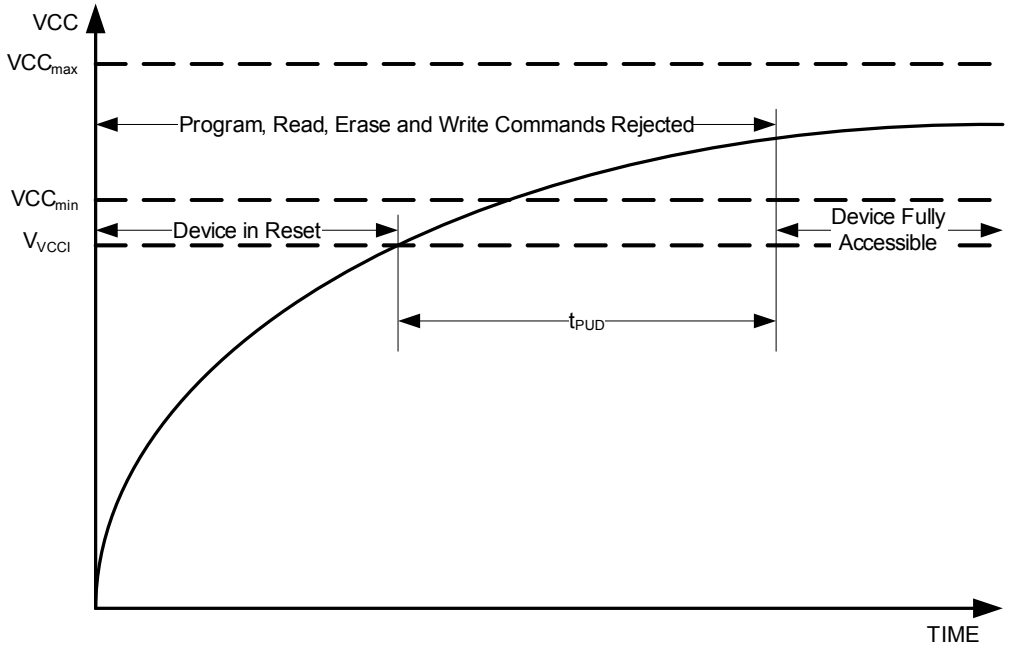


Figure 4-3. Power-up Timing

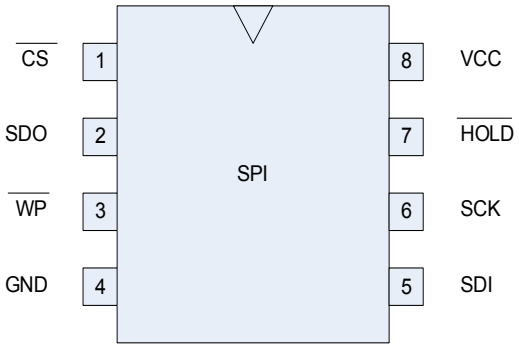


5. Pin Descriptions and Pin-out

Table 5-1. Pin Descriptions

Mnemonic	Pin Number	Pin Name	Description
$\overline{CS}$	1	Chip Select	Making $\overline{CS}$ low activates the internal circuitry for device operation. Making $\overline{CS}$ high deselects the device and switches into standby mode to reduce power. When the device is not selected ($\overline{CS}$ high), data is not accepted via the Serial Data Input pin (SDI) and the Serial Data Output pin (SDO) remains in a high-impedance state.
SDO	2	Serial Data Out	Sends read data or status on the falling edge of SCK.
$\overline{WP}$	3	Write Protect	N/A
GND	4	Ground	
SDI	5	Serial Data In	Device data input; accepts commands, addresses, and data on the rising edge of SCK.
SCK	6	Serial Clock	Provides timing for the SPI interface. SPI commands, addresses, and data are latched on the rising edge on the Serial Clock signal, and output data is shifted out on the falling edge of the Serial Clock signal.
$\overline{HOLD}$	7	Hold	When pulled low, serial communication with the master device is paused, without resetting the serial sequence.
V_{cc}	8	Power	Power supply pin.

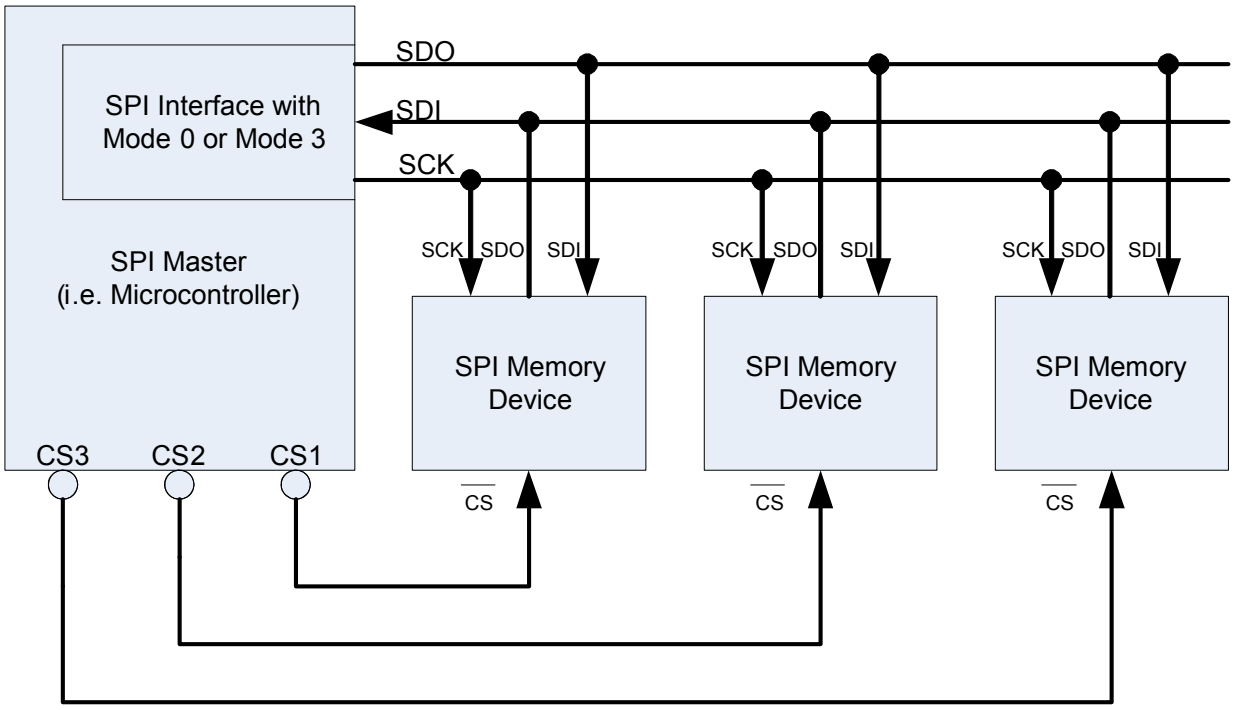
Figure 5-1. Pin Out



6. SPI Modes Description

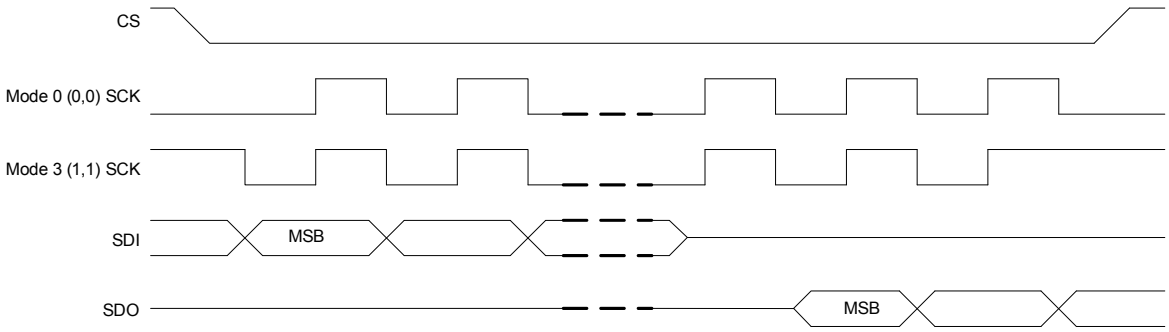
Multiple Adesto SPI devices can be connected onto a Serial Peripheral Interface (SPI) serial bus controlled by an SPI master, such as a microcontroller, as shown in Figure 6-1,

Figure 6-1. Connection Diagram, SPI Master and SPI Slaves



The Adesto RM25C128A supports two SPI modes: Mode 0 (0, 0) and Mode 3 (1, 1). The difference between these two modes is the clock polarity when the SPI master is in standby mode ($\overline{CS}$ high). In Mode 0, the Serial Clock (SCK) stays at 0 during standby. In Mode 3, the SCK stays at 1 during standby. An example sequence for the two SPI modes is shown in Figure 6-2. For both modes, input data (on SDI) is latched in on the rising edge of Serial Clock (SCK), and output data (SDO) is available beginning with the falling edge of Serial Clock (SCK).

Figure 6-2. SPI Modes



7. Registers

7.1 Instruction Register

The Adesto RM25C128A uses a single 8-bit instruction register. The instructions and their operation codes are listed in Table 7.1. All instructions, addresses, and data are transferred with the MSB first, and begin transferring with the first low-to-high SCK transition after the $\overline{CS}$ pin goes low.

Table 7-1. Device Operating Instructions

Instruction	Description	Operation Code	Address Cycles	Dummy Cycles	Data Cycles
WR	Write 1 to 64 bytes	02H	2	0	1-64
READ	Read data from memory array	03H	2	0	1 to ∞
FREAD	Fast Read data from data memory	0BH	2	1	1 to ∞
WRDI	Write Disable	04H	0	0	0
RDSR	Read Status Register	05H	0	0	1 to ∞
WREN	Write Enable	06H	0	0	0
PERS	Page Erase 64 bytes	42H	2	0	0
CERS	Chip Erase	60H	0	0	0
		C7H	0	0	0
PD	Power Down	B9H	0	0	0
RES	Resume from Power Down	ABH	0	0	0

7.2 Status Register

The Adesto RM25C128A uses a single 8-bit Status Register. The Write In Progress (WIP) and Write Enable (WEL) status of the device can be determined by reading this register.

The Status Register format is shown in Table 7-2 The Status Register bit definitions are shown in Table 7-3.

Table 7-2. Status Register Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	WEL	WIP

Table 7-3. Status Register Bit Definitions

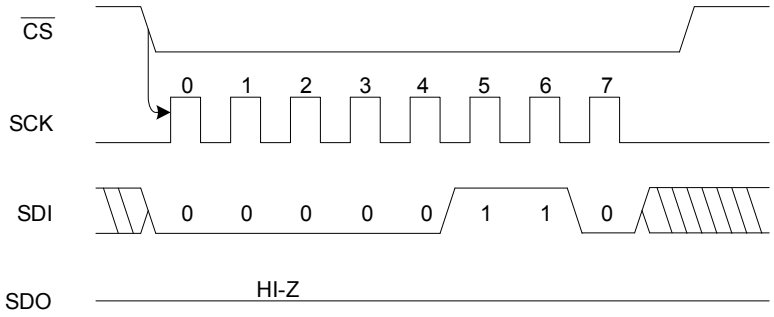
Bit	Name	Description	R/W	Non-Volatile Bit
0	WIP	**Write In Progress** “0” indicates the device is ready “1” indicates that the program/erase cycle is in progress and the device is busy	R	No
1	WEL	**Write Enable Latch** “0” Indicates that the device is disabled “1” indicates that the device is enabled	R/W	No
2	N/A	Reserved. Read as “0”	N/A	No
3	N/A			
4	N/A			
5	N/A	Reserved. Read as “0”	N/A	No
6	N/A	Reserved. Read as “0”	N/A	No
7	N/A	Reserved. Read as “0”	N/A	No

8. Command Descriptions

8.1 WREN (Write Enable):

The device powers up with the Write Enable Latch set to zero. This means that no write or erase instructions can be executed until the Write Enable Latch is set using the Write Enable (WREN) instruction. The Write Enable Latch is also set to zero automatically after any non-read instruction. Therefore, all page programming instructions and erase instructions must be preceded by a Write Enable (WREN) instruction. The sequence for the Write Enable instruction is shown in Figure 8-1.

Figure 8-1. WREN Sequence



The following table is a list of actions that will automatically set the Write Enable Latch to zero when successfully executed. If an instruction is not successfully executed, for example if the $\overline{CS}$ pin is brought high before an integer multiple of 8 bits is clocked, the Write Enable Latch will not be reset.

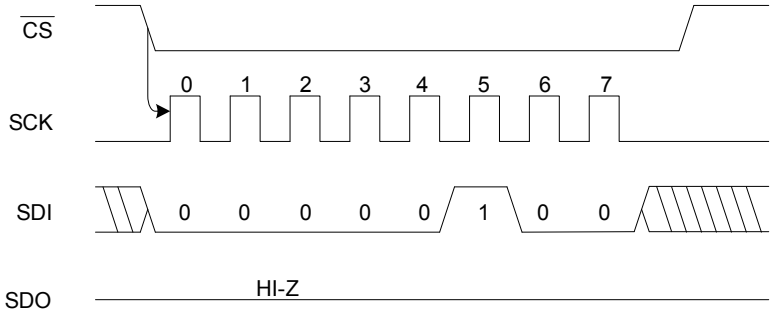
Table 8-1. Write Enable Latch to Zero

Instruction/Operation
Power-Up
WRDI (Write Disable)
WR (Write)
PERS (Page Erase)
CERS (Chip Erase)
PD (Power Down)

8.2 WRDI (Write Disable):

To protect the device against inadvertent writes, the Write Disable instruction disables all write modes. Since the Write Enable Latch is automatically reset after each successful write instruction, it is not necessary to issue a WRDI instruction following a write instruction. The WRDI instruction is independent of the status of the WP pin. The WRDI sequence is shown in Figure 8-2.

Figure 8-2. WRDI Sequence



8.3 RDSR (Read Status Register):

The Read Status Register instruction provides access to the Status Register and indication of write protection status of the memory.

Caution: The Write In Progress (WIP) and Write Enable Latch (WEL) indicate the status of the device. The RDSR sequence is shown in Figure 8-3. (Note: The Write Status Register command is not available in this device, and should not be used. Use of this command may cause unexpected behavior.)

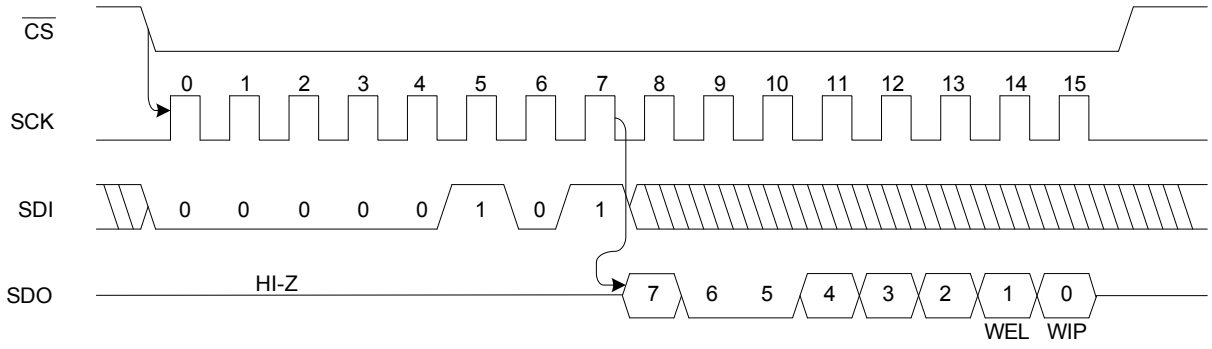


Figure 8-3. RDSR Sequence

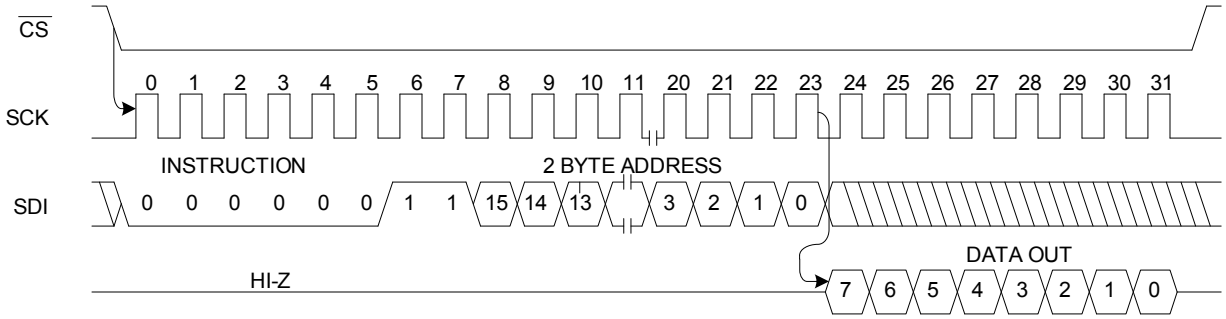
8.4 READ (Read Data):

Reading the Adesto RM25C128A via the Serial Data Output (SDO) pin requires the following sequence: First the $\overline{CS}$ line is pulled low to select the device; then the READ op-code is transmitted via the SDI line, followed by the address to be read (A15-A0). Although not all 16 address bits are used, a full 2 bytes of address must be transmitted to the device. For the 128Kbit device, only address A0 to A13 are used; the rest are don't cares and must be set to "0".

Once the read instruction and address have been sent, any further data on the SDI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SDO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the byte of data comes out. This completes the reading of one byte of data.

The READ sequence can be automatically continued by keeping the $\overline{CS}$ low. At the end of the first data byte the byte address is internally incremented and the next higher address data byte will be shifted out. When the highest address is reached, the address counter will roll over to the lowest address (00000), thus allowing the entire memory to be read in one continuous read cycle. The READ sequence is shown in Figure 8-4.

Figure 8-4. Single Byte READ Sequence



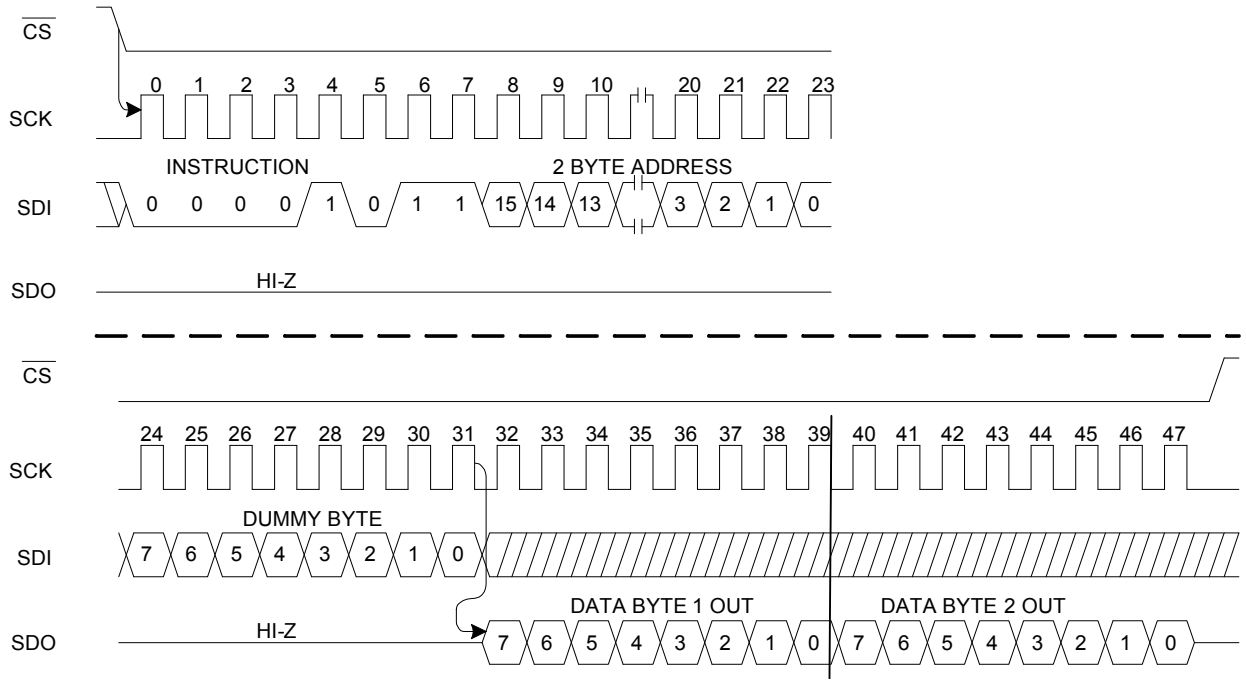
8.5 FREAD (Fast Read Data):

The Adesto RM25C128A also includes the Fast Read Data command, which facilitates reading memory data at higher clock rates, up to 5MHz. After the $\overline{CS}$ line is pulled low to select the device, the FREAD op-code is transmitted via the SDI line. This is followed by the 2-byte address to be read (A15-A0) and then a 1-byte dummy. For the 128Kbit device, only address A0 to A13 are used; the rest are don't cares and must be set to "0".

The next 8 bits transmitted on the SDI are dummy bits. The data (D7-D0) at the specified address is then shifted out onto the SDO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. This completes the reading of one byte of data.

The FREAD sequence can be automatically continued by keeping the $\overline{CS}$ low. At the end of the first data byte, the byte address is internally incremented and the next higher address data byte is then shifted out. When the highest address is reached, the address counter rolls over to the lowest address (00000), allowing the entire memory to be read in one continuous read cycle. The FREAD sequence is shown in Figure 8-5.

Figure 8-5. Two Byte FREAD Sequence



8.6 WRITE (WR):

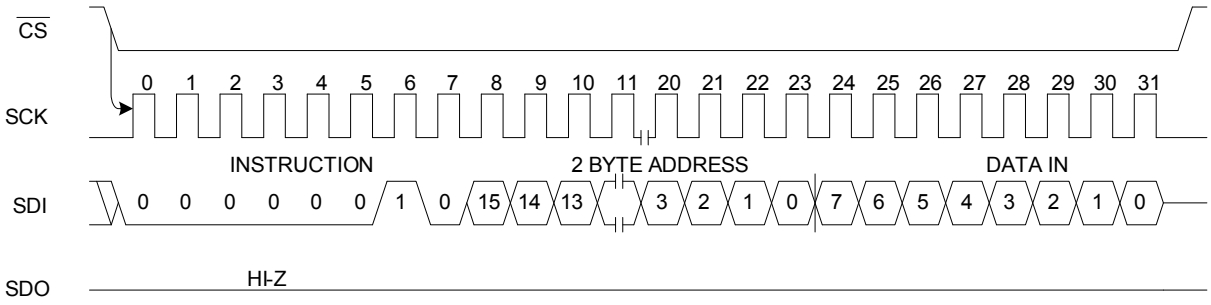
Product	Density	Page Size (byte)
RM25C128A	**128 Kbit**	**64**

The Write (WR) instruction allows bytes to be written to the memory. But first, the device must be write-enabled via the WREN instruction. The $\overline{CS}$ pin must be brought high after completion of the WREN instruction; then the $\overline{CS}$ pin can be brought back low to start the WR instruction. The $\overline{CS}$ pin going high at the end of the WR input sequence initiates the internal write cycle. During the internal write cycle, all commands except the RDSR instruction are ignored.

A WR instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WR op-code is transmitted via the SDI line, followed by the byte address (A15-A0) and the data (D7-D0) to be written. The internal write cycle sequence will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The Write In Progress status of the device can be determined by initiating a Read Status Register (RDSR) instruction and monitoring the WIP bit. If the WIP bit (Bit 0) is a “1”, the write cycle is still in progress. If the WIP bit is “0”, the write cycle has ended. Only the RDSR instruction is enabled during the write cycle. The sequence of a one-byte WR is shown in Figure 8-6.

Figure 8-6. One Byte Write Sequence



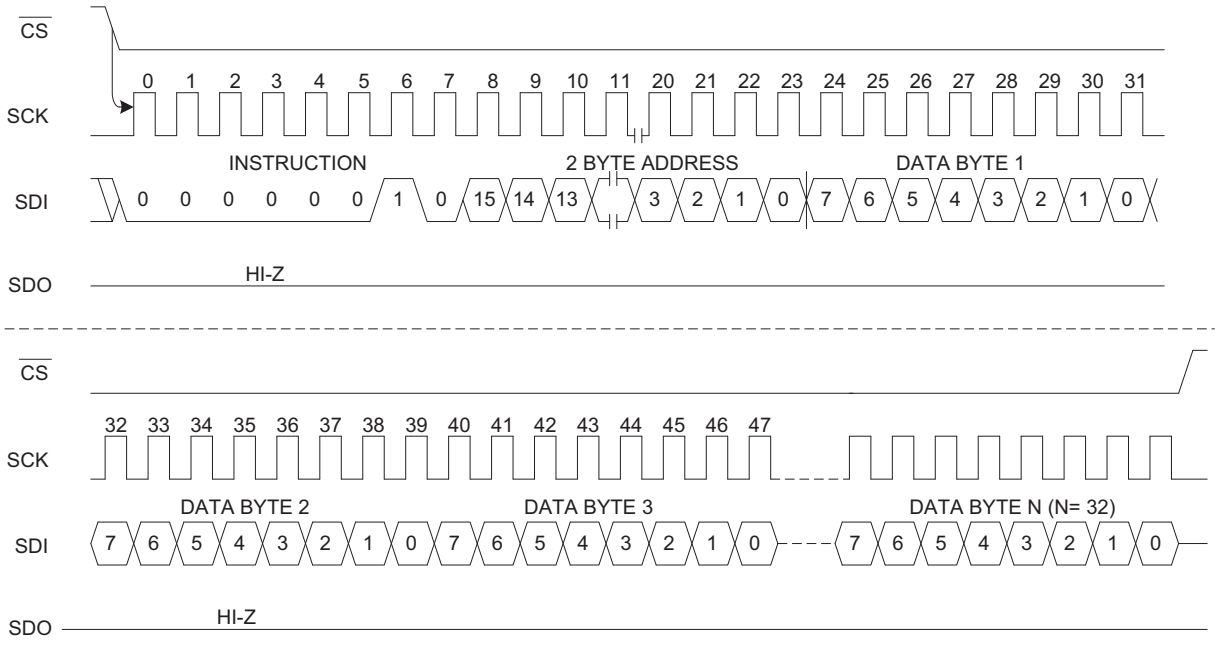
The Adesto RM25C128A is capable of a 64-byte write operation.

For the RM25C128A: After each byte of data is received, the six low-order address bits (A5-A0) are internally incremented by one; the high-order bits of the address will remain constant. All transmitted data that goes beyond the end of the current page are written from the start address of the same page (from the address whose 6 least significant bits [A5-A0] are all zero). If more than 64 bytes are sent to the device, previously latched data are discarded and the last 64 data bytes are ensured to be written correctly within the same page. If less than 64 data bytes are sent to the device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

The Adesto RM25C128A is automatically returned to the write disable state at the completion of a program cycle. The sequence for a 64 byte WR is shown in Figure 8-7. Note that the Multi-Byte Write operation is internally executed by sequentially writing the words in the Page Buffer.

NOTE: If the device is not write enabled (WREN) previous to the Write instruction, the device will ignore the write instruction and return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to reinitiate the serial communication.

Figure 8-7. WRITE Sequence



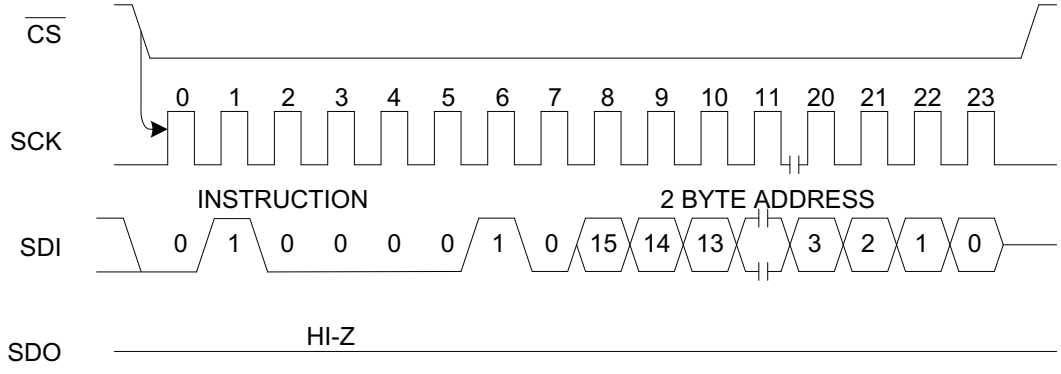
8.7 PER (Page Erase 32/64 bytes):

Page Erase sets all bits inside the addressed 32/64-byte page to a 1. A Write Enable (WREN) instruction is required prior to a Page Erase. After the WREN instruction is shifted in, the $\overline{CS}$ pin must be brought high to set the Write Enable Latch.

The Page Erase sequence is initiated by bringing the $\overline{CS}$ pin low; this is followed by the instruction code, then 2 address bytes. Any address inside the page to be erased is valid. This means the bottom five/six bits (A4-A0)/(A5-A0) of the address are ignored. Once the address is shifted in, the $\overline{CS}$ pin is brought high, which initiates the self-timed Page Erase function. The WIP bit in the Status Register can be read, using the RDSR instruction, to determine when the Page Erase cycle is complete.

The sequence for the PER is shown in Figure 8-8.

Figure 8-8. PERS Sequence



8.8 CER (Chip Erase):

Chip Erase sets all bits inside the device to a 1. A Write Enable (WREN) instruction is required prior to a Chip Erase. After the WREN instruction is shifted in, the $\overline{CS}$ pin must be brought high to set the Write Enable Latch.

The Chip Erase sequence is initiated by bringing the $\overline{CS}$ pin low; this is followed by the instruction code. There are two different instruction codes for CER, 60h and C7h. Either instruction code will initiate the Chip Erase sequence. No address bytes are needed. Once the instruction code is shifted in, the $\overline{CS}$ pin is brought high, which initiates the self-timed Chip Erase function. The WIP bit in the Status Register can be read, using the RDSR instruction, to determine when the Chip Erase cycle is complete.

The sequence for the 60h CER instruction is shown in Figure 8-9. The sequence for the C7h CER instruction is shown in Figure 8-10.

Figure 8-9. CERS Sequence (60h)

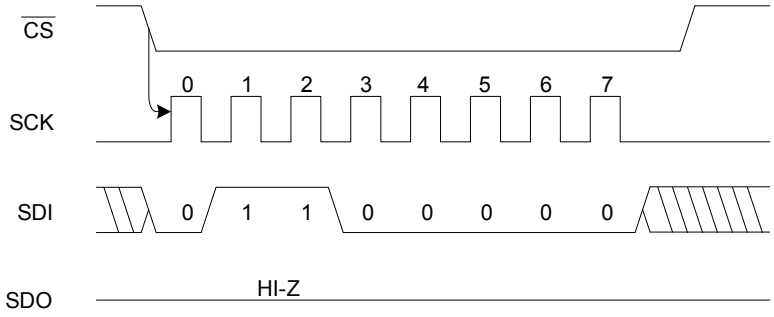
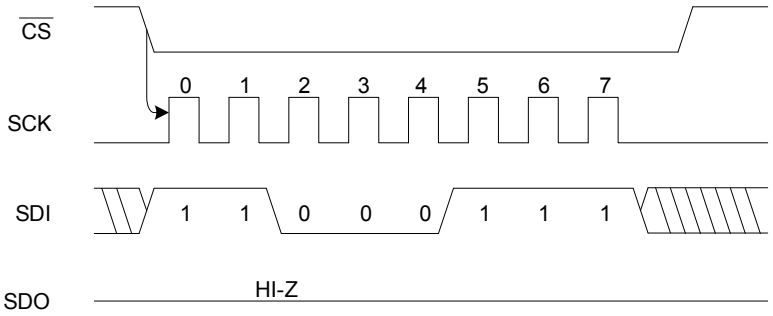


Figure 8-10. CERS Sequence (C7h)



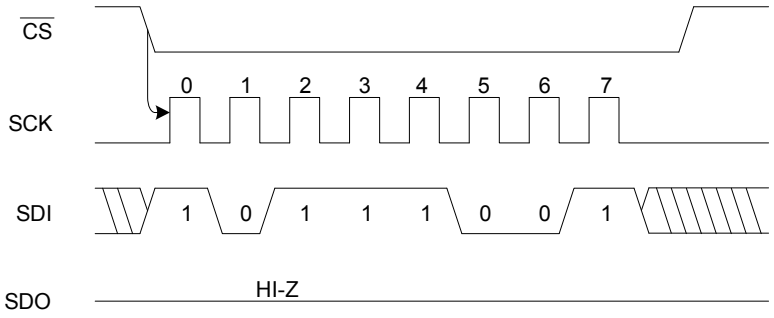
8.9 PD (Power Down):

Power Down mode allows the user to reduce the power of the device to its lowest power consumption state.

All instructions given during the Power Down mode are ignored except the Resume from Power down (RES) instruction. Therefore this mode can be used as an additional software write protection feature.

The Power Down sequence is initiated by bringing the $\overline{CS}$ pin low; this is followed by the instruction code. Once the instruction code is shifted in the $\overline{CS}$ pin is brought high, which initiates the PD mode. The sequence for PD is shown in Figure 8-11.

Figure 8-11. PD Sequence



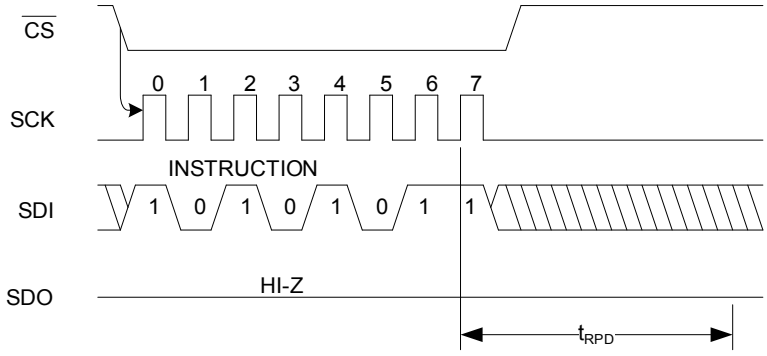
8.10 RES (Resume from Power Down):

The Resume from Power Down mode is the only command that will wake the device up from the Power Down mode. All other commands are ignored.

In the simple instruction command, after the $\overline{CS}$ pin is brought low, the RES instruction is shifted in. At the end of the instruction, the $\overline{CS}$ pin is brought back high.

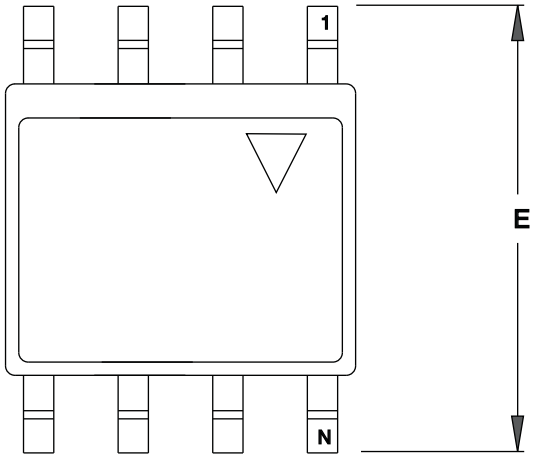
The rising edge of the SCK clock number 7 (8^{th} rising edge) initiates the internal RES instruction. The device becomes available for Read and Write instructions 75µS after the 8^{th} rising edge of the SCK (t_{PUD}, see AC Characteristics). The sequence for simple RES instruction is shown in Figure 8-12.

Figure 8-12. Simple RES Sequence

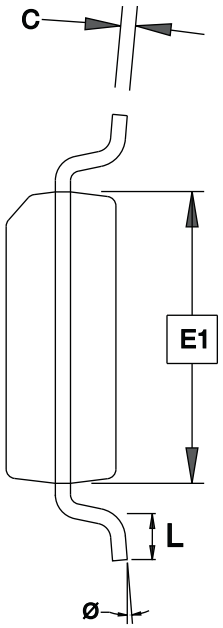


9. Package Information

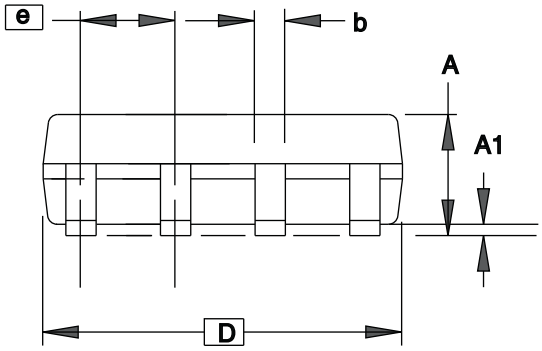
9.1 SN (JEDEC SOIC)



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

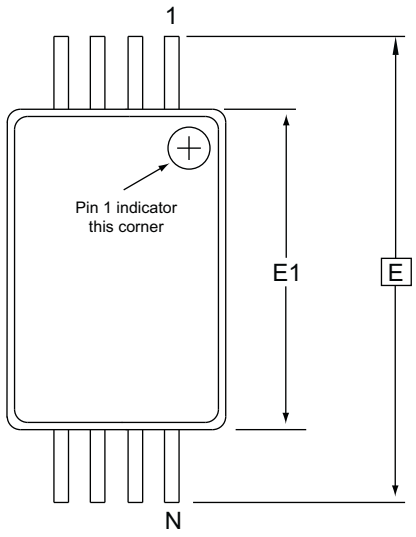
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
ø	0°	–	8°	

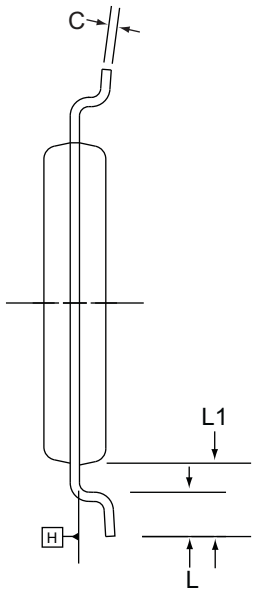
8/20/14

adesto™ TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE 8S1, 8-lead (0.150"Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

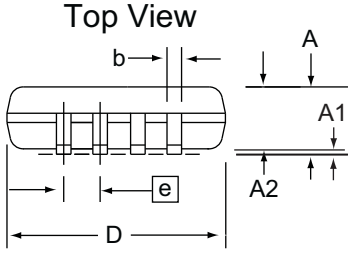
9.2 TA-TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

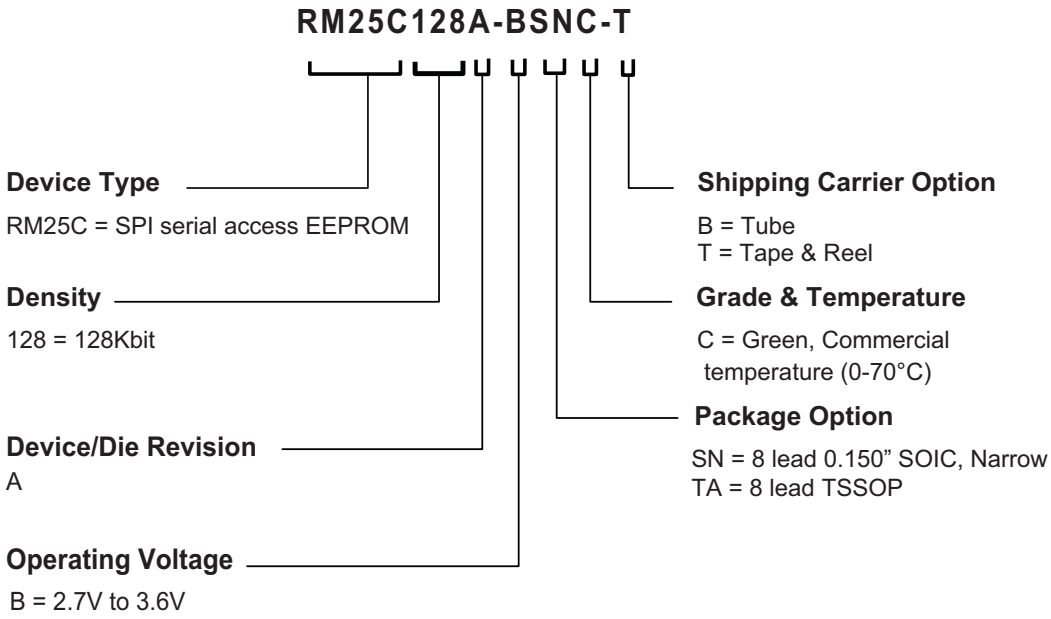
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

12/8/11

adesto TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE TA, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

10. Ordering Information

10.1 Ordering Detail



10.2 Ordering Codes

Ordering Code	Package	Density	Operating Voltage	f_{SCKF}	Device Grade	Ship Carrier	Qty. Carrier
RM25C128A-BSNC-B	SN	128 Kbit	2.7V to 3.6V	5MHz	Commercial (0°C to 70°C)	Tube	100
RM25C128A-BSNC-T						Reel	4000
RM25C128A-BTAC-B	TA	128 Kbit	2.7V to 3.6V	5MHz	Commercial (0°C to 70°C)	Tube	100
RM25C128A-BTAC-T						Reel	6000

Package Type	
SN	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
TA	8-lead 3 x 4.4 mm, Thin Shrink Small Outline Package

11. Revision History

Doc. Rev.	Date	Comments
RM25C128A-065A	10/2014	Initial document release.
RM25C128A-065B	1/2015	Updated document index and formatting.

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