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FAIRCHILD SEMICONDUCTOR®

September 2004

RMPA2259

28dBm WCDMA PowerEdge™ Power Amplifier Module

General Description

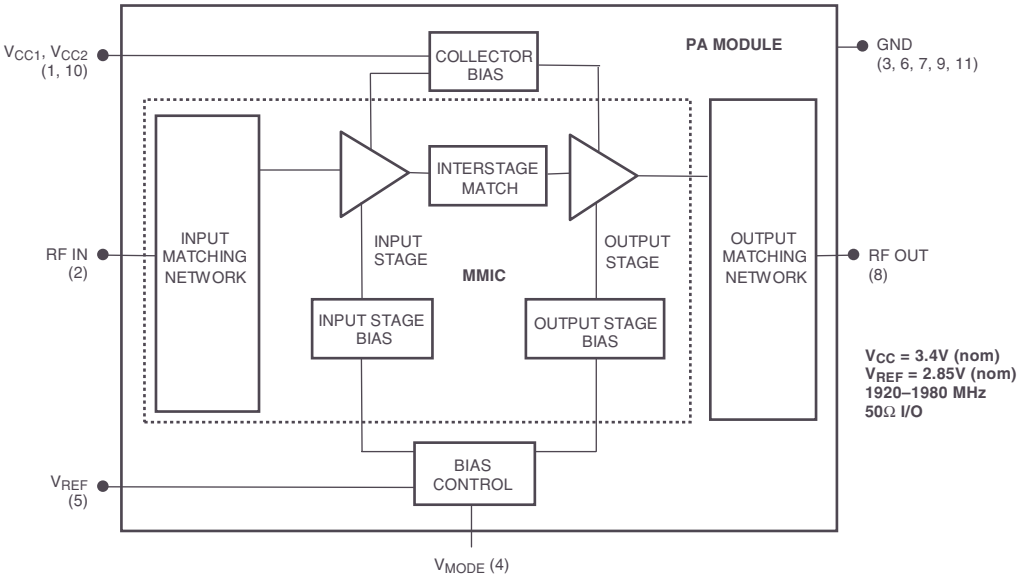
The RMPA2259 power amplifier module (PAM) is designed for WCDMA applications. The 2 stage PAM is internally matched to 50Ω to minimize the use of external components and features a low power mode to reduce standby current and DC power consumption during peak phone usage. High power-added efficiency and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) process.

Features

- Single positive-supply operation with low power and shutdown modes
- 40% linear efficiency at +28dBm average output power
- Compact LCC package – 4.0 x 4.0 x 1.5mm
- Internally matched to 50Ω and DC blocked RF input/output.
- High-Power/Low-Power operating modes for extended battery life

Device

Module Block Diagram



Absolute Ratings [1]

Symbol	Parameter	Ratings	Units
V_{CC1}, V_{CC2}	Supply Voltage	5.0	V
V_{REF}	Reference Voltage	2.6 to 3.5	V
V_{MODE}	Power Control Voltage	3.5	V
P_{IN}	RF Input Power	+10	dBm
T_{STG}	Storage Temperature Range	-55 to +150	°C

Note:
1: No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.

Electrical Characteristics[1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
f	Operating Frequency		1920		1980	MHz
WCDMA Operation						
SSg	Small-Signal Gain	Po = 0dBm		24		dB
Gp	Power Gain	Po = +28dBm, Vmode = 0V		26.5		dB
		Po = +16dBm, Vmode ≥ 2.0V		24		dB
Po	Linear Output Power	Vmode = 0V	28			dBm
		Vmode ≥ 2.0V	16			dBm
PAEd	PAE (digital) @ +28dBM	Vmode = 0V		40		%
	PAE (digital) @ +16dBM	Vmode ≥ 2.0V		9		%
	PAEd (digital) @ +16dBM	Vmode ≥ 2.0V, Vcc = 1.4V		20		%
Itot	High Power Total Current	Po = +28dBm, Vmode = 0V		450		mA
	Low Power Total Current	Po = +16dBm, Vmode = 2.0V		130		mA
	Adjacent Channel Leakage Ratio	3GPP 3.2 03-00 DPCCH + 1 DPDCH				
ACLR1	±5.0MHz Offset	Po = +28dBm, Vmode = 0V		-40		dBc
		Po = +16dBm, Vmode ≥ 2.0V		-43		dBc
ACLR2	±10.0MHz Offset	Po = +28dBm, Vmode = 0V		-53		dBc
		Po = +16dBm, Vmode ≥ 2.0V		-66		dBc
General Characteristics						
VSWR	Input Impedance			2.0:1		
NF	Noise Figure			3		dB
Rx No	Receive Band Noise Power	Po ≤ +28dBm, 1920 to 1980 MHz		-139		dBm/Hz
2fo-5fo	Harmonic Suppression	Po ≤ +28dBm			-30	dBc
S	Spurious Outputs[2, 3]	Load VSWR ≤ 5.0:1			-60	dBc
	Ruggedness with Load Mismatch[3]	No permanent damage			10:1	
Tc	Case Operating Temperature		-30		85	°C
DC Characteristics						
Iccq	Quiescent Current	Vmode ≥ 2.0V		50		mA
Iref	Reference Current	Po ≤ +28dBm		5	8	mA
Icc(off)	Shutdown Leakage Current	No applied RF signal		1	5	µA

Notes:
1: All parameters met at T_C = +25°C, V_{CC} = +3.4V, f = 1950MHz and load VSWR ≤ 1.2:1.
2: All phase angles
3: Guaranteed by design

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
f	Operating Frequency	1920		1980	MHz
V_{CC1}, V_{CC2}	Supply Voltage	3.0	3.4	4.2	V
V_{REF}	Reference Voltage				
	Operating	2.7	2.85	3.1	V
	Shutdown	0		0.5	V
V_{MODE}	Bias Control Voltage				
	Low-Power	1.8	2.0	3.0	V
	High-Power	0		0.5	V
P_{OUT}	Linear Output Power				
	High-Power			+28	dBm
	Low-Power			+16	dBm
T_C	Case Operating Temperature	-30		+85	°C

Note:
1: RF input power for WCDMA P_{OUT} = +28dBm.

Typical Characteristics

High-Power Mode (Vmode = 0V)

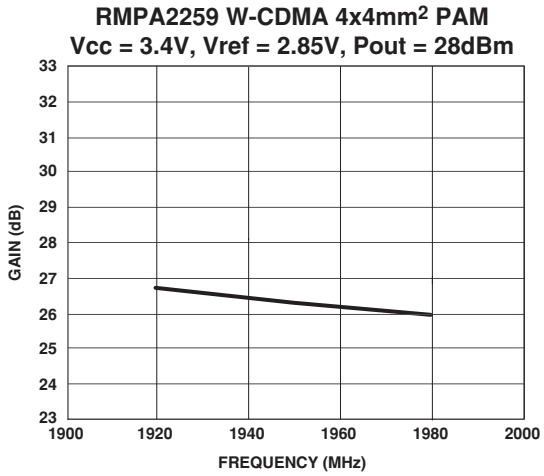


Figure 1.

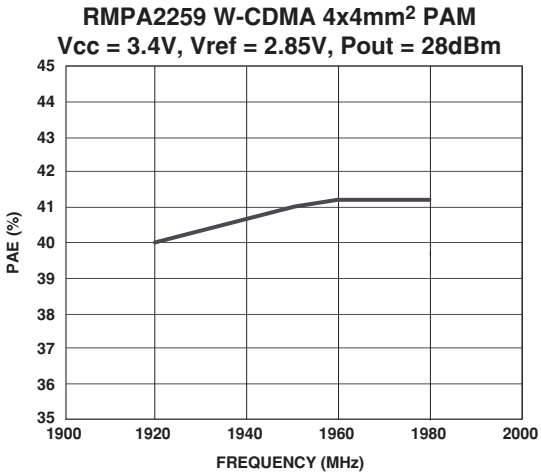


Figure 2.

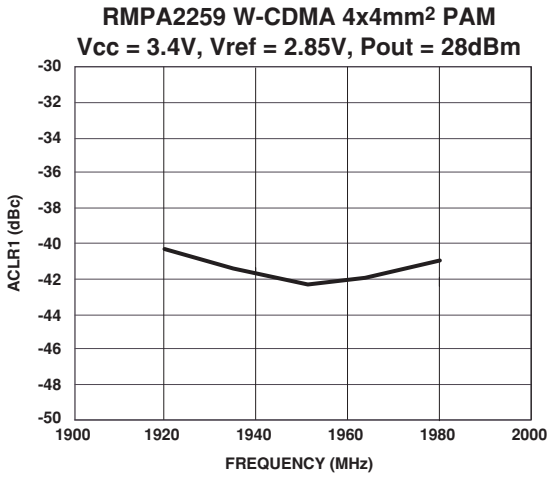


Figure 3.

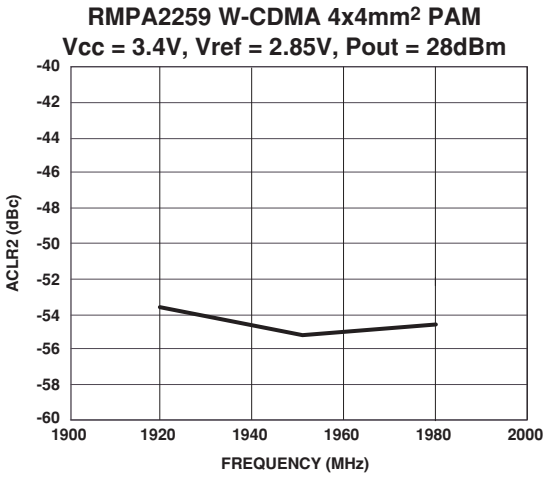


Figure 4.

Efficiency Improvement Application

In addition to high-power/low-power bias modes, the efficiency of the PA module can be significantly increased at backed-off RF power levels by dynamically varying the supply voltage (Vcc) applied to the amplifier. Since mobile handsets and power amplifiers frequently operate at 10–20dB back-off, or more, from maximum rated linear power, battery life is highly dependent on the DC power consumed at antenna power levels in the range of 0 to +16dBm. The reduced demand on transmitted RF power allows the PA supply voltage to be reduced for improved efficiency, while still meeting linearity requirements for CDMA modulation with excellent margin. High-efficiency DC-DC converters are now available to implement switched-voltage operation.

The following charts show measured performance of the PA module in low-power mode (Vmode = +2.0V) at +16dBm output power and over a range of supply voltages from 3.4V nominal to 1.2V. Power-added efficiency is more than doubled from 9.5 percent to nearly 25 percent (Vcc = 1.2V) while maintaining a typical ACLR1 of -46dBc and ACLR2 of approximately -60dBc.

Operation at even lower levels of Vcc supply voltage are possible with a further restriction on the maximum RF output power. As shown below, the PA module can be biased at a supply voltage of as low as 0.7V with an efficiency as high as 10–12 percent at +8dBm output power. Excellent signal linearity is still maintained even under this low supply voltage condition.

Typical Characteristics (continued)

Low-Power Mode (Po = +16dBm)

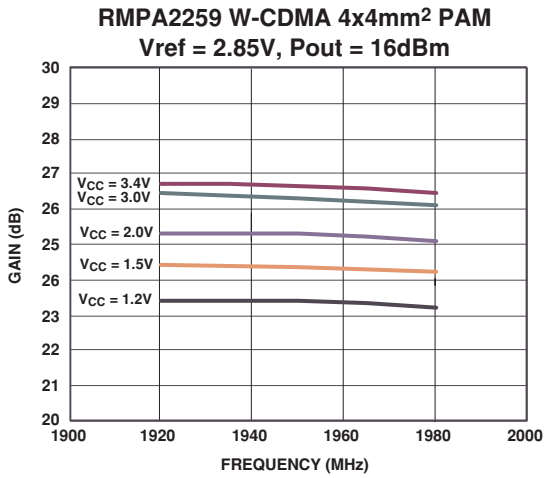


Figure 5.

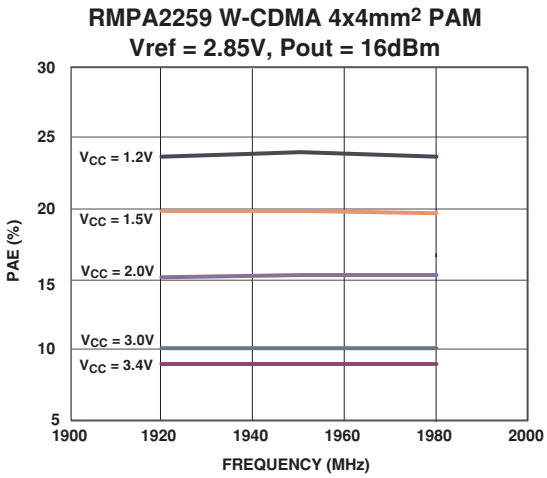


Figure 6.

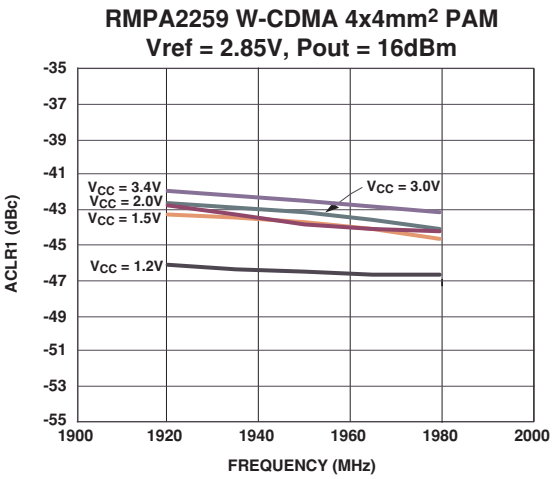


Figure 7.

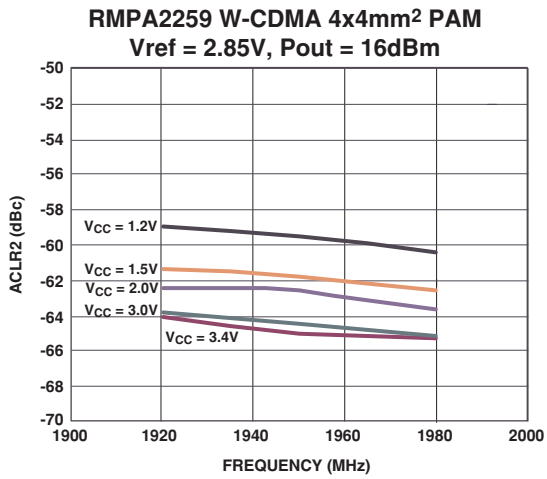


Figure 8.

Typical Characteristics (continued)

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 16dBm, Freq = 1.95GHz

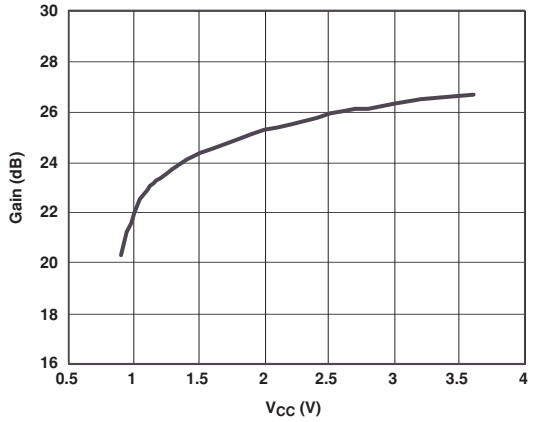


Figure 9.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 16dBm, Freq = 1.95GHz

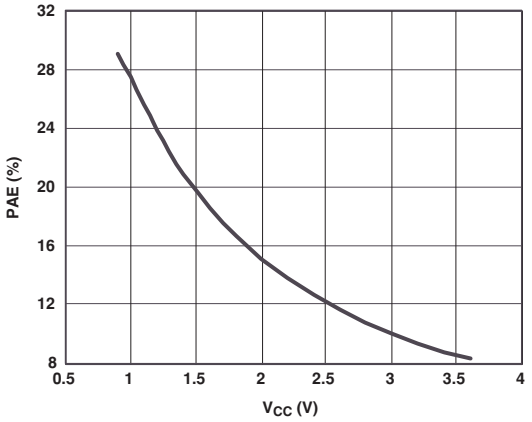


Figure 10.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 16dBm, Freq = 1.95GHz

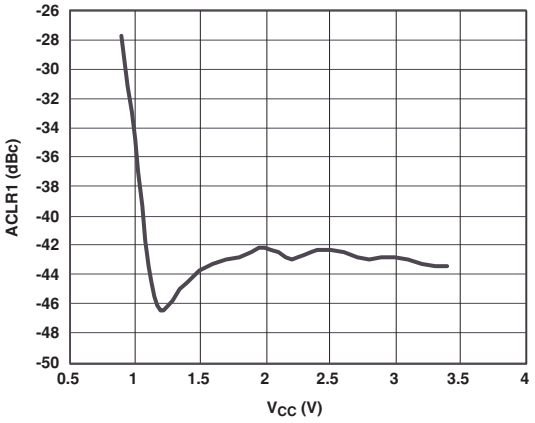


Figure 11.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 16dBm, Freq = 1.95GHz

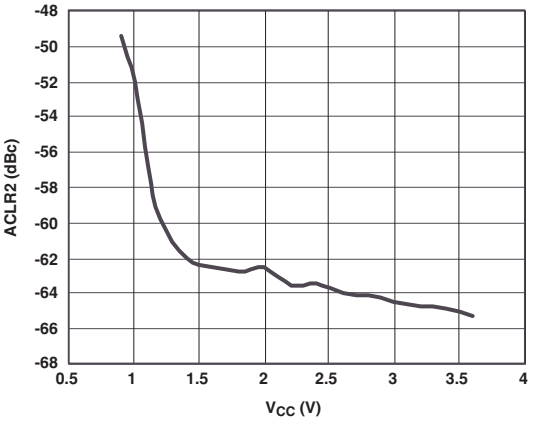


Figure 12.

Typical Characteristics (continued)

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 12dBm, Freq = 1.95GHz

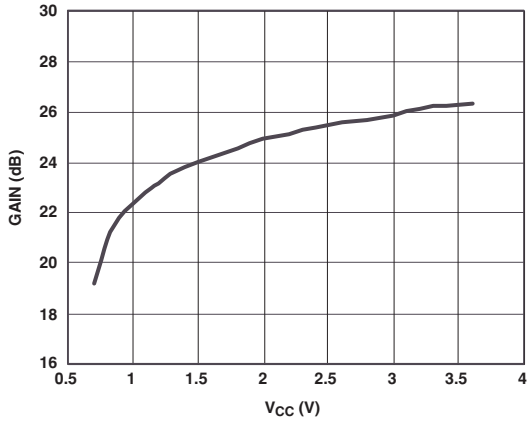


Figure 13.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 12dBm, Freq = 1.95GHz

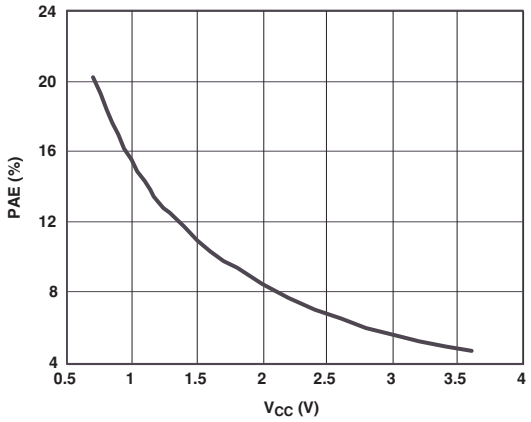


Figure 14.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 12dBm, Freq = 1.95GHz

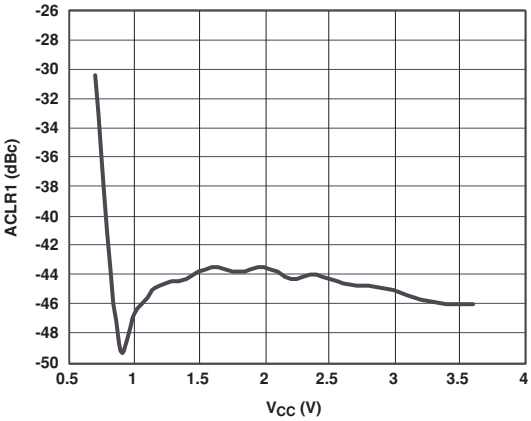


Figure 15.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 12dBm, Freq = 1.95GHz

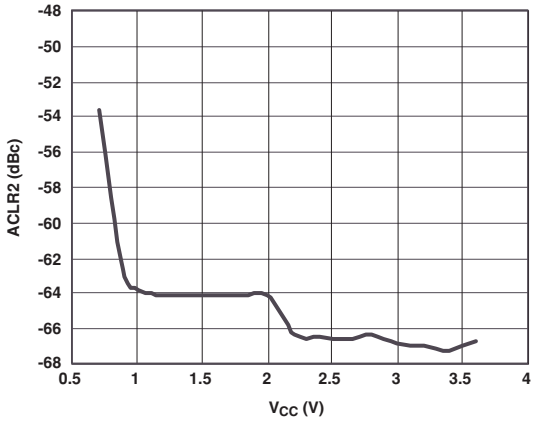


Figure 16.

Typical Characteristics (continued)

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 8dBm, Freq = 1.95GHz

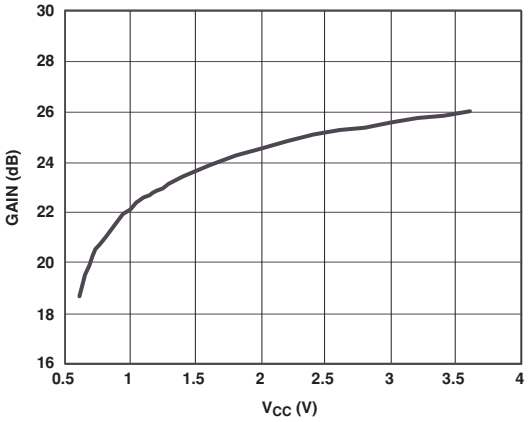


Figure 17.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 8dBm, Freq = 1.95GHz

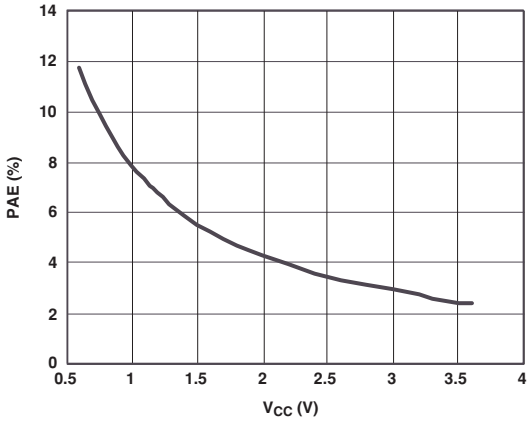


Figure 18.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 8dBm, Freq = 1.95GHz

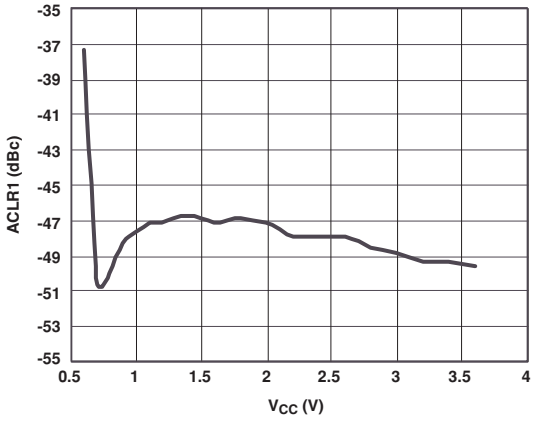


Figure 19.

RMPA2259 W-CDMA 4x4mm² PAM
Vref = 2.85V, Pout = 8dBm, Freq = 1.95GHz

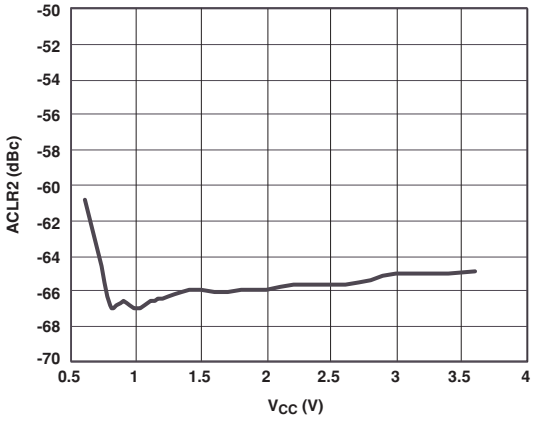


Figure 20.

Applications Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC and ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, and ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
- Assemble the dry-baked devices within 7 days of removal from the oven.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.

Solder Materials & Temperature Profile:
Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

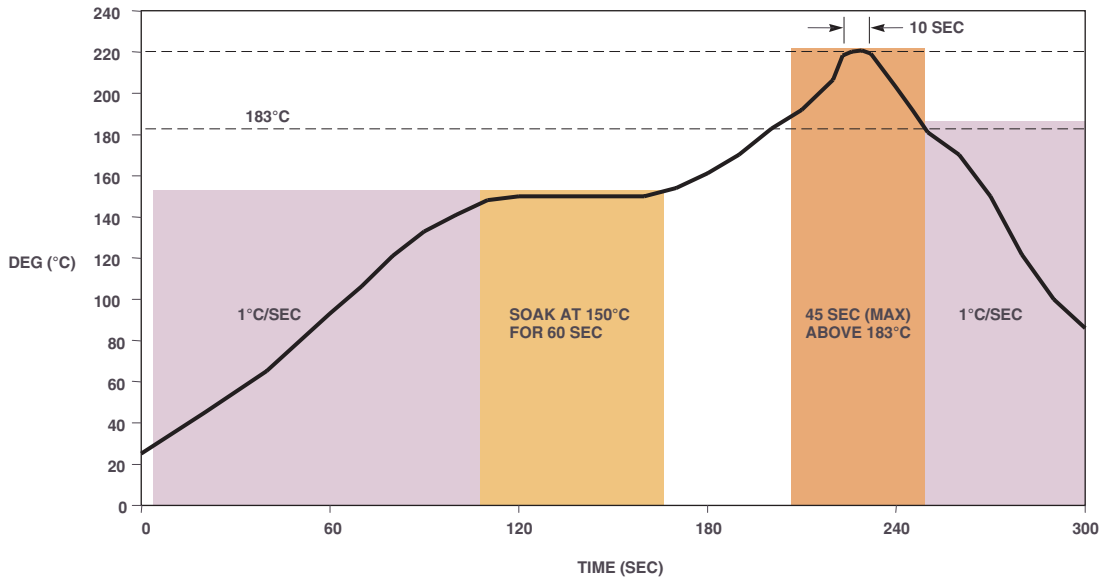
Reflow Profile

- Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1- 2°C/sec.
- Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120–150 seconds at 150°C.
- Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215–220°C, with a maximum limit of 225°C.
- Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

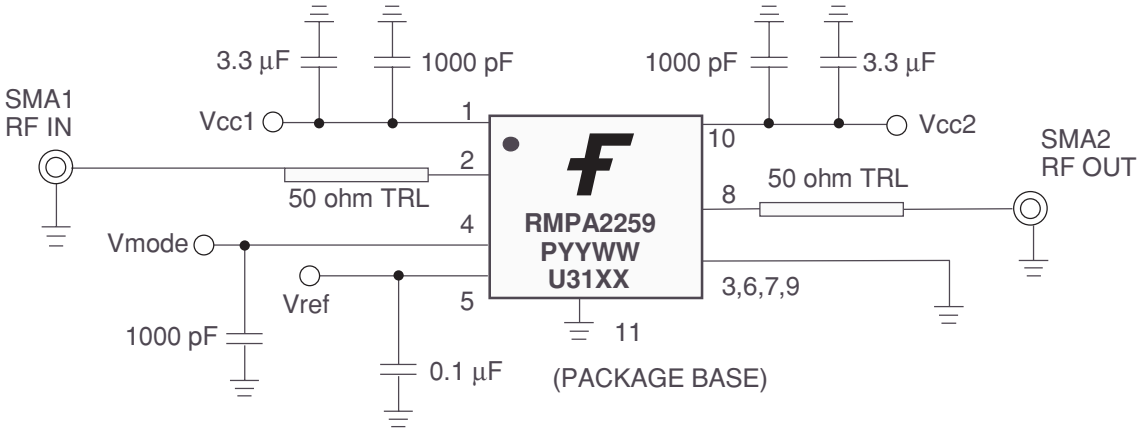
Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heat sink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

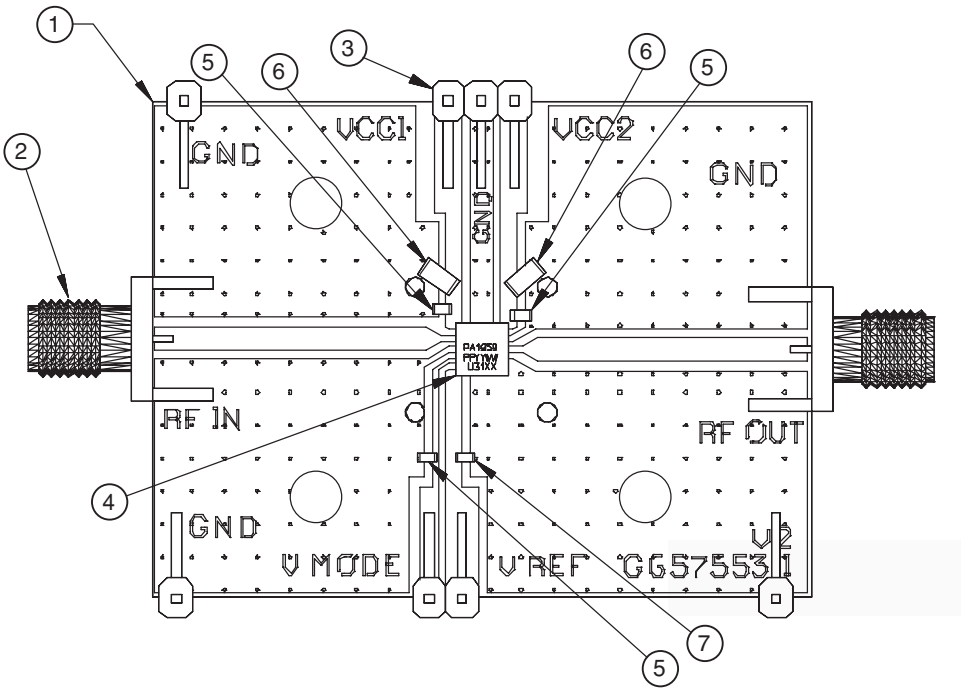
Recommended Solder Reflow Profile



Evaluation Board Schematic



Evaluation Board Layout



Materials List

Qty	Item No.	Part Number	Description	Vendor
1	1	G657553-1 V2	PC Board	Fairchild
2	2	#142-0701-841	SMA Connector	Johnson
3	3	#2340-5211TN	Terminals	3M
Ref	4	G65758 4-	Assembly, RMPA1959	Fairchild
3	5	GRM39XR102KS0V	1000pF Capacitor (0603)	Murata
3	5 (Alt)	ECJ-1V81H102K	1000pF Capacitor (0603)	Panasonic
2	6	C3216X5R1A335M	3.3µF Capacitor (1206)	TDK
1	7	GRM39YSV104Z16V	0.1µF Capacitor (0603)	Murate
1	7 (Alt)	ECJ-1VB1CID4K	0.1µF Capacitor (0603)	Panasonic
A/R	8	SN63	Solder Paste	Indium Corp.
A/R	9	SN96	Solder Paste	Indium Corp

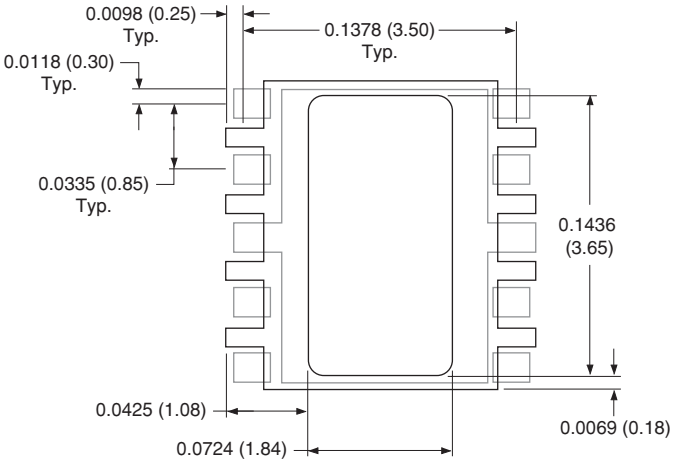
DC Turn On Sequence:

1. Vcc1 = Vcc2 = 3.4V (typical)

2. Vref = 2.85V (typical)

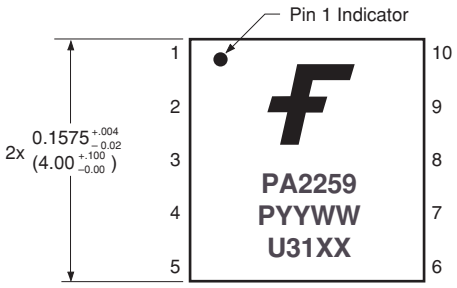
3. Vmode = 2.0V (Pout < 16dBm), 0V (Pout > 16dBm)

Package Outline



Bottom View

Front View



Top View

Dimensions are in inches (mm)

Package Pinout

Pin #	Signal Name	Description
1	Vcc1	Supply Voltage to Input Stage
2	RF In	RF Input Signal
3	GND	Ground
4	Vmode	High-Power/Low-Power Mode Control
5	Vref	Reference Voltage
6	GND	Ground
7	GND	Ground
8	RF Out	RF Output Signal
9	GND	Ground
10	Vcc2	Supply Voltage to Output Stage
11	GND	Paddle Ground

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CoolFET™	FRFET™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QFET®	SuperSOT™-8
DOME™	GTO™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	HiSeC™	MSX™	QT Optoelectronics™	TinyLogic®
E²CMOS™	I²C™	MSXPro™	Quiet Series™	TINYOPTO™
EnSigna™	*i-Lo*™	OCX™	RapidConfigure™	TruTranslation™
FACT™	ImpliedDisconnect™	OCXPro™	RapidConnect™	UHC™
FACT Quiet Series™		OPTOLOGIC®	µSerDes™	UltraFET®
Across the board. Around the world.™		OPTOPLANAR™	SILENT SWITCHER®	VCX™
The Power Franchise®		PACMAN™	SMART START™	
Programmable Active Droop™		POP™	SPM™	

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.