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## RMPA2453

### 2.4–2.5 GHz InGaP HBT Linear Power Amplifier

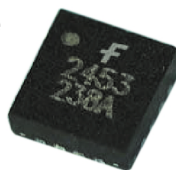
#### General Description

The RMPA2453 power amplifier is designed for high performance WLAN applications in the 2.4–2.5 GHz frequency band. The low profile 16 pin 3 x 3 x 0.9 mm package with internal matching on both input and output to 50Ω minimizes next level PCB space and allows for simplified integration. The on-chip detector provides power sensing capability while the logic control provides power saving shutdown options. The PA's low power consumption and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

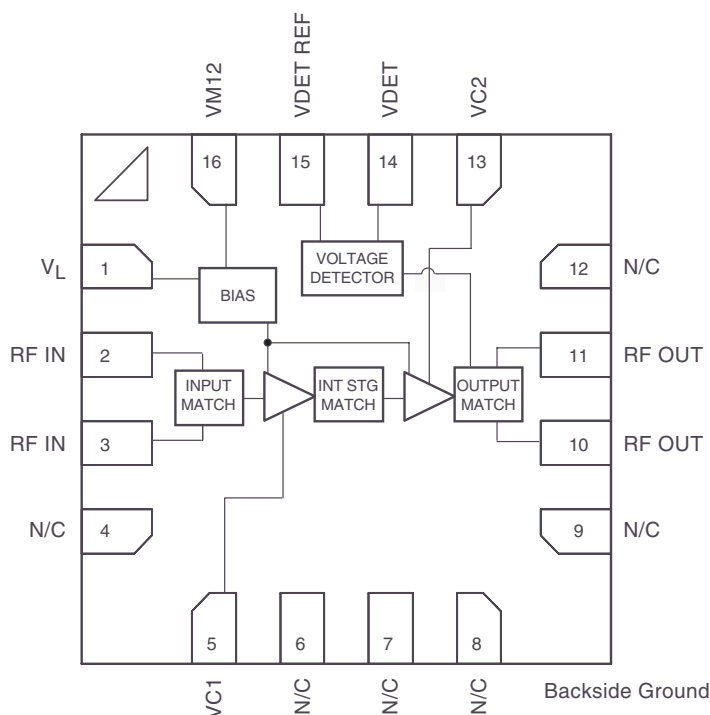
#### Features

- 26dB small signal gain
- 26.5dBm output power @ 1dB compression
- 2.5% EVM at 18dBm modulated output power
- 3.5% EVM at 19dBm modulated output power
- 3.3V single positive supply operation
- Two power saving shutdown options (bias and logic control)
- Integrated power detector with 20dB dynamic range
- Low profile 16 pin 3 x 3 x 0.9 mm leadless package
- Internally matched to 50Ω and DC blocked RF input/output
- Optimized for use in 802.11b/g applications

#### Device



#### Functional Block Diagram



Pin	Description
1	V <sub>L</sub> (logic)
2	RF IN
3	RF IN
4	N/C
5	VC1
6	N/C
7	N/C
8	N/C
9	N/C
10	RF OUT
11	RF OUT
12	N/C
13	VC2
14	VDET
15	VDET REF
16	VM12

**Absolute Ratings<sup>1</sup>**

Symbol	Parameter	Ratings	Units
VC1, VC2	Positive Supply Voltage	5	V
IC1, IC2	Supply Current		
	IC1	120	mA
	IC2	700	mA
VM12	Positive Bias Voltage	4.0	V
V <sub>L</sub>	Logic Voltage	5	V
P <sub>IN</sub>	RF Input Power	10	dBm
T <sub>CASE</sub>	Case Operating Temperature	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C

**Notes:**

1: No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values

**Electrical Characteristics<sup>1, 3</sup>** 802.11g OFDM Modulation (RF framed with 176ms burst time 100ms idle time) 54Mbps Data Rate 16.7MHz Bandwidth

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Supply Voltage	3.0	3.3	3.6	V
Gain	24.5	26	29	dB
Total Current @ 18dBm P <sub>OUT</sub>		133	160	mA
Total Current @ 19dBm P <sub>OUT</sub>		145	165	mA
EVM @ 18dBm P <sub>OUT</sub> <sup>2</sup>		2.5	3.5 <sup>3</sup>	%
EVM @ 19dBm P <sub>OUT</sub> <sup>2</sup>		3.5	4.5 <sup>3</sup>	%
Detector Output @ 19dBm P <sub>OUT</sub>		515	600	mV
Detector Threshold <sup>4</sup>		5.0	7.0	dBm
P <sub>OUT</sub> Spectral Mask Compliance <sup>5</sup>		21.0		dBm

**Electrical Characteristics<sup>3, 6</sup>** 802.11b CCK Modulation (RF not framed) 11Mbps Data Rate 22.0MHz Bandwidth

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Supply Voltage	3.0	3.3	3.6	V
Gain	24.5	26	29	dB
Total Current		250		mA
First Sidelobe Power		-35		dBc
Second Sidelobe Power		-55		dBc
Max P <sub>OUT</sub> Spectral Mask Compliance <sup>7</sup>		24.0		dBm

**Notes:**

1: VC1, VC2, VM12 = 3.3V, T<sub>C</sub> = 25°C, PA is constantly biased, 50Ω system.

2: Percentage includes system noise floor of EVM = 0.8%.

3: EVM not measured 100% in production.

4: P<sub>OUT</sub> measured at P<sub>IN</sub> corresponding to power detection threshold.

5: Measured at P<sub>IN</sub> at which Spectral Mask Compliance is satisfied. Two-sample windowing length applied.

6: VC1, VC2, VM12 = 3.3V, T<sub>C</sub> = 25°C, P<sub>OUT</sub> = +23dBm, 50Ω system. Satisfies spectral mask.

7: P<sub>IN</sub> is adjusted to point where spectral performance reaches maximum limit.

**Electrical Characteristics<sup>1</sup>** Single Tone

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Supply Voltage	3.0	3.3	3.6	V
Gain	24.5	26	29	dB
Total Quiescent Current		105	135	mA
Bias Current at pin VM12 <sup>2</sup>	10.0	12.5	15.0	mA
P1dB Compression	25	26.5		dBm
Standby Current <sup>3</sup>		0.7		mA
Shutdown Current (VM12 = 0V)		<1.0		μA
Input Return Loss		19		dB
Output Return Loss		22		dB
Detector Output at P1dB Comp		2.0		V
Detector P <sub>OUT</sub> Threshold		7.0	9.0	dBm
2nd Harmonic Output at P1dB		-45		dBc
3rd Harmonic Output at P1dB		-42		dBc

**Logic**

Shutdown Control (V <sub>L</sub> ):				
Device Off, Logic High Input	2.0	2.4		V
Device On, Logic Low Input		0.0	0.8	V
Logic Current		150		μA
Turn-on Time <sup>4</sup>		<1		μS
Turn-off Time		<1		μS
Spurious (Stability) <sup>5</sup>		-65		dBc

**Notes:**

1: VC1, VC2, VM12 = 3.3V, T<sub>C</sub> = 25°C, 50Ω system.

2: Bias current is included in the Total Quiescent Current.

3: V<sub>L</sub> is set to Input Logic Level High for PA Off operation.

4: Measured from Device On signal turn on (Logic Low) to the point where RF P<sub>OUT</sub> stabilizes to 0.5dB.

5: Load VSWR is set to 8:1 and the angle is varied 360 degrees. P<sub>OUT</sub> = -30dBm to P1dB.

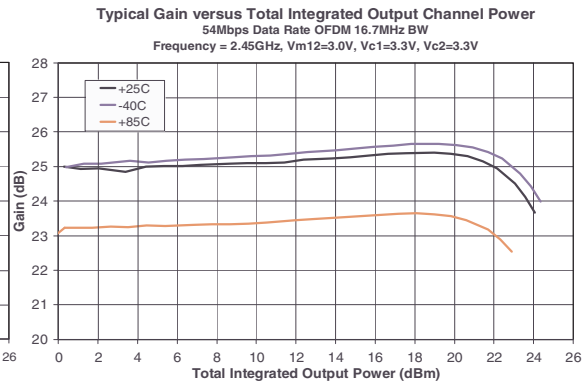
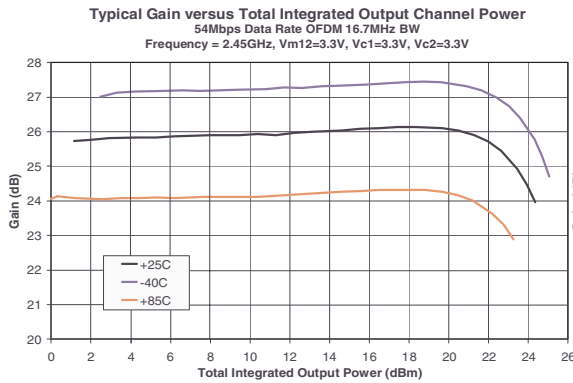
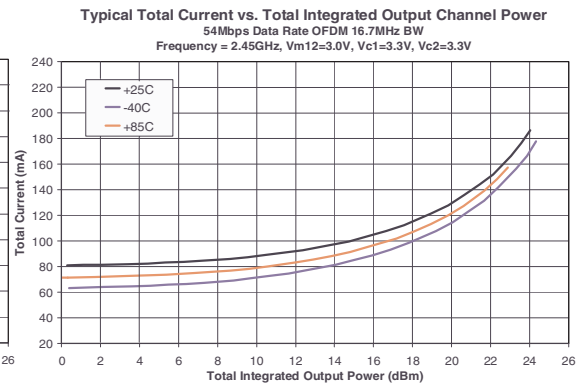
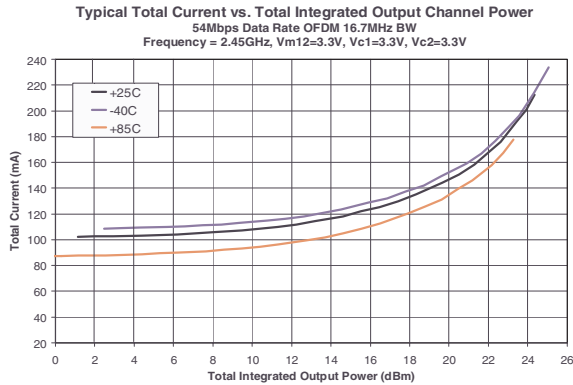
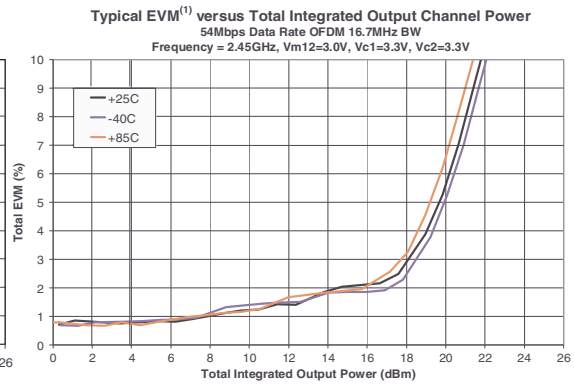
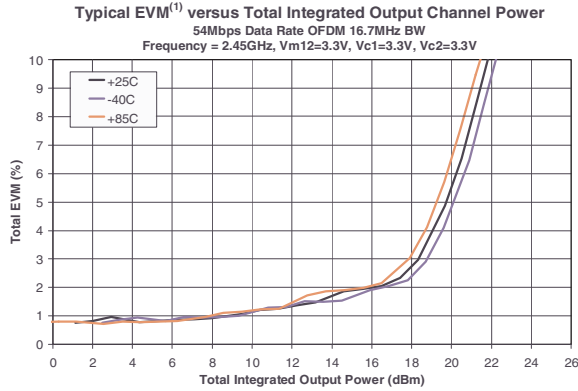


## Typical Characteristics 802.11g

Temperature dependency

Left column VM12 = 3.3V

Right column VM12 = 3.0V



**Note:**

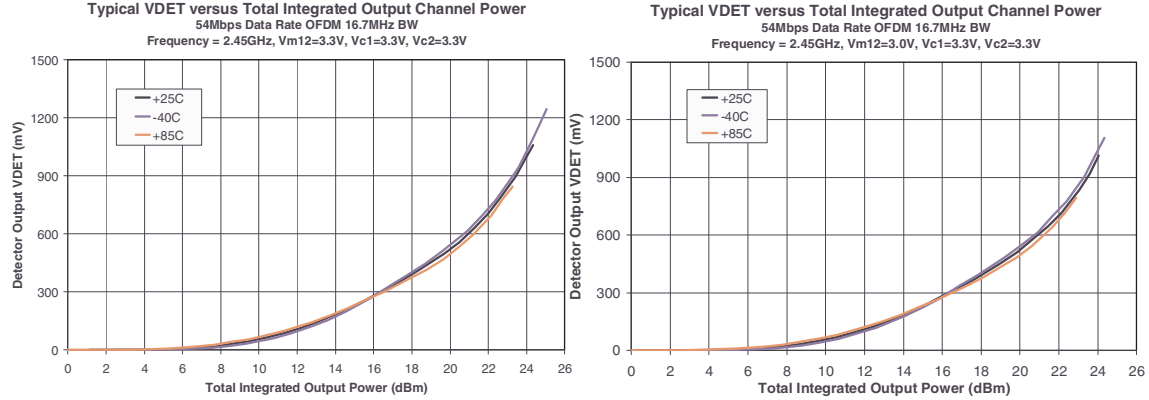
1: Uncorrected EVM. Source EVM is approximately 0.8%.

## Typical Characteristics 802.11g (Continued)

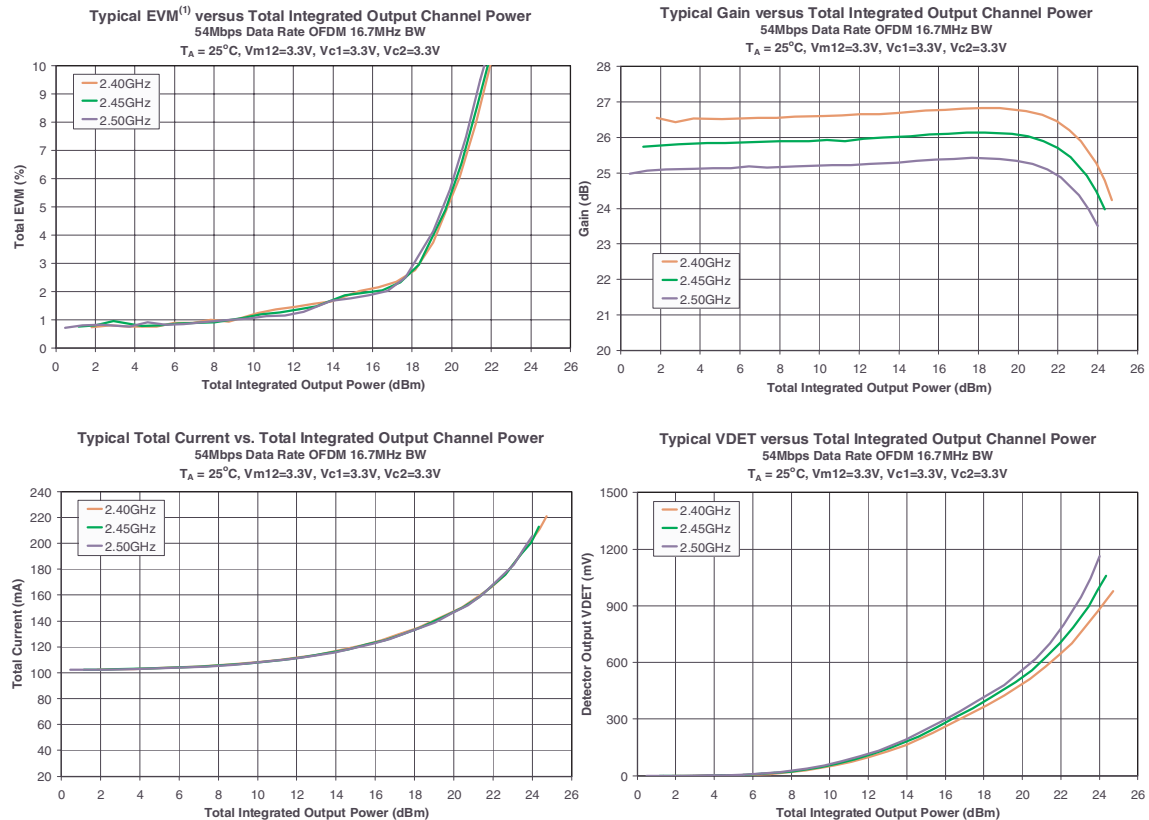
### Temperature Dependency

Left column VM12 = 3.3V

Right column VM12 = 3.0V



### Frequency Dependency VM12 = 3.3V



**Note:**

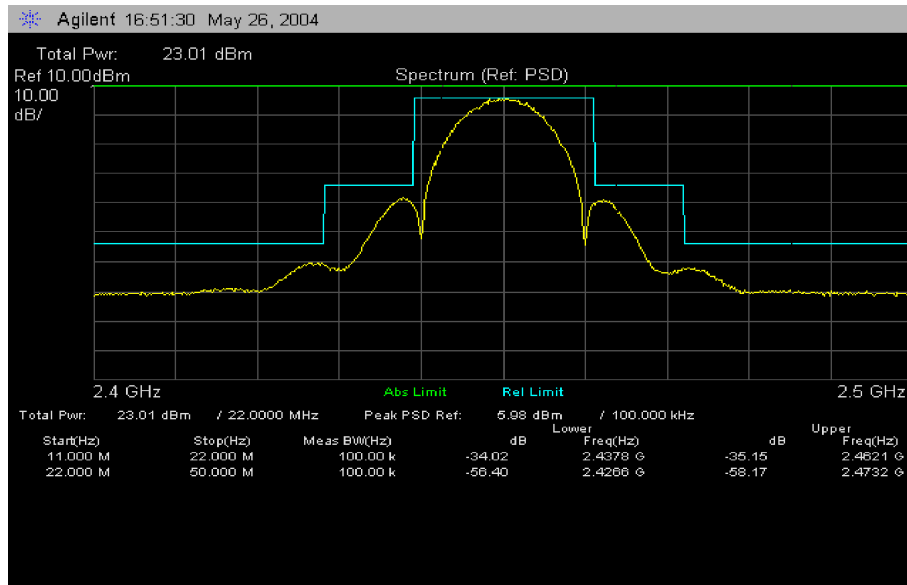
1: Uncorrected EVM. Source EVM is approximately 0.8%.

## Typical Characteristics 802.11b

Spec ANA Pout = 23 dBm

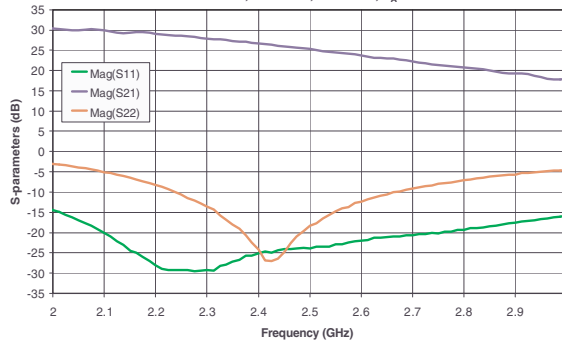
Pin adjusted to the point where the part just begins to approach the 802.11b spectral mask requirements.

**RMPA2453 Spectral Plot Showing Compliance to 802.11b  
Spectral Mask Requirements @ 23 dBm Modulated Output Power  
11 Mbps CCK Data 22 MHz BW  
VC1, VC2 = 3.3V VM12 = 3.3V T=25°C**

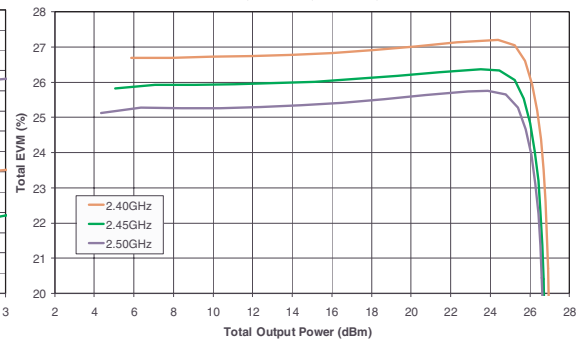


## Single Tone

**Typical Small Signal S-parameters versus Frequency**  
Vm12=3.3V, Vc1=3.3V, Vc2=3.3V, TA = 25°C



**Typical Single Tone Gain versus Single Tone Output Power**  
Vm12=3.3V, Vc1=3.3V, Vc2=3.3V, TA = 25°C



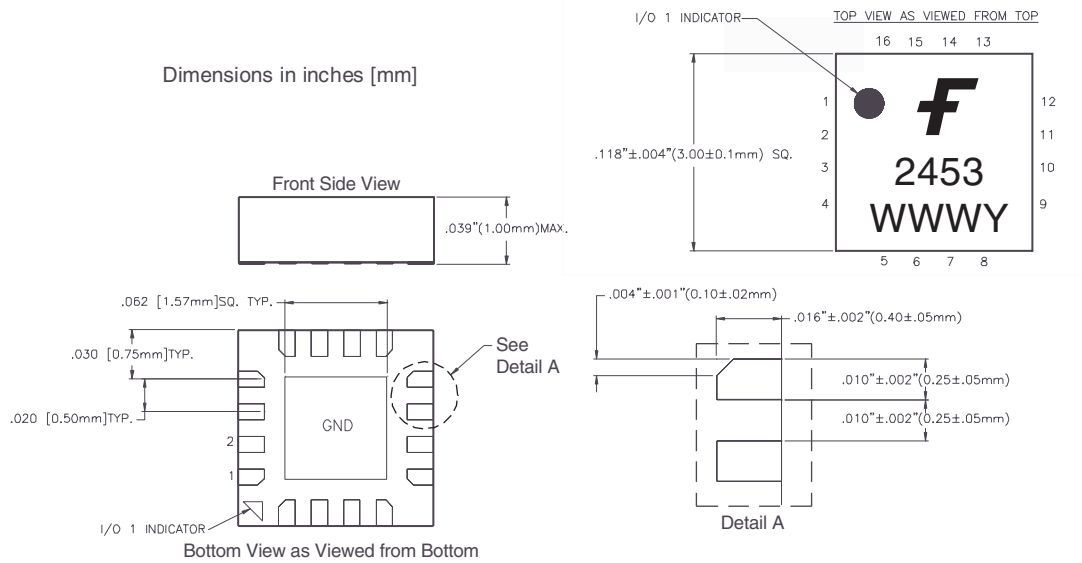
## Application Information

### Precautions to Avoid Permanent Device Damage:

**Static Sensitivity:** Follow ESD precautions to protect against ESD damage.

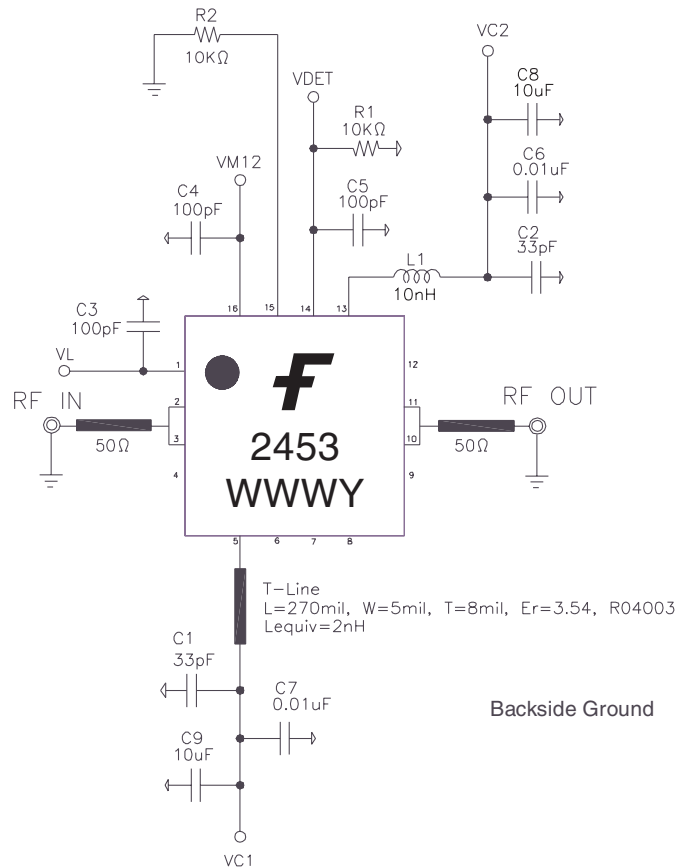
- A properly grounded static-dissipative surface on which to place devices.
- Static-dissipative floor or mat.
- A properly grounded conductive wrist strap for each person to wear while handling devices.

## Package Outline



**Note:** Dimensions do not include protrusions or mold flash. These are not to exceed 0.006" (.155mm) on any side.

## Evaluation Board Schematic



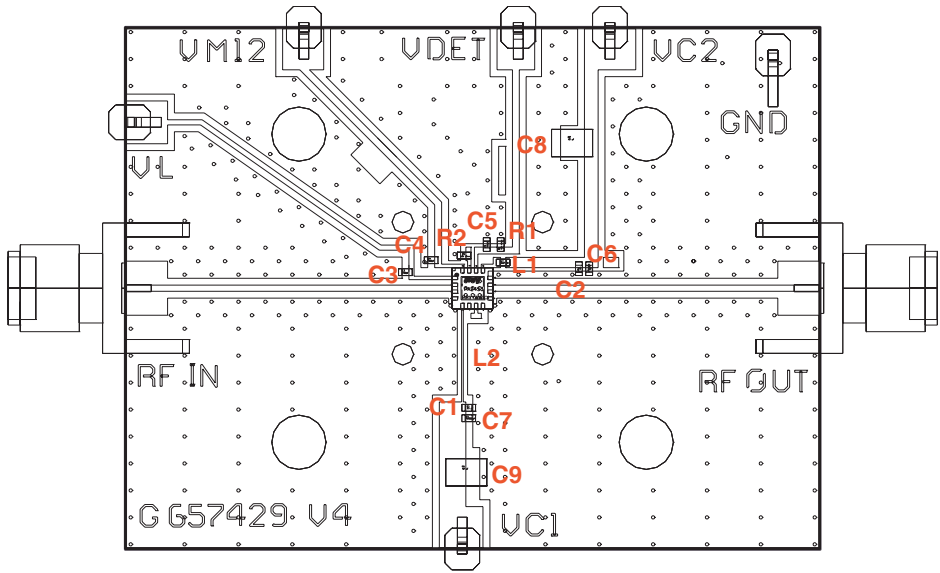


# Evaluation Board of Materials

MATERIALS LIST

QTY	ITEM NO.	PART NUMBER	DESCRIPTION	VENDOR
1	1	G657429	PC, BOARD	FAIRCHILD
2	2	#142-0701-841	SMA CONNECTOR	JOHNSON
6	3	#S1322-XX-ND	RT ANGLE SGL M HEADER	DIGIKEY
REF	4	G657557	ASSEMBLY, RMPA2453	FAIRCHILD
2	5 (C1&C2)	GRM39C0G330J50V	33 pF CAPACITOR	MURATA
3	6 (C3,C4&C5)	GRM36C0G101J50V	100 pF CAPACITOR	MURATA
2	7 (C6&C7)	GMC10X7R103M25NT	.01 uF CAPACITOR	MURATA
2	8 (C8&C9)	CC1206JX5R106M	10 uF CAPACITOR (6.3V)	TDK
1	9 (L1)	LLV1005FB10NJ	10 nH INDUCTOR	TOKO
2	10 (R1&R2)	RC1-0402-1002J	10K OHM RESISTER	IMS
A/R	11	SN63	SOLDER PASTE	INDIUM CORP
A/R	12	SN96	SOLDER PASTE	INDIUM CORP

# Evaluation Board Layout



Actual Board Size = 2.0" X 1.5"

## Evaluation Board Turn-On Sequence<sup>1</sup>

### Recommended turn-on sequence:

- 1) Connect common ground terminal to the Ground (GND) pin on the board.
- 2) Apply low voltage 0.0 to +1.0 V to pin  $V_L$ .
- 3) Apply positive supply voltage VC1 (= 3.3V) to pin VC1 (first stage collector).
- 4) Apply positive supply voltage VC2 (= 3.3V) to pin VC2 (second stage collector).
- 5) Apply positive bias voltage VM12 (= 3.3V) to pin VM12 (bias networks).
- 6) At this point, you should expect to observe the following positive currents flowing into the pins:

Pin	Current
VM12	10.0 – 15.0 mA
VC1	35.0 – 55.0 mA
VC2	40.0 – 60.0 mA
$V_L$	<1 nA

- 7) Apply input RF power to SMA connector pin RFIN. Currents in pins VC1 and VC2 will vary depending on the input drive level.

- 8) Vary positive voltage  $V_L$  on pin VREG from +0.5V to +2.4V to shut down the amplifier or alter the power level. Shut down current flow into the pins:

Pin	Current
VM12	<0.7 mA
VC1	<1 nA
VC2	<1 nA
$V_L$	<0.25 mA

### Recommended turn-off sequence:

Use reverse order described in the turn-on sequence above.

#### Note:

1: Turn on sequence is not critical and it is not necessary to sequence power supplies in actual system level design.

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