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## USB PD Port and Power Controller

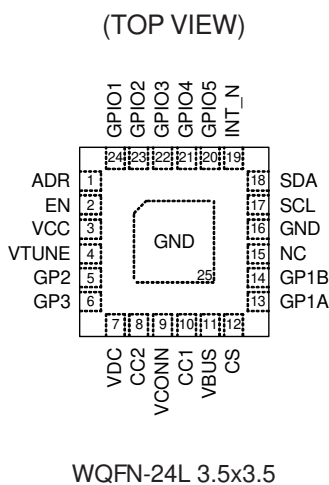
### General Description

The RT1711P is a USB Type-C and Power Delivery (PD) controller, which complies with the latest USB Type-C and PD standards. The RT1711P integrates a complete Type-C transceiver including the Type-C termination resistors, Rp and Rd, and enables the USB Type-C detection including attach and orientation. It also integrates the physical layer of the USB BMC power delivery protocol, allowing power transfers of up to 100W and role swap. The BMC PD function provides full support for Alternate Modes on the USB Type-C standard. The RT1711P provides a complete power management solution, which consists of one barrel jack path and one VBUS path for charging systems. Another provider path provides a seamless voltage transition and avoids the discontinuity of voltage transition during USB PD power contracts.

### Applications

- Tablets
- Laptops
- Notebooks
- Monitors
- Power Banks
- TVs

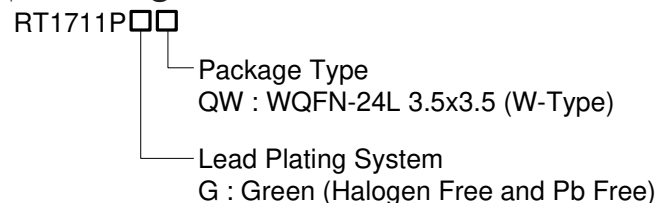
### Pin Configuration



### Features

- **PD-Compatible Dual-Role**
- **Support USB PD3.0 and TCPC1.0**
- **Full Power Path Control**
  - ▶ **Barrel Jack Path : Up to 20V (N-MOSFET)**
  - ▶ **PD Provider & Consumer Path Up to 20V (N-MOSFET)**
- **Protection**
  - ▶ **VBUS Provider Path with Programmable Over-Current Protection (OCP) and Over-Voltage Protection (OVP)**
  - ▶ **VBUS Path with Aided Discharge**
  - ▶ **VCONN with Programmable Current Limit**
  - ▶ **VCONN with OVP Protection and Discharge**
  - ▶ **CC Pin 20V Short-VBUS Circuit Protection**
- **Adjustable DC-DC Output Voltages**
- **Current Capability Definition and Detection**
- **Cable Recognition and Alternate Modes Support**
- **Dead Battery and No Battery Support**
- **Low-Power Mode for Attach Detection**
- **BIST Mode Supported**
- **Support GPIO**
- **24-Lead WQFN Package**

### Ordering Information

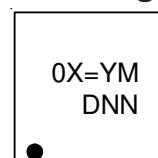


Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

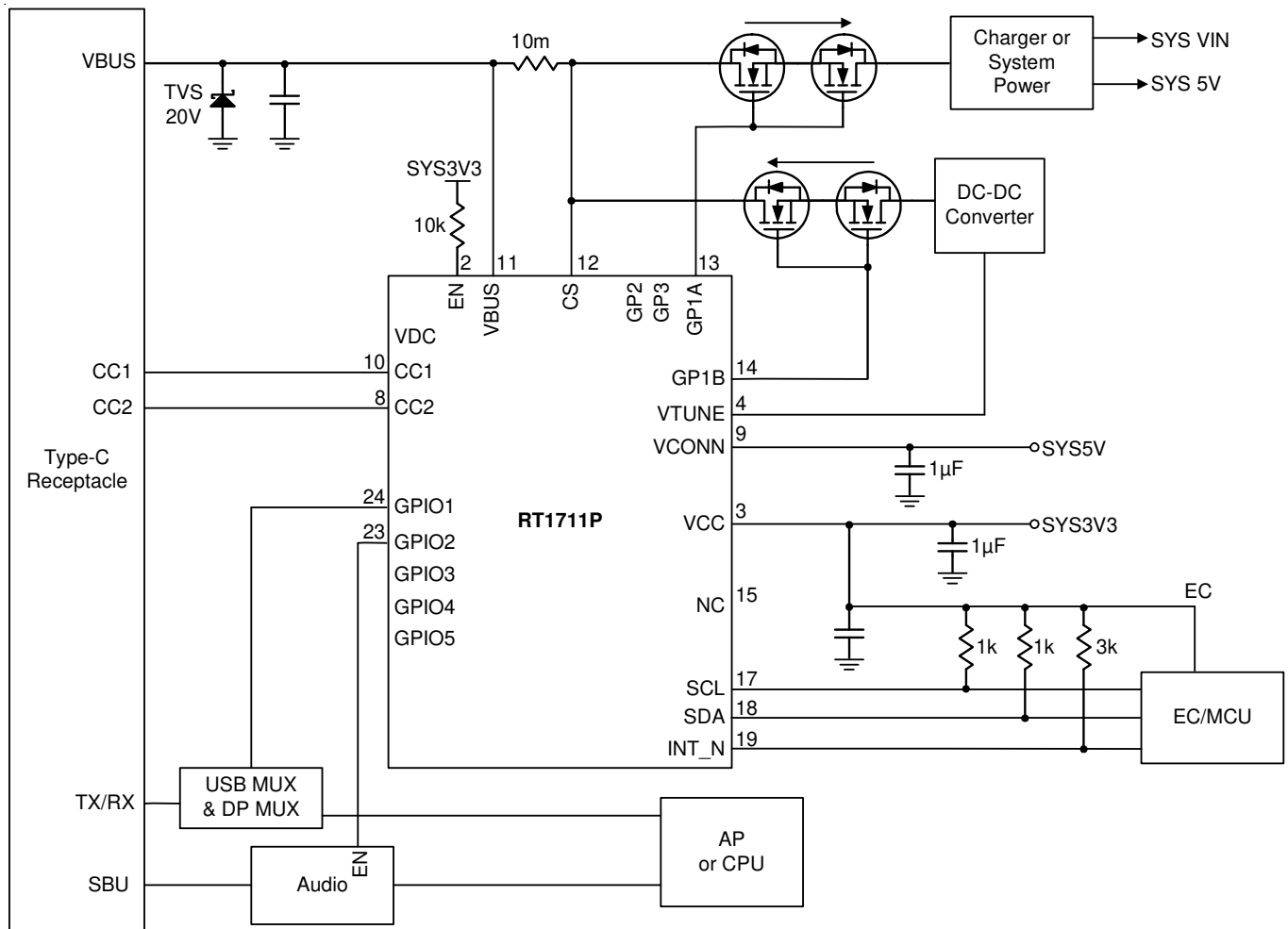
### Marking Information



0X= : Product Code  
YMDNN : Date Code

## Typical Application Circuit

### Provider/Consumer



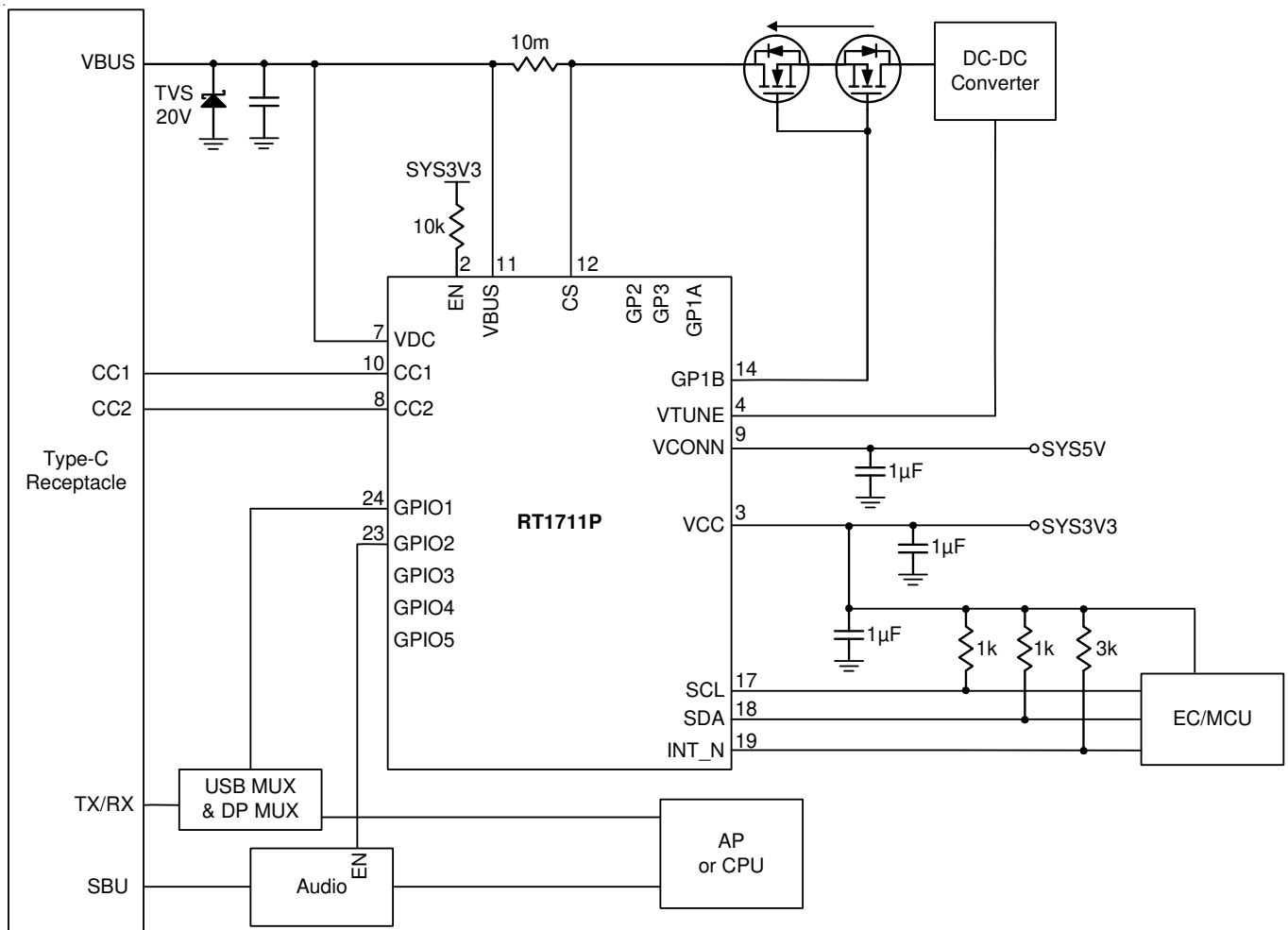
Note : SYS3V3 is connected to a PMIC and is supplied by the PMIC.

1. DC-DC converter recommend best solution. The following table can pass USB PD compliance test.
2. The RT8131B is a high efficiency single phase synchronous buck DC-DC controller. Please refer to the RT8131B datasheet.
3. The RT8525D is a wide input operating voltage range step up controller. High voltage output and large output current are feasible by using an external N-MOSFET. Please refer to the RT8525D datasheet.

VIN	Watts	VOUT/IOUT	Item
12V to 20V	45W	5V, 9V, 12V, 15V/20V	RT8525D (Boost IC)
		3A, 3A, 3A, 3A, 2.25A	RT8131B (Buck IC)
18V to 20V	65W	5V, 9V, 12V, 15V/20V	RT8525D (Boost IC)
		3A, 3A, 3A, 3A, 3.25A	RT8131B (Buck IC)
24V	45W/65W/100W	5V, 9V, 12V, 15V, 20V	RT8131B (Buck IC)
		3A, 3A, 3A, 3A/5A, 3A/5A	



Provider

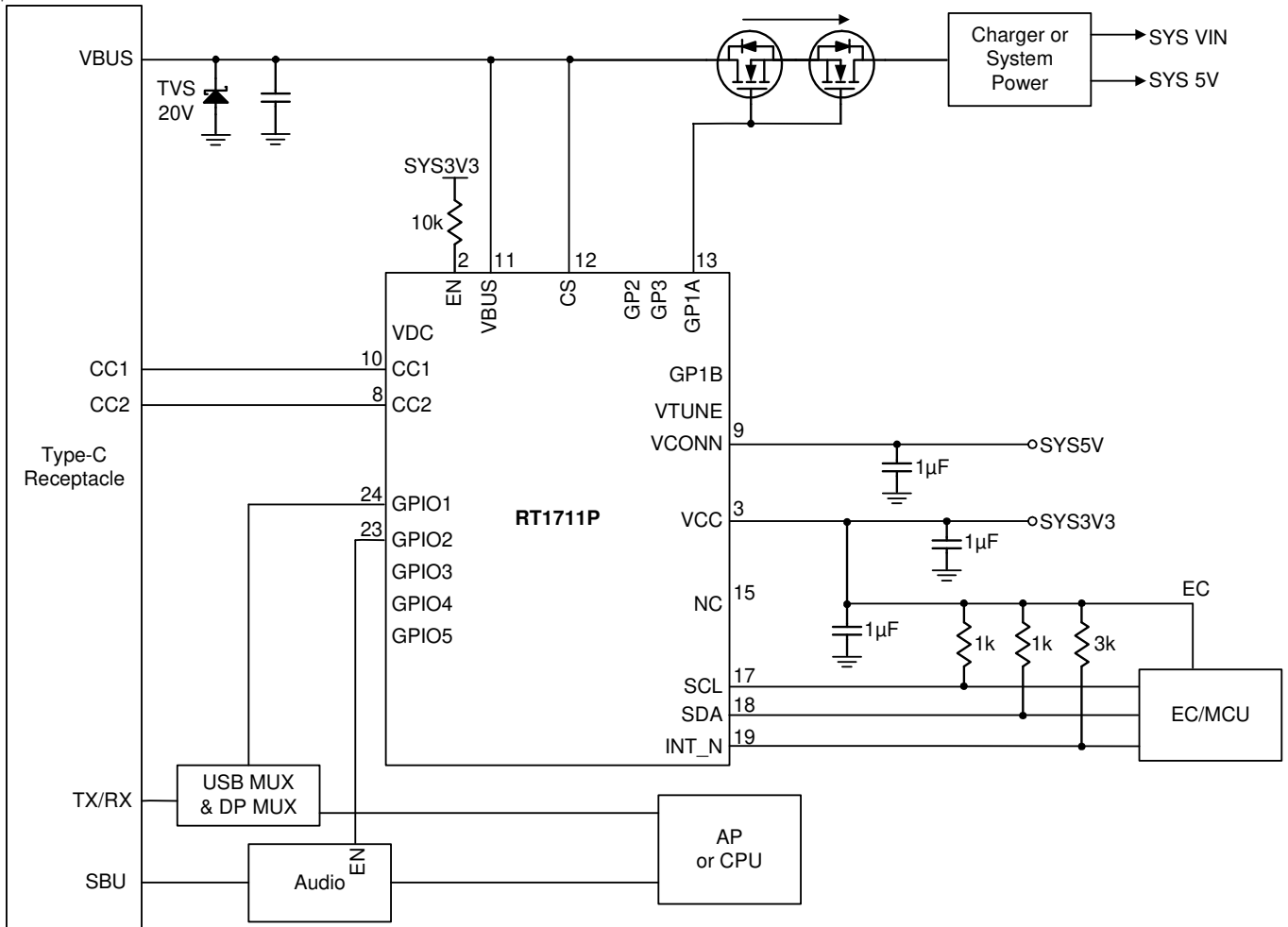


Note : SYS3V3 is connected to a PMIC and is supplied by the PMIC.

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VIN	Watts	VOUT/IOUT	Item
12V to 20V	45W	5V, 9V, 12V, 15V/20V	RT8525D (Boost IC)
		3A, 3A, 3A, 3A, 2.25A	RT8131B (Buck IC)
18V to 20V	65W	5V, 9V, 12V, 15V/20V	RT8525D (Boost IC)
		3A, 3A, 3A, 3A, 3.25A	RT8131B (Buck IC)
24V	45W/65W/100W	5V, 9V, 12V, 15V, 20V	RT8131B (Buck IC)
		3A, 3A, 3A, 3A/5A, 3A/5A	

## Consumer

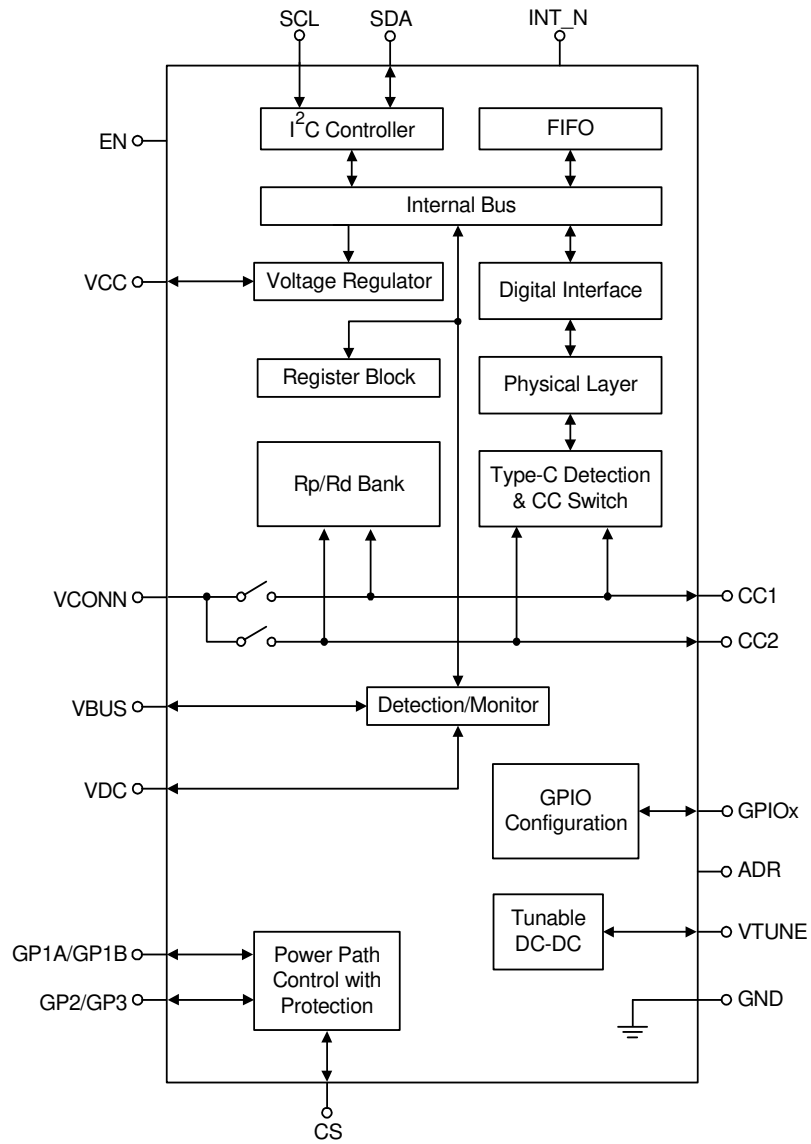


Note : SYS3V3 is connected to a PMIC and is supplied by the PMIC.

**Functional Pin Description**

Pin No.	Pin Name	Pin Function
1	ADR	Address selection node when used with multiple type-C ports.
2	EN	External power path control input, active-high.
3	VCC	Input supply voltage.
4	VTUNE	Connected to FB pin of a DC-DC converter to adjust DC-DC output voltages.
5	GP2	High voltage open-drain gate driver, which may be used to drive an NMOS/PMOS power switch. This pin is connected to the gate of the power switch. (Related to VDC).
6	GP3	High voltage open-drain gate driver, which may be used to drive an NMOS/PMOS power switch. This pin is connected to the gate of the power switch. (Related to VDC).
7	VDC	Barrel jack or wireless charger DC power input pin for charging path control.
8	CC2	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation.
9	VCONN	Regulated input voltage to power CCx pins as VCONN.
10	CC1	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation.
11	VBUS	VBUS input using for OCP/OVP detection and as a power source for VBUS path control.
12	CS	Current sense input.
13	GP1A	High voltage open-drain gate driver, which may be used to drive an NMOS/PMOS power switch. This pin is connected to the gate of the power switch. (Related to VBUS).
14	GP1B	High voltage open-drain gate driver, which may be used to drive an NMOS/PMOS power switch. This pin is connected to the gate of the power switch. (Related to VBUS).
15	NC	No internal connection.
16, 25 (Exposed Pad)	GND	Ground. The exposed pad must be connected to GND and well soldered to a large copper PCB and for maximum power dissipation.
17	SCL	I <sup>2</sup> C interface serial clock input. Open-drain. An external pull-up resistor is required.
18	SDA	I <sup>2</sup> C serial data input/output. Open-drain. An external pull-up resistor is required.
19	INT_N	Interrupt output, active-low open-drain, to prompt the processor to read the registers.
20	GPIO5	Configurable GPIO with open-drain or push-pull type, used as switch control, DC-DC enable, audio enable, and accessory unit control.
21	GPIO4	Configurable GPIO with open-drain or push-pull type, used as switch control, DC-DC enable, audio enable, and accessory unit control.
22	GPIO3	Configurable GPIO with open-drain or push-pull type, used as switch control, DC-DC enable, audio enable, and accessory unit control.
23	GPIO2	Configurable GPIO with open-drain or push-pull type, used as switch control, DC-DC enable, audio enable, and accessory unit control.
24	GPIO1	Configurable GPIO with open-drain or push-pull type, used as switch control, DC-DC enable, audio enable, and accessory unit control.

Functional Block Diagram



**Absolute Maximum Ratings** (Note 1)

- VCC/VCONN ----- -0.3V to 6V
- CC1/CC2 (Testing condition: VCC ≥ 3V) ----- -0.3V to 24V
- CC1/CC2 (Testing condition: VCC < 3V) ----- -0.3V to 6V
- VBUS/VDC ----- - 0.3V to 24V
- Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C  
 WQFN-24L 3.5x3.5 ----- 3.5W
- Package Thermal Resistance (Note 2)  
 WQFN-24L 3.5x3.5, θ<sub>JA</sub> ----- 28.5°C/W  
 WQFN-24L 3.5x3.5, θ<sub>JC</sub> ----- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)  
 HBM (Human Body Model) ----- 2kV

**Recommended Operating Conditions** (Note 4)

- Supply Input Voltage ----- 3V to 5.5V
- VBUS/VDC ----- 4V to 22V
- VCONN Supply Current ----- 200 to 400mA
- VCONN Supply Voltage ----- 4.75V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

**Electrical Characteristics**

(V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Common Normative Signaling Requirements</b>						
Bit Rate	f <sub>BITRATE</sub>		270	300	330	Kbps
<b>Common Normative Signaling Requirements for Transmitter</b>						
Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate.	ρ <sub>BitRate</sub>		--	--	0.25	%
Time from the end of last bit of a Frame until the start of the first bit of the next Preamble.	t <sub>InterFrameGap</sub>		25	--	--	μs
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line.	t <sub>StartDrive</sub>		-1	--	1	μs



Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>BMC Common Normative Requirements</b>						
Time to cease driving the line after the end of the last bit of the Frame.	t <sub>EndDriveBMC</sub>		--	--	23	μs
Fall Time	t <sub>F</sub>		300	--	--	ns
Time to cease driving the line after the final high-to-low transition	t <sub>HoldLowBMC</sub>		1	--	--	μs
Rise Time	t <sub>R</sub>		300	--	--	ns
Voltage Swing	V <sub>SWING</sub>		1.05	1.125	1.2	V
Transmitter Output Impedance	Z <sub>DRIVER</sub>		33	--	75	Ω
<b>BMC Receiver Normative Requirements</b>						
Time Window for Detecting Non-Idle	t <sub>TransitionWindow</sub>		12	--	20	μs
Receiver Input Impedance	Z <sub>BMCRX</sub>		1	--	--	MΩ
<b>Power Consumption</b>						
Disable Mode Current	I <sub>DM</sub>	VCONN supply on power on state, I <sup>2</sup> C pull low and no transaction	--	25	--	μA
		VCONN supply off power on state, I <sup>2</sup> C pull low and no transaction	--	15	--	
Idle Mode Current (As a source)	I <sub>SBID1</sub>	Cable attached with Ra, Rd	--	360	--	μA
		Cable attached with Rd		290		
Idle Mode Current (As a sink)	I <sub>SBID2</sub>	Cable attached	--	180	--	μA
Low-Power Mode	I <sub>UL</sub>	Cable unattached VCONN supply on, DRP toggle	--	V <sub>CC</sub> = 35	--	μA
			--	V <sub>CONN</sub> = 20	--	
		Cable unattached VCONN supply off, DRP toggle.	--	V <sub>CC</sub> = 25	--	
<b>Type-C Port Control</b>						
VCONN Switch On-Resistance	R <sub>ON_VCONN</sub>		--	--	1	Ω
VCONN OCP Range	I <sub>OCP_VCONN</sub>		200	--	600	mA
VCONN Switched-On Time	t <sub>SOFT_VCONN</sub>		--	1.2	--	ms
DFP 80μA CC Current	I <sub>CC_DFP80μ</sub>		64	80	96	μA
DFP 180μA CC Current	I <sub>CC_DFP180μ</sub>		166	180	194	μA
DFP 330μA CC Current	I <sub>CC_DFP330μ</sub>		304	330	356	μA
UFP Pull-Down Resistance through Each CC Pin	R <sub>d</sub>		4.59	5.1	5.61	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UFP Pull-Down Threshold Voltage in Dead Battery	V <sub>TH_DBL</sub>	Under I <sub>CC</sub> = I <sub>CC_DFP80μ</sub> and I <sub>CC_DFP180μ</sub>	0.2	--	1.6	V
UFP Pull-Down Threshold Voltage in Dead Battery	V <sub>TH_DBH</sub>	Under I <sub>CC</sub> = I <sub>CC_DFP330μ</sub>	0.8	--	2.6	V
<b>VCC/VDC/EN Operation Conditions</b>						
VCC Input Supply Voltage	V <sub>VCC</sub>		3.0	3.3	5.5	V
VDC Input Supply Voltage	V <sub>VDC</sub>		4.5	--	20	V
EN Threshold			0.8	1	1.2	V
<b>VBUS Related Parameters</b>						
VBUS Detection Valid Voltage (Rising)		Rising	--	4	--	V
VBUS Detection Invalid Voltage (Falling)		Falling	--	3.5	--	V
VBUS Vsafe0V			--	--	0.8	V
VBUS Measure Range			4	--	20	V
VBUS Measurement Resolution			--	50	--	mV
VBUS Measurement Update Interval			--	5.375	--	ms
VBUS Over-Voltage Protection Threshold Range	V <sub>TH_VBUSOVP</sub>		5.5	--	23	V
VBUS Over-Current Protection Threshold Range	I <sub>TH_VBUSOCP</sub>		0.6	--	6	A
VBUS OCP Deglitch Time	t <sub>D_VBUSOCP</sub>		--	--	200	μs
VBUS Tuning Resolution (Source Side)			--	100	--	mV
<b>I<sup>2</sup>C Electrical Characteristics</b>						
I <sup>2</sup> C Bus Supply Voltage	V <sub>CC_I2C</sub>		1.5	--	3.6	V
Logic-Low Threshold Voltage for Inputs	V <sub>IL_I2C</sub>		--	--	0.4	V
Logic-High Threshold Voltage for Inputs	V <sub>IH_I2C</sub>		1.3	--	--	V
Logic-Low Threshold Voltage for Open-Drain Outputs	V <sub>OL_I2C</sub>	Open-drain	--	--	0.4	V
Input Current for Each I/O Pin	I <sub>IN_IO_I2C</sub>	0.1 * V <sub>CC</sub> < V <sub>IN_IO</sub> < 0.9 * V <sub>CC</sub> (Max)	-10	--	10	μA
SCL Clock Frequency	f <sub>SCL</sub>		0	--	1000	kHz
Maximum Spike Pulse width	t <sub>W_MAX_SP</sub>		--	--	50	ns
Data Hold Time	t <sub>DH</sub>		30	--	--	ns
Data Set-Up Time	t <sub>DS</sub>		70	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>GPIO1 to GPIO5 Electrical Characteristics</b>						
Logic-Low Threshold Voltage for Inputs	V <sub>IL_GPIO</sub>		--	--	0.4	V
Logic-High Threshold Voltage for Inputs	V <sub>IH_GPIO</sub>		1.1	--	--	V
Logic-Low Threshold Voltage for Outputs	V <sub>OL_GPIO</sub>	I <sub>OL</sub> = 4mA	--	--	0.4	V
Logic-High Threshold Voltage for Outputs	V <sub>OH_GPIO</sub>	I <sub>OH</sub> = -4mA	V <sub>CC</sub> - 0.7V	--	--	V

(V<sub>CC</sub> = 3.3V, V<sub>VCONN</sub> = 5V, V<sub>BUS</sub> = 20V, T<sub>A</sub> = 25°C, unless otherwise specified.)

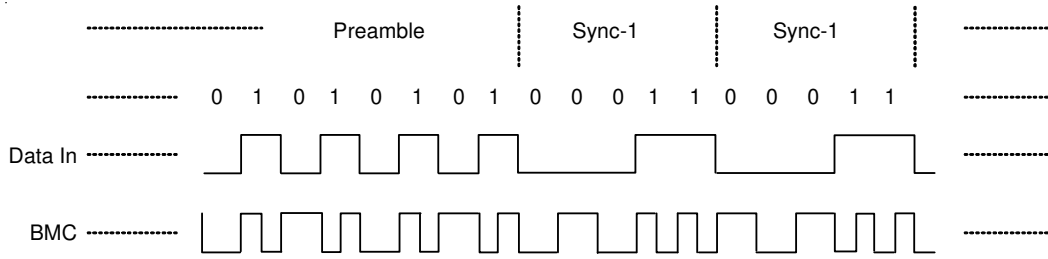
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>N-MOSFET Gate Control Related Parameters</b>						
GP1A/GP1B		For N-MOSFET gate control	V <sub>BUS</sub> + V <sub>VCONN</sub> - 1	V <sub>BUS</sub> + V <sub>VCONN</sub> - 0.7	V <sub>BUS</sub> + V <sub>VCONN</sub> - 0.2	V
GP2/GP3		For N-MOSFET gate control	V <sub>VDC</sub> + V <sub>VCONN</sub> - 1	V <sub>VDC</sub> + V <sub>VCONN</sub> - 0.7	V <sub>VDC</sub> + V <sub>VCONN</sub> - 0.2	V

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

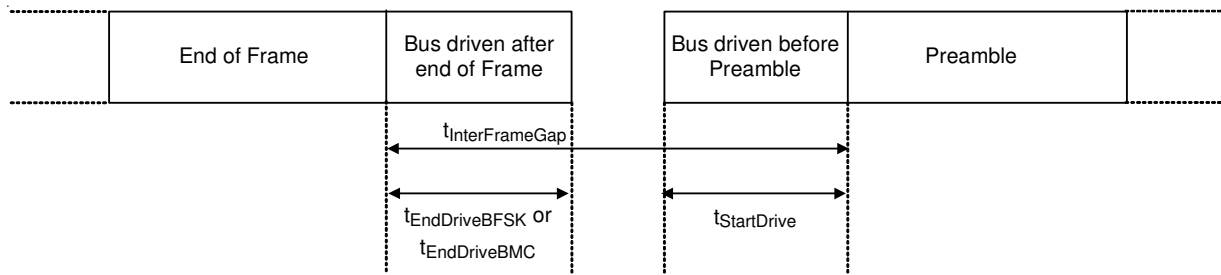
**Note 2.** θ<sub>JA</sub> is measured under natural convection (still air) at T<sub>A</sub> = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ<sub>JC</sub> is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

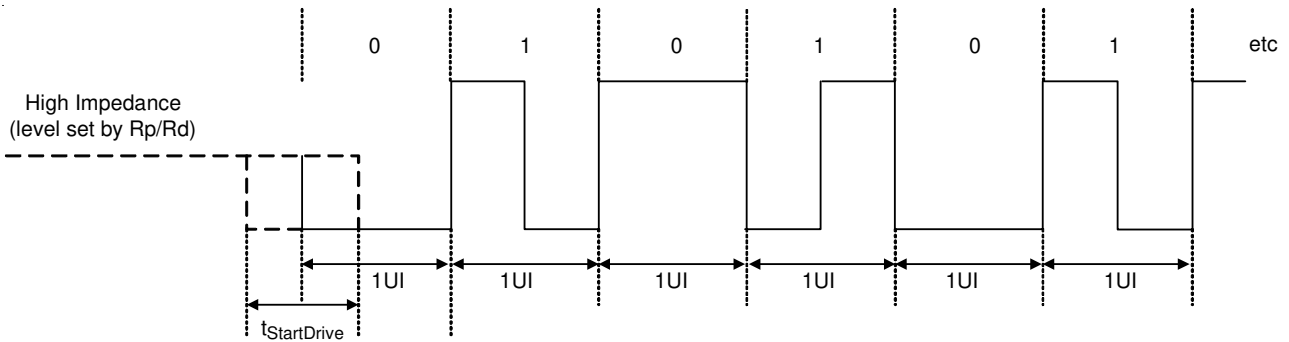
**Note 4.** The device is not guaranteed to function outside its operating conditions.



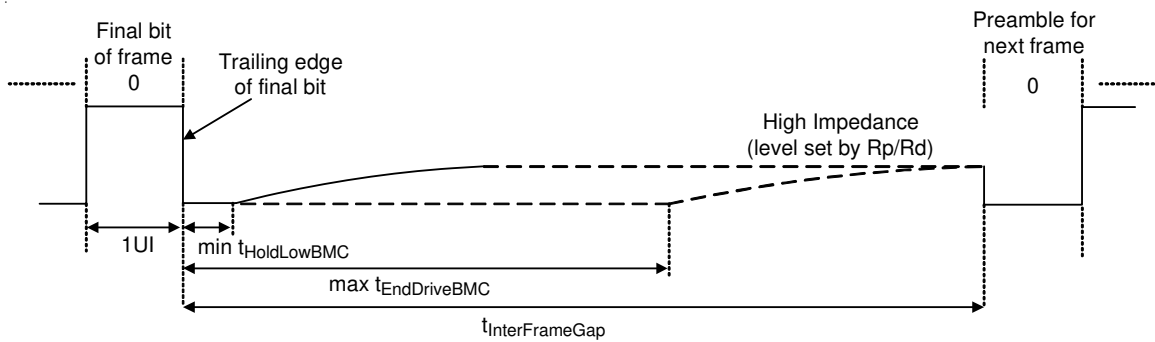
BMC Example



Inter-Frame Gap Timings



BMC Encoded Start of Preamble

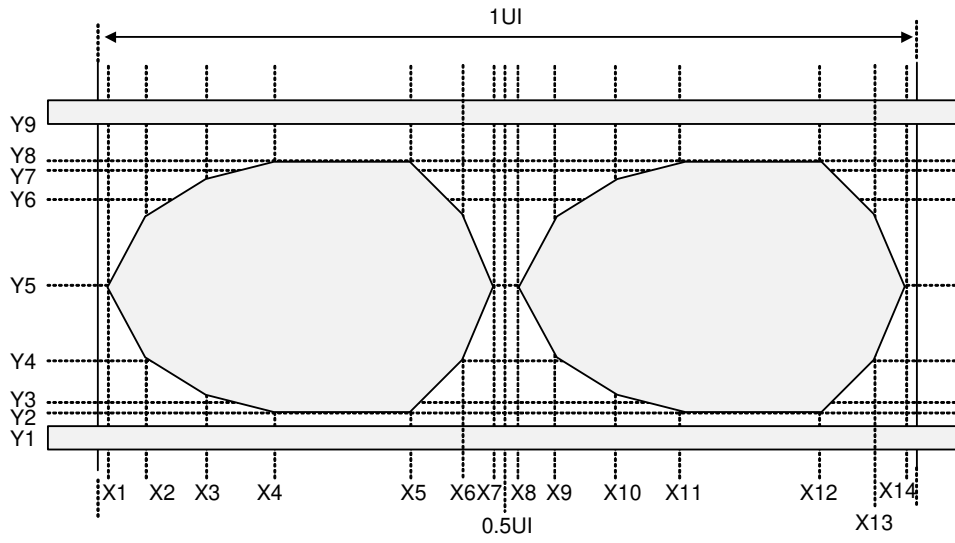


Transmitting or Receiving BMC Encoded Frame Terminated

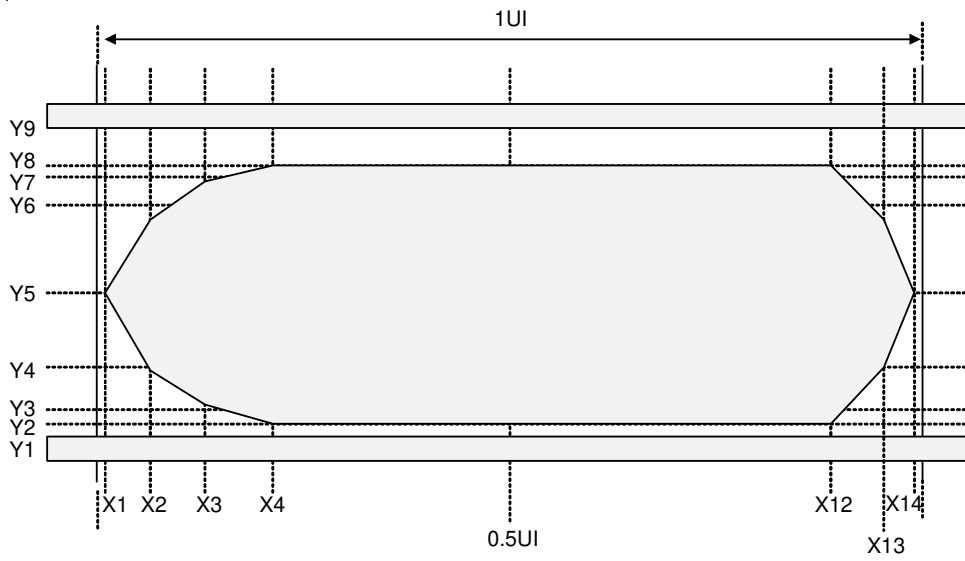
BMC TC Mask Definition, X Values						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Left Edge of Mask	X1Tx			0.015		UI
X2Tx point	X2Tx			0.07		UI
X3Tx point	X3Tx			0.15		UI
X4Tx point	X4Tx			0.25		UI
X5Tx point	X5Tx			0.35		UI
X6Tx point	X6Tx			0.43		UI
X7Tx point	X7Tx			0.485		UI
X8Tx point	X8Tx			0.515		UI
X9Tx point	X9Tx			0.57		UI
X10Tx point	X10Tx			0.65		UI
X11Tx point	X11Tx			0.75		UI
X12Tx point	X12Tx			0.85		UI
X13Tx point	X13Tx			0.93		UI
Right Edge of Mask	X14Tx			0.985		UI

BMC TC Mask Definition, Y Values						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Lower bound of outer mask	Y1Tx			-0.075		V
Lower bound of inner mask	Y2Tx			0.075		V
Y3Tx point	Y3Tx			0.15		V
Y4Tx point	Y4Tx			0.325		V
Inner mask vertical midpoint	Y5Tx			0.5625		V
Y6Tx point	Y6Tx			0.8		V
Y7Tx point	Y7Tx			0.975		V
Y8Tx point	Y8Tx			1.04		V
Upper bound of outer mask	Y9Tx			1.2		V





BMC T<sub>X</sub> "ONE" Mask



BMC T<sub>X</sub> "ZERO" Mask

Application Information

Output Voltage Setting for the DC-DC Converter

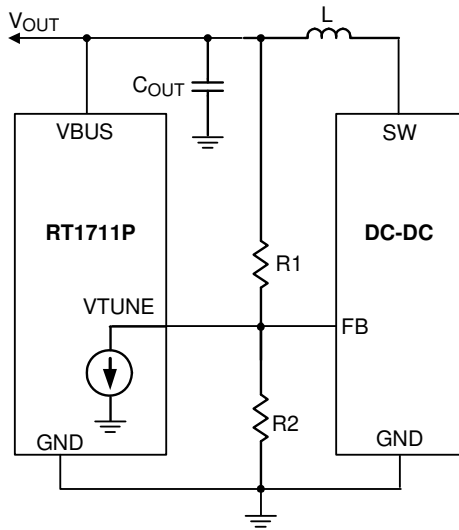


Figure 1

Figure 1 shows the RT1711P can change the output voltage ( $V_{OUT}$ ) of the DC-DC converter by controlling the VTUNE sinking current.

The following table shows the range of R1 value :

$V_{REF}$ of DC-DC	R1 Range ( $\Omega$ )
0.6V	60k to 80k
0.8V	60k to 80k
1.225V	60k to 80k
1.25V	60k to 80k

The default  $V_{OUT}$  needs to be set as 5V output, so that R2 value can be decided by the following equation :

$$R2 = \frac{R1}{\left(\frac{5V}{V_{REF}}\right) - 1}$$

The “Num” (register A6h, A7h) is a 10-bit number and each step is 25mV. The range of “Num” is 0 to 832 and the range of the output voltage ( $V_{OUT}$ ) is 5V to 20V.

The output voltage ( $V_{OUT}$ ) of the DC-DC converter can be programmed according to the following equation :

If the “Num” value is less than or equal to 200 :

$$V_{OUT} = 5V$$

If the “Num” value is greater than 200 :

$$V_{OUT} = 25mV \times \text{Num equal } 0 \text{ when the value is from } 0 \text{ to } 200.$$

For example :

Setting “Num” = 600 represents 15V output.

Setting “Num” = 0 to 200 represents 5V output.

I<sup>2</sup>C address Setting by the ADR Pin

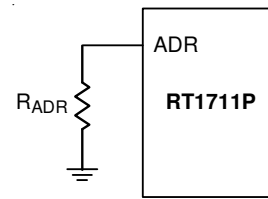


Figure 2

Figure 2 shows I<sup>2</sup>C address setting by  $R_{ADR}$  resistor

Where  $R_{ADR} = 0\Omega$ , the I<sup>2</sup>C address shows below :

1	0	0	1	1	0	0	R/W
---	---	---	---	---	---	---	-----

MSB

LSB

Where  $R_{ADR} = 310k\Omega$ , the I<sup>2</sup>C address shows below :

1	0	0	1	1	0	1	R/W
---	---	---	---	---	---	---	-----

MSB

LSB

Where  $R_{ADR} = 670k\Omega$ , the I<sup>2</sup>C address shows below :

1	0	0	1	1	1	0	R/W
---	---	---	---	---	---	---	-----

MSB

LSB

Where  $R_{ADR} = \text{open}$ , the I<sup>2</sup>C address shows below :

1	0	0	1	1	1	1	R/W
---	---	---	---	---	---	---	-----

MSB

LSB

**Type-C Detection**

The RT1711P implements multiple comparators that can be used by software to determine the state of the CC1, CC2 and VBUS pins. This status information provides the host processor with all of the information required to determine attach and detach status.

The RT1711P has three threshold comparators that match the USB Type-C specification for the three charge current levels that can be detected by a Type-C device. These comparators automatically cause interrupts to occur when there is a change of state.

The RT1711P also has a comparator that monitors if VBUS has reached a valid threshold or not. The DAC can be used to measure VBUS up to 20V which allows the software to confirm that changes to the VBUS line has occurred as expected based on Power Delivery (PD) to change the voltage level.

**Detection through Autonomous DRP Toggles**

The RT1711P has the capability to do autonomous DRP toggle. In DRP toggle the RT1711P implements DRP toggle between presenting as a SRC (source) and presenting as a SNK (sink). It can also present as a SRC or SNK only and monitor CC1, CC2 and VBUS status.

**PD Protocol Communication**

Type-C connector allows USB Power Delivery (PD) to be communicated over the connected CC pin between two ports. The communication method is the BMC Power Delivery protocol. Possible uses are outlined below.

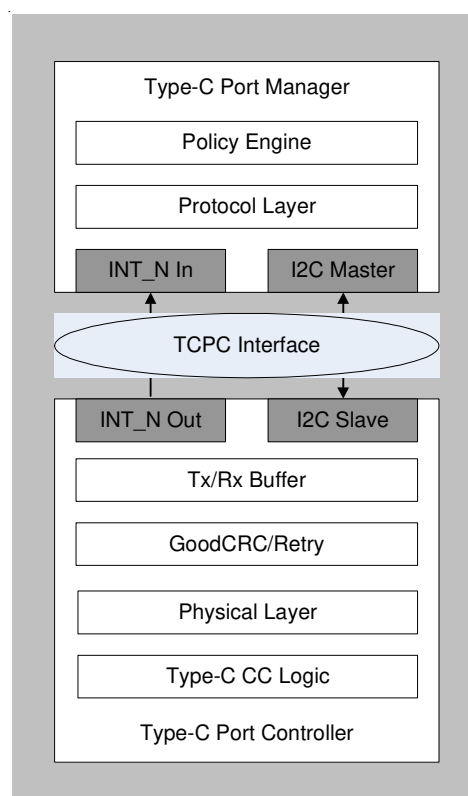
- ▶ Negotiating and controlling power levels
- ▶ Alternative interfaces such as DisplayPort
- ▶ Role swap for dual-role ports that switch who is the source or sink
- ▶ Communication with USB Type-C full featured cables

The RT1711P integrates a BMC PD block which includes the BMC physical layer and packet buffer which allow packets to be sent and received by the host software through I2C accesses. The RT1711P allows host software to implement all features of USB BMC PD through writes and reads of the buffer and control of the RT1711P physical interface.

**Abbreviations :**

Term	Description
BMC	Biphase Mark Coding
TCPC	Type-C Port Controller
TCPCI	Type-C Port Controller Interface
TCPM	Type-C Port Manager

**Type-C Port Controller (TCPC) Interface :**



The Type-C Port Controller Interface, TCPCI, is the interface between a Type-C Port Manager and a Type-C Port Controller.

**The Controller Interface uses the I<sup>2</sup>C Protocol :**

- ▶ The TCPM is the only master on this I<sup>2</sup>C bus
- ▶ The TCPC is a slave device on this I<sup>2</sup>C bus
- ▶ Each Type-C port has its own unique I<sup>2</sup>C slave address  
The TCPC shall have equal numbers of unique I<sup>2</sup>C slave addresses and supported Type-C ports
- ▶ The TCPC supports fast-mode bus speed

- ▶ The TCPC has an open drain output, active low INT\_N Pin. This pin is used to indicate change of state, where INT\_N pin is asserted when any Alert Bits are set
- ▶ The TCPCI supports an I/O nominal voltage range of 1.8V and 3.3V
- ▶ The TCPC can auto-increment the I<sup>2</sup>C internal register address of the last byte transferred during a read independent of an ACK/NACK from the master

**Register Map :**

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x00	1	VENDOR_ID	7:0	VID[7:0]	0	R	A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.
0x01	1		7:0	VID[15:8]	0	R	
0x02	1	PRODUCT_ID	7:0	PID[7:0]	0	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC.
0x03	1		7:0	PID[15:8]	0	R	
0x04	1	DEVICE_ID	7:0	DID[7:0]	0	R	A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the TCPC.
0x05	1		7:0	DID[15:8]	0	R	
0x06	1	USBTYPEPEC_REV	7:0	USBTYPEPEC_REV	0	R	Version number assigned by USB-IF (Currently at Revision 1.1 – 0001 0001)
0x07	1		7:0	Reserved	0	R	
0x08	1	USBPD_REV_VER	7:0	USBPD_VER	0	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x09	1		7:0	USBPD_REV	0	R	0010 0000 – Revision 2.0
0x0A	1	PD_INTERFACE_REV	7:0	PDIF_VER	0	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x0B	1		7:0	PDIF_REV	0	R	0010 0000 – Revision 2.0
0x10	1	ALERT	7	ALARM_VBUS_VOLTAGE_H	0	RW	0b : Cleared 1b : A high-voltage alarm has occurred
			6	TX_SUCCESS	0	RW	0b : Cleared, 1b : Reset or SOP* message transmission successful.
			5	TX_DISCARD	0	RW	0b: Cleared, 1b: Reset or SOP* message transmission not sent due to incoming receive message.
			4	TX_FAIL	0	RW	0b : Cleared, 1b : SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.
			3	RX_HARD_RESET	0	RW	0b : Cleared, 1b : Received Hard Reset message
			2	RX_SOP_MSG_STATUS	0	RW	0b : Cleared, 1b : Receive status register changed
			1	POWER_STATUS	0	RW	0b : Cleared, 1b : Port status changed
			0	CC_STATUS	0	RW	0b : Cleared, 1b : CC status changed



Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x11	1	ALERT	7	Reserved	0	R	
			6	Reserved	0	R	
			5	Reserved	0	R	
			4	Reserved	0	R	
			3	VBUS_SINK_DISCNT	0	RW	0b : Cleared 1b : A VBUS Sink Disconnect Threshold crossing has been detected
			2	RXBUF_OVFLOW	0	RW	0b : TCPC Rx buffer is functioning properly. 1b : TCPC Rx buffer has overflowed.
			1	FAULT	0	RW	0b : No Fault. 1b : A Fault has occurred. Read the FAULT_STATUS register.
			0	ALARM_VBUS_VOLTAGE_L	0	RW	0b : Cleared 1b : A low-voltage alarm has occurred
0x12	1	ALERT_MASK	7	M_ALARM_VBUS_VOLTAGE_H	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			6	M_TX_SUCCESS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			5	M_TX_DISCARD	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			4	M_TX_FAIL	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			3	M_RX_HARD_RESET	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			2	M_RX_SOP_MSG_STATUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			1	M_POWER_STATUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			0	M_CC_STATUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
0x13	1	ALERT_MASK	7	Reserved	0	R	
			6	Reserved	0	R	
			5	Reserved	0	R	
			4	Reserved	0	R	
			3	M_VBUS_SINK_DISCNT	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			2	M_RXBUF_OVFLOW	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			1	M_FAULT	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			0	M_ALARM_VBUS_VOLTAGE_L	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x14	1	POWER_STATUS_MASK	7	M_DBG_ACC_CONNECT	0	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			6	M_TCPC_INITIAL	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			5	M_SRC_HV	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			4	M_SRC_VBUS	1	RW	0b: Interrupt masked, 1b: Interrupt unmasked
			3	M_VBUS_PRESENT_DETC	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			2	M_VBUS_PRESENT	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			1	M_VCONN_PRESENT	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			0	M_SINK_VBUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
0x15	1	FAULT_STATUS_MASK	7	M_VCON_OV	0	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			6	M_FORCE_OFF_VBUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			5	M_AUTO_DISC_FAIL	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			4	M_FORCE_DISC_FAIL	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			3	M_VBUS_OC	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			2	M_VBUS_OV	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			1	M_VCON_OC	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			0	M_I2C_ERROR	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
0x18	1	CONFIG_STANDARD_OUTPUT	7	H_IMPEDENCE	0	R	Not support.
			6	DBG_ACC_CONNECT_O	1	R	Not support.
			5	AUDIO_ACC_CONNECT	1	R	Not support.
			4	ACTIVE_CABLE_CONNECT	0	R	Not support.
			3:2	MUX_CTRL	0	R	Not support.
			1	CONNECT_PRESENT	0	R	Not support.
			0	CONNECT_ORIENT	0	R	Not support.

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x19	1	TCPC_CONTROL	7:5	Reserved	0	R	
			4	Reserved	0	R	
			3:2	I2C_CK_STRETCH	00	R	Not support.
			1	BIST_TEST_MODE	0	RW	0 : Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1 : BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.
			0	PLUG_ORIENT	0	RW	0b : When Vconn is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b : When Vconn is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. Required
0x1A	1	ROLE_CONTROL	7	Reserved	0	R	
			6	DRP	0	RW	0b : No DRP. Bits B3..0 determine Rp/Rd/Ra settings 1b: DRP
			5:4	RP_VALUE	0	RW	00b : Rp default 01b : Rp 1.5A 10b : Rp 3.0A 11b : Reserved
			3:2	CC2	10	RW	00b : Reserved 01b : Rp (Use Rp definition in B5..4) 10b : Rd 11b : Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6
			1:0	CC1	10	RW	00b : Reserved 01b : Rp (Use Rp definition in B5..4) 10b : Rd 11b : Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x1B	1	FAULT_CONTROL	7	DIS_VCON_OV	0	RW	0b : Fault detection circuit enabled 1b : Fault detection circuit disabled
			6:5	Reserved	0	R	
			4	DIS_FORCE_OFF_VBUS	0	RW	0b : Allow STANDARD INPUT SIGNAL Force Off Vbus control (default) 1b : Block STANDARD INPUT SIGNAL Force Off Vbus control. VBUS gate control by setting register 0xBB[3:0]
			3	DIS_VBUS_DISC_FAULT_TIMER	0	RW	0b : VBUS Discharge Fault Detection Timer enabled 1b : VBUS Discharge Fault Detection Timer disabled
			2	DIS_VBUS_OC	0	RW	0b : Internal and External OCP circuit enabled 1b : Internal and External OCP circuit disabled
			1	DIS_VBUS_OV	0	RW	0b : Internal and External OVP circuit enabled 1b : Internal and External OVP circuit disabled
			0	DIS_VCON_OC	0	RW	0b : Fault detection circuit enabled 1b : Fault detection circuit disabled
0x1C	1	POWER_CONTROL	7	Reserved	0	R	
			6	VBUS_VOL_MONITOR	0	RW	0b : VBUS_VOLTAGE Monitoring is enabled (default) 1b : VBUS_VOLTAGE Monitoring is disabled
			5	DIS_VOL_ALARM	0	RW	0b: Voltage Alarms Power status reporting is enabled (default) 1b: Voltage Alarms Power status reporting is disabled
			4	AUTO_DISC_DISCNCT_EN	1	RW	0b : The TCPC shall not automatically discharge VBUS based on VBUS voltage. 1b : The TCPC shall automatically discharge during 50ms. (default)
			3	BLEED_DISC_EN	0	RW	0b : Disable bleed discharge (default) 1b : Enable bleed discharge of VBUS
			2	FORCE_DISC_EN	0	RW	0b : Disable forced discharge (default) 1b : Enable forced discharge of VBUS during 50ms.
			1	VCONN_POWER_SPT	0	RW	0b : TCPC delivers at least 1W on VCONN 1b : TCPC delivers at least the power indicated in DEVICE_CAPABILITIES. VCONNPowerSupported
			0	EN_VCONN	0	RW	0b : Disable VCONN Source (default) 1b : Enable VCONN Source to CC Required

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x1D	1	CC_STATUS	7:6	Reserved	0	R	
			5	DRP_STATUS	0	R	0b : the TCPC has stopped toggling or (ROLE_CONTROL.DRP = 00) 1b : the TCPC is toggling
			4	DRP_RESULT	0	R	0b : the TCPC is presenting Rp 1b : the TCPC is presenting Rd
			3:2	CC2_STATUS	0	R	<p>If (ROLE_CONTROL.CC2 = Rp) or (DrpResult = 0) 00b : SRC.Open (Open, Rp) 01b : SRC.Ra (below maximum vRa) 10b : SRC.Rd (within the vRd range) 11b : reserved</p> <p>If (ROLE_CONTROL.CC2 = Rd) or (DrpResult = 1) 00b : SNK.Open (Below maximum vRa) 01b : SNK.Default (Above minimum vRd-Connect) 10b : SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A 11b : SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A</p> <p>If ROLE_CONTROL.CC2 = Ra, this field is set to 00b If ROLE_CONTROL.CC2 = Open, this field is set to 00b</p> <p>This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVconn = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.</p>
1:0	CC1_STATUS	0	R	<p>If (ROLE_CONTROL.CC1 = Rp) or (DrpResult = 0) 00b : SRC.Open (Open, Rp) 01b : SRC.Ra (below maximum vRa) 10b : SRC.Rd (within the vRd range) 11b : reserved</p> <p>If (ROLE_CONTROL.CC1 = Rd) or DrpResult = 1) 00b : SNK.Open (Below maximum vRa) 01b : SNK.Default (Above minimum vRd-Connect) 10b : SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A 11b : SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A</p> <p>If ROLE_CONTROL.CC1 = Ra, this field is set to 00b If ROLE_CONTROL.CC1 = Open, this field is set to 00b</p> <p>This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVconn = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.</p>			



Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x1E	1	POWER_STATUS	7	DBG_ACC_CONNECT	0	R	Not support.
			6	TCPC_INITIAL	0	R	0b : The TCPC has completed initialization and all registers are valid 1b : The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh
			5	SRC_HV	0	R	0b : vSafe5V 1b : High Voltage
			4	SRC_VBUS	0	R	0b : Sourcing Vbus is disabled 1b : Sourcing Vbus is enabled
			3	VBUS_PRESENT_DET	0	R	0b : VBUS Present Detection Disabled 1b : VBUS Present Detection Enabled (default)
			2	VBUS_PRESENT	0	R	0b : VBUS Disconnected 1b : VBUS Connected
			1	VCONN_PRESENT	0	R	0b : VCONN is not present 1b : This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V
			0	SINK_VBUS	0	R	0b : Sink is Disconnected (Default and if not supported) 1b : TCPC is sinking VBUS to the system load
0x1F	1	FAULT_STATUS	7	VCON_OV	0	RW	0b : Not in an over-voltage protection state 1b : Over-voltage fault latched.
			6	FORCE_OFF_VBUS	0	RW	0b : No Fault Detected, no action (default and not supported) 1b : VBUS Source/Sink has been forced off due to external fault
			5	AUTO_DISC_FAIL	0	RW	0b : No discharge failure 1b : Discharge commanded by the TCPM failed
			4	FORCE_DISC_FAIL	0	RW	0b : No discharge failure 1b : Discharge commanded by the TCPM failed.
			3	VBUS_OC	0	RW	0b : Not in an over-current protection state 1b : Over-current fault latched
			2	VBUS_OV	0	RW	0b : Not in an over-voltage protection state 1b : Over-voltage fault latched.
			1	VCON_OC	0	RW	0b : No Fault detected 1b : Over current VCONN fault latched
			0	I2C_ERROR	0	RW	

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x20	1		7:0	Reserved	0	R	
0x21	1		7:0	Reserved	0	R	
0x22	1		7:0	Reserved	0	R	
0x23	1	COMMAND	7:0	COMMAND	0	W	0010 0010b DisableVbusDetect. 0011 0011b EnableVbusDetect 0100 0100b DisableSinkVbus 0101 0101b Enable SinkVbus. 0110 0110b DisableSourceVbus. 0111 0111b SourceVbusDefaultVoltage. 1000 1000b SourceVbusHighVoltage.
0x24	1	DEVICE_CAPABILITIES_1L	7:5	ROLES_SUPPORT	110	R	000b : Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b : Source only 010b : Sink only 011b : Sink with accessory support (optional) 100b: DRP only 101b : Adapter or Cable (Ra) only 110b : Source, Sink, DRP, Adapter/Cable all supported 111b : Not valid
			4	ALL_SOP_SUPPORT	1	R	0b : All SOP* except SOP'_DBG/SOP''_DBG 1b : All SOP* messages are supported
			3	SOURCE_VCONN	1	R	0b : TCPC is not capable of switching VCONN 1b : TCPC is capable of switching VCONN
			2	CPB_SINK_VBUS	1	R	0b : TCPC is not capable controlling the sink path to the system load 1b : TCPC is capable of controlling the sink path to the system load
			1	SOURCE_HV_VBUS	1	R	0b : TCPC is not capable of controlling the source high voltage path to VBUS 1b : TCPC is capable of controlling the source high voltage path to VBUS
			0	SOURCE_VBUS	1	R	0b : TCPC is not capable of controlling the source path to VBUS 1b : TCPC is capable of controlling the source path to VBUS

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x25	1	DEVICE_CAPABILITIES_1H	7	Reserved	0	R	
			6	CPB_VBUS_OC	1	R	0b : VBUS OCP is not reported by the TCPC 1b : VBUS OCP is reported by the TCPC
			5	CPB_VBUS_OV	1	R	0b : VBUS OVP is not reported by the TCPC 1b : VBUS OVP is reported by the TCPC
			4	CPB_BLEED_DISC	1	R	0b : No Bleed Discharge implemented in TCPC 1b : Bleed Discharge is implemented in the TCPC
			3	CPB_FORCE_DISC	1	R	0b : No Force Discharge implemented in TCPC 1b : Force Discharge is implemented in the TCPC
			2	VBUS_MEASURE_ALARM	1	R	0b : No VBUS voltage measurement nor VBUS Alarms 1b : VBUS voltage measurement and VBUS Alarms
			1:0	SOURCE_RP_SUPPORT	10	R	00b : Rp default only 01b : Rp 1.5A and default 10b : Rp 3.0A, 1.5A, and default 11b : Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register