



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



ARM® RVI™ and RVT™

Setting up the Hardware



ARM RVI and RVT

Setting up the Hardware

Copyright © 2010 ARM. All rights reserved.

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
May 2010	A	Non-confidential	First release.
November 2010	B	Non-confidential	Second release.

Proprietary Notice

Words and logos marked with ® or ™ are registered trademarks or trademarks of ARM® in the EU and other countries, except as otherwise stated below in this proprietary notice. Other brands and names mentioned herein may be the trademarks of their respective owners.

Neither the whole nor any part of the information contained in, or the product described in, this document may be adapted or reproduced in any material form except with the prior written permission of the copyright holder.

The product described in this document is subject to continuous developments and improvements. All particulars of the product and its use contained in this document are given by ARM in good faith. However, all warranties implied or expressed, including but not limited to implied warranties of merchantability, or fitness for purpose, are excluded.

This document is intended only to assist the reader in the use of the product. ARM shall not be liable for any loss or damage arising from the use of any information in this document, or any error or omission in such information, or any incorrect use of the product.

Where the term ARM is used it means “ARM or any of its subsidiaries as appropriate”.

This product includes software developed by the Apache Software Foundation (see <http://www.apache.org>).

Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

Web Address

<http://www.arm.com>

Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity



The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling ARM RVI and RVT equipment.

The ARM RVI and RVT modules generate, use, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- ensure attached cables do not lie across the target board
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- consult the dealer or an experienced radio/TV technician for help

Note

It is recommended that wherever possible shielded interface cables be used.

Contents

ARM RVI and RVT Setting up the Hardware

Chapter 1	Conventions and feedback	
Chapter 2	Introduction to RVI and RVT	
2.1	About RVI and RVT	2-2
2.2	RVI product contents	2-3
2.3	RVT and RVT2 product contents	2-4
2.4	RVI and RVT availability and compatibility	2-5
2.5	Introduction to EmbeddedICE logic and debug extensions	2-6
2.6	Debug extensions to the ARM processor	2-7
2.7	EmbeddedICE debug architecture and debug monitor differences	2-8
2.8	Introduction to the RVI components	2-9
2.9	The RVI debug unit	2-10
2.10	RVI hardware variants - end panel elements	2-12
2.11	RVI hardware variants - v2 LVDS probe	2-13
2.12	The RVI firmware	2-15
2.13	The RVI host software	2-16
2.14	RVT front panel components	2-17
2.15	RVT2 front panel components	2-18
Chapter 3	System requirements for using RVI and RVT	
3.1	Host software requirements	3-2
3.2	Host hardware requirements	3-3
3.3	Target hardware requirements	3-4
3.4	Connecting the RVI hardware	3-5
3.5	Using nonstandard connectors	3-8
3.6	Hot-plugging and unplugging the JTAG cable	3-9
3.7	Connecting the RVT hardware	3-10
3.8	Using RVI and RVT	3-14

Chapter 1

Conventions and feedback

The following describes the typographical conventions and how to give feedback:

Typographical conventions

The following typographical conventions are used:

`monospace` Denotes text that can be entered at the keyboard, such as commands, file and program names, and source code.

monospace Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.

monospace italic

Denotes arguments to commands and functions where the argument is to be replaced by a specific value.

`monospace bold`

Denotes language keywords when used outside example code.

italic Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold Highlights interface elements, such as menu names. Also used for emphasis in descriptive lists, where appropriate, and for ARM® processor signal names.

Feedback on this product

If you have any comments and suggestions about this product, contact your supplier and give:

- your name and company

- the serial number of the product
- details of the release you are using
- details of the platform you are using, such as the hardware platform, operating system type and version
- a small standalone sample of code that reproduces the problem
- a clear explanation of what you expected to happen, and what actually happened
- the commands you used, including any command-line options
- sample output illustrating the problem
- the version string of the tools, including the version number and build numbers.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

- the title
- the number, ARM DUI 0515B
- if viewing online, the topic names to which your comments apply
- if viewing a PDF version of a document, the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

ARM periodically provides updates and corrections to its documentation on the ARM Information Center, together with knowledge articles and *Frequently Asked Questions* (FAQs).

Other information

- ARM Information Center, <http://infocenter.arm.com/help/index.jsp>
- ARM Technical Support Knowledge Articles, <http://infocenter.arm.com/help/topic/com.arm.doc.faqs/index.html>
- ARM Support and Maintenance, <http://www.arm.com/support/services/support-maintenance.php>.

Chapter 2

Introduction to RVI and RVT

The following topics introduce ARM® RVI™ and RVT™, and describe the software components:

- *About RVI and RVT on page 2-2*
- *RVI product contents on page 2-3*
- *RVT and RVT2 product contents on page 2-4*
- *RVI and RVT availability and compatibility on page 2-5*
- *Introduction to EmbeddedICE logic and debug extensions on page 2-6*
- *Debug extensions to the ARM processor on page 2-7*
- *EmbeddedICE debug architecture and debug monitor differences on page 2-8*
- *Introduction to the RVI components on page 2-9*
- *The RVI debug unit on page 2-10*
- *RVI hardware variants - end panel elements on page 2-12*
- *RVI hardware variants - v2 LVDS probe on page 2-13*
- *The RVI firmware on page 2-15*
- *The RVI host software on page 2-16*
- *RVT front panel components on page 2-17.*

2.1 About RVI and RVT

The ARM RVI debug unit enables your debugger to connect to ARM processor-based targets using JTAG or *Serial-Wire Debug* (SWD).

RVI provides the software and hardware interface between a debugger running on a Windows or Red Hat Linux host computer, and a *Joint Test Action Group* (JTAG) *IEEE Standard 1149.1-2001* port on the target hardware.

RVI also supports a *Serial Wire Debug* (SWD) connection to the *Debug Access Port* (DAP). SWD is an alternative protocol to JTAG for connecting to CoreSight™ processors, and has the advantage of requiring fewer pins than previous probes. It also supports higher data rates.

The RVT trace capture unit connects to the trace port of an ARM processor-based target to extract trace data off-chip.

The RVT2 trace capture unit connects to the trace port of an ARM processor-based target to extract trace data off-chip, either storing it onto its 24MB buffer or streaming it to the host computer to enable hardware platform profiling.

The RVT or RVT2 unit works in conjunction with RVI to provide real-time trace functionality for software running on *System-on-Chip* (SoC) devices with deeply embedded processors that contain the *Embedded Trace Macrocell*™ (ETM) logic.

You can use RVI and RVT or RVT2 with systems that contain one or more ARM processors. RVI also supports the *Embedded Trace Buffer*™ (ETB) for capturing small amounts of trace information at high processor clock speeds.

2.1.1 See also

Concepts

- [RVI product contents on page 2-3](#)
- [RVT and RVT2 product contents on page 2-4](#)
- [RVI and RVT availability and compatibility on page 2-5](#)
- [Introduction to EmbeddedICE logic and debug extensions on page 2-6](#)
- [Introduction to the RVI components on page 2-9.](#)

Reference

Using the Debug Hardware Configuration Utilities:

- [Using Trace, ../com.arm.doc.dui0498b/I999867.html](#)

2.2 RVI product contents

The ARM RVI product comprises:

- An RVI debug unit that connects to your target board over a JTAG interface and to your PC using either USB or Ethernet.
 - Mains cables and a power supply that powers the RVI unit.
 - An Ethernet cable.
 - A USB cable.
 - Two alternative cables that connect RVI to the target JTAG connector:
 - a short 20-way ribbon cable
 - a long 40-way ribbon cable and a *Low Voltage Differential Signaling (LVDS)* 40-way to 20-way probe.
 - A TI adaptor board.
 - A 20-way to 14-way adaptor, for targets that use a 14-way *Insulation Displacement Connector (IDC)* box header.
- Caution**
- Before using this adaptor, see *Using nonstandard connectors* for more information.
-
- Software on CD-ROM that enables a debugger to communicate with the RVI unit, and to configure and manage the RVI unit.
 - Documentation, including:
 - online versions of this document in Eclipse browser and PDF formats
 - a packing list.

2.2.1 See also

Tasks

- [Connecting the RVI hardware on page 3-5](#)
- [Using nonstandard connectors on page 3-8](#)

Concepts

- [About RVI and RVT on page 2-2](#)
- [RVT and RVT2 product contents on page 2-4](#)
- [RVI and RVT availability and compatibility on page 2-5](#)
- [Introduction to EmbeddedICE logic and debug extensions on page 2-6](#)
- [Introduction to the RVI components on page 2-9.](#)

2.3 RVT and RVT2 product contents

Unless specifically stated, RVT is used throughout to refer to both RVT and RVT2.

The RVT product comprises:

- The RVT trace capture unit.
- Eight plastic spacers (four 16mm and four 8mm), supplied with the RVT.
- The 60-way interface cable (a flat ribbon cable with a square *Insulation Displacement Connector* (IDC) socket at each end).
- The trace probe. This is a small PCB that contains the interface circuits that buffer the signals between the target board and the interface cable.
- A power supply unit is not supplied, because RVT is powered by the unit.
- For 32-bit trace using RVT2, you also require a 32-bit dual-Mictor trace probe (Part Number RT200-BD-00032).

When considering your system requirements, you must also provide some target hardware containing a device supported by RVT.

2.3.1 See also

Tasks

- [Connecting the RVT hardware on page 3-10.](#)

Concepts

- [About RVI and RVT on page 2-2](#)
- [RVI product contents on page 2-3](#)
- [RVI and RVT availability and compatibility on page 2-5](#)
- [Introduction to EmbeddedICE logic and debug extensions on page 2-6](#)
- [Introduction to the RVI components on page 2-9.](#)

2.4 RVI and RVT availability and compatibility

RVI and RVT are available from ARM and its resellers.

Contact ARM directly regarding OEM licenses.

The RVI software for the host computer is compatible with 32-bit versions of the following operating systems:

- Windows XP Professional (Service Pack 2, or later)
- Windows Vista Business Edition and Windows Vista Enterprise Edition
- Red Hat Enterprise Linux 4 and Red Hat Enterprise Linux 5

RVI provides:

- The ability to access the target hardware.
- Tools to configure your debugger so that it can connect to the target through RVI. Your debugger provides the user interface items, such as register windows and disassemblers, that make it possible to debug your application.

For more information on compatibility with target hardware, see the documentation supplied with your hardware.

2.4.1 See also

Concepts

- [About RVI and RVT on page 2-2](#)
- [Introduction to EmbeddedICE logic and debug extensions on page 2-6](#)
- [Introduction to the RVI components on page 2-9.](#)

Other information

- Patch downloads, <http://www.arm.com/support>

2.5 Introduction to EmbeddedICE logic and debug extensions

The EmbeddedICE[®] logic and the ARM processor debug extensions enable RVI to debug software running on an ARM processor. The basic principles of this operation are described in the following:

- [Debug extensions to the ARM processor on page 2-7](#)
- [EmbeddedICE debug architecture and debug monitor differences on page 2-8.](#)

Note

To determine whether a specific ARM processor has support for JTAG debugging, see its datasheet or technical reference manual.

2.5.1 See also

Concepts

- [About RVI and RVT on page 2-2](#)
- [RVI and RVT availability and compatibility on page 2-5](#)
- [Debug extensions to the ARM processor on page 2-7](#)
- [EmbeddedICE debug architecture and debug monitor differences on page 2-8](#)
- [Introduction to the RVI components on page 2-9.](#)

Reference

ARM[®] DSTREAM[™] and RVI[™] Using the Debug Hardware Configuration Utilities:

- [Using Trace, ../com.arm.doc.dui0498b/I999867.html](#)

2.6 Debug extensions to the ARM processor

The debug extensions consist of several scan chains around the processor, and some additional signals that are used to control the behavior of the processor for debug purposes. The most significant of these additional signals are:

- BREAKPT** This processor signal enables external hardware to halt processor execution for debug purposes. When HIGH during an instruction fetch, the instruction is tagged as breakpointed, and the processor stops if this instruction reaches the execute stage of the pipeline.
- DBGRRQ** This processor signal is a level-sensitive input that causes the processor to enter debug state when the current instruction has completed.
- DBGACK** This processor signal is an output from the processor that goes HIGH when the processor is in debug state so that external devices can determine the current state of the processor.

RVI uses these, and other signals, through the debug interface of the processor, for example by writing to the control register of the EmbeddedICE logic. For more details, see the topic that describes the debug interface support of the ARM datasheet or technical reference manual for your processor (for example, the *ARM7TDMI (Rev 4) Technical Reference Manual*).

2.6.1 See also

Concepts

- [EmbeddedICE debug architecture and debug monitor differences on page 2-8.](#)

2.7 EmbeddedICE debug architecture and debug monitor differences

A debug monitor is an application that runs on your target hardware in conjunction with your application, and requires target resources (for example, memory, access to exception vectors, and timers) to be available.

The EmbeddedICE debug architecture requires almost no resources. Rather than being an application on the board, it works by using:

- additional debug hardware within the processor, to enable the host to communicate with the target
- an external run control unit that buffers and translates the processor signals into something that is usable by a host computer.

The EmbeddedICE debug architecture enables debugging to be as non-intrusive as possible:

- the target being debugged requires very little special hardware to support debugging
- in most cases you do not have to set aside memory for debugging in the system being debugged and you do not have to incorporate special software into the application
- execution of the system being debugged is only halted when a breakpoint unit is triggered, or you request that execution is halted.

2.7.1 See also

Concepts

- [Debug extensions to the ARM processor on page 2-7.](#)

2.8 Introduction to the RVI components

The following topics introduce the components of the RVI product, and describe how they fit together:

- [The RVI debug unit on page 2-10](#)
- [The RVI firmware on page 2-15](#)
- [The RVI host software on page 2-16.](#)

2.8.1 See also

Concepts

- [About RVI and RVT on page 2-2](#)
- [RVI and RVT availability and compatibility on page 2-5](#)
- [Introduction to EmbeddedICE logic and debug extensions on page 2-6.](#)

Reference

Using the Debug Hardware Configuration Utilities:

- [Using Trace, ../com.arm.doc.dui0498b/I999867.html](#)

2.9 The RVI debug unit

The RVI debug unit provides the hardware to enable a computer to control multiple JTAG capable devices. The unit has ports at one end for connecting to the host computer and to a power source. These ports are shown in the following figure:

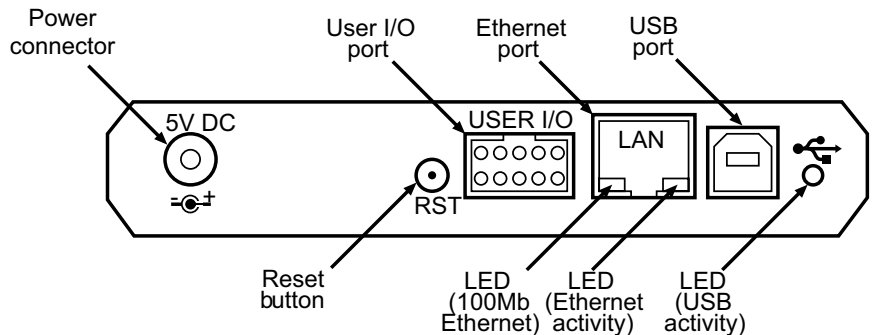


Figure 2-1 Ports for connecting to the host computer

The RST button is used to reset the RVI unit when required, and returns RVI to its power-up state. Using the RST button in this way does not reset the target. This button must not be confused with the Reset button that might be implemented on your target, located on the target board itself.

———— **Note** ————

When using v3.0 or later RVI hardware in conjunction with a v2 *Low Voltage Differential Signaling* (LVDS) probe, resetting RVI or power-cycling RVI does not cause a target reset. Any other hardware combination, however, might cause a target reset.

The LEDs at the bottom of the Ethernet port display information about Ethernet speed and activity:

- The green LED shows the Ethernet speed. When Off, it indicates a speed of 10Mbps, and when On indicates a speed of 100Mbps.
- The yellow LED indicates that activity is taking place.

The ports at the other end of the unit connect to the target hardware, and are shown in the following figure:

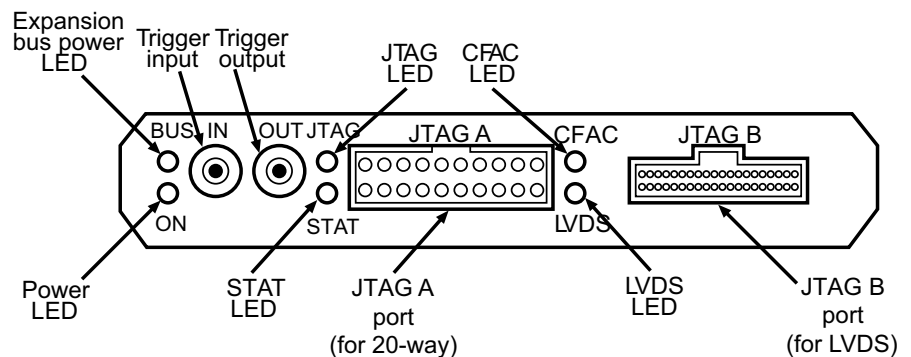


Figure 2-2 Ports for connecting to the target hardware

Cables are supplied to connect the run control unit to the host computer, and to the target hardware.

Note

RVI does not currently support the Trigger input and Trigger output signals.

If the RVI unit detects an internal hardware or software failure from which it cannot recover, the four LEDs JTAG, STAT, CFAC and LVDS flash continuously. You must reboot RVI before you can continue using it. To do this, press the RST button.

During installation of an update or a patch, the CFAC LED lights up, denoting that *Compact Flash Activity* (CFAC) is taking place. While this is happening, you must not disconnect power from the run control unit, and must wait until this LED has extinguished. The CFAC LED also lights up when a debugger connects, and during *Dynamic Host Configuration Protocol* (DHCP) lease renewal.

The RVI unit contains an internal cooling fan that operates to control the internal temperature when necessary. The ventilation panels on the top and bottom of the RVI unit and the RVT unit must not be obscured.

2.9.1 See also**Tasks**

ARM® DSTREAM™ and RVT™ Using the Debug Hardware Configuration Utilities:

- *Installing a firmware update or patch, [../com.arm.doc.dui0498b/Ciaihbf.html](#)*

Concepts

- *[RVI hardware variants - end panel elements](#) on page 2-12*
- *[RVI hardware variants - v2 LVDS probe](#) on page 2-13*
- *[The RVI firmware](#) on page 2-15*
- *[The RVI host software](#) on page 2-16.*

Reference

ARM® DSTREAM™ and RVT™ Using the Debug Hardware Configuration Utilities:

- *[Debugging with a target reset, ../com.arm.doc.dui0498b/CHDBIEFI.html](#)*

2.10 RVI hardware variants - end panel elements

Depending on the hardware unit that you are using, it is possible that the features of your unit might be different in appearance or functionality from those generally referred to. In units used with software earlier than RVI v3.0, the end panel elements of the unit for the host computer port connections are arranged as shown in the following figure:

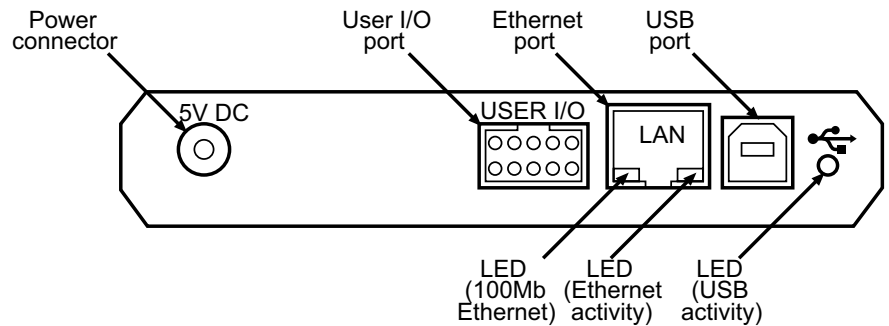


Figure 2-3 Pre-v3.0 host computer ports end panel

An example of the target hardware ports of the end panel of the unit is shown in the following figure:

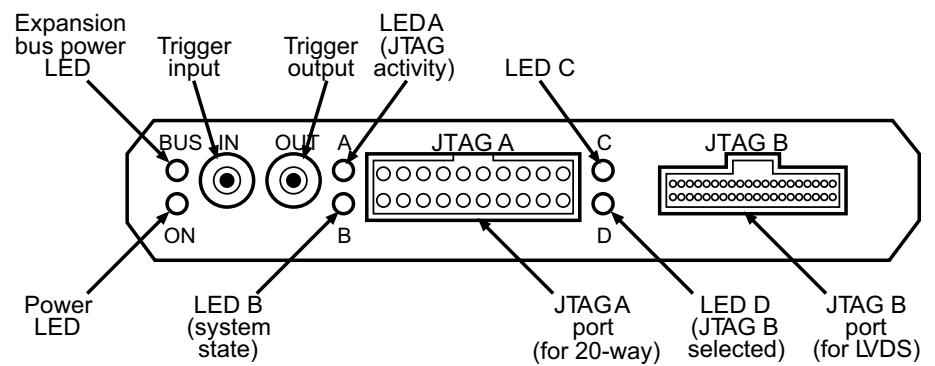


Figure 2-4 Target hardware ports end panel

2.10.1 See also

Concepts

- [The RVI debug unit on page 2-10.](#)

2.11 RVI hardware variants - v2 LVDS probe

The RVI unit comprises a v2 *Low Voltage Differential Signaling* (LVDS) probe. The probe is visibly different by the presence of two colored LEDs that signify the status of the activity taking place.

The functionality of the v3.1 probe enables you to make a *Serial Wire Debug* (SWD) connection to the *Debug Access Port* (DAP).

The following figure shows the dimensions of the LVDS probe and its LED locations:

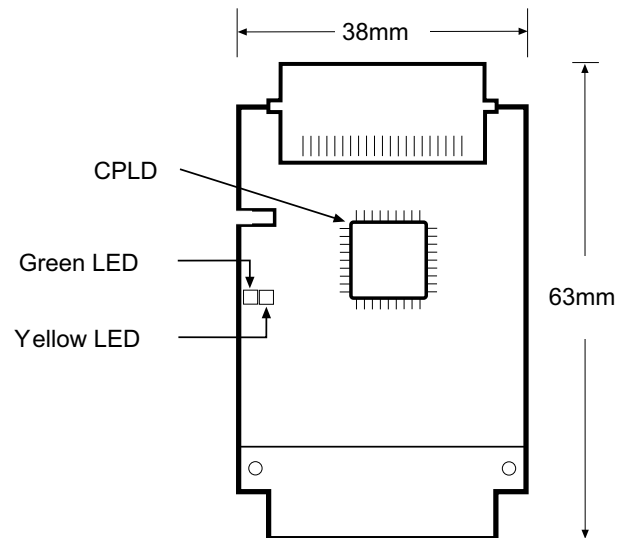


Figure 2-5 LVDS probe LEDs and dimensions

The following table provides a diagnostic means to determine the type of activity taking place, according to the permutations of the green and yellow LEDs:

Table 2-1 Diagnostic table

Green	Yellow	Power	CPLD OK	JTAG mode	SW Mode	JTAG Activity	SW Activity
Off	Off	No	N/A	N/A	N/A	N/A	N/A
Dim	Dim	Yes	No	N/A	N/A	N/A	N/A
On	On	Yes	Yes	N/A	N/A	N/A	N/A
Off	On	Yes	Yes	Yes	No	No	N/A
Flicker	On	Yes	Yes	Yes	No	Yes	N/A
On	Off	Yes	Yes	No	Yes	N/A	No
On	Flicker	Yes	Yes	No	Yes	N/A	Yes

RVI v4.0 supports the SWD debugging protocol as an alternative to JTAG. SWD can only be used with the LVDS probe, and without using the JTAG ribbon cable. The probe must be a v2 type as described, and you might have to upgrade its firmware.

As shown in the previous figure, compatible probes have two LEDs on their front left-hand side. At power-up, both LEDs are lit. If only the yellow LED is lit, you must upgrade the probe to make it SWD-capable.

In addition, if your probe does not appear to have a CPLD located as shown in the previous figure, it means that your probe is of the v1.5 type, and must be replaced if SWD-compatibility is required. To upgrade your probe to the v2 type, contact ARM for more information.

SWD supports only a single DAP and not a chain of devices. The graphical representation of the target system changes to represent this when SWD is selected.

———— **Note** —————

The v2 LVDS probe is supplied as standard with RVI v3.1 and later units. The probe can also be used with a RVI v3.0 unit, if you update it with a firmware patch that provides support for the v3.1 probe.

2.11.1 See also

Reference

ARM RVI System and Interface Design Reference:

- [Chapter 7 Serial Wire Debug.](#)

ARM® DSTREAM™ and RVT™ Using the Debug Hardware Configuration Utilities:

- [Installing a firmware update or patch, ../com.arm.doc.dui0498b/Ciaihbf.html](#)
- [Upgrading an LVDS probe, ../com.arm.doc.dui0498b/BABBHIAC.html](#)

2.12 The RVI firmware

The RVI firmware is located in the RVI debug unit. It receives commands from the RVI host software and translates them into JTAG accesses. The RVI firmware contains specific sections of code for each ARM[®] processor. These are called templates.

You can update the RVI firmware using the RVI Update application in the following ways:

- for firmware fixes, you can obtain firmware patches from the ARM web site
- for firmware updates that add new functionality, such as additional templates, you must obtain a new CD that also contains updates to the host software

2.12.1 See also

Concepts

- *The RVI debug unit on page 2-10*
- *The RVI host software on page 2-16.*

ARM[®] DSTREAM[™] and RVI[™] Using the Debug Hardware Configuration Utilities:

- *Managing the firmware on your debug hardware unit,*
[../com.arm.doc.dui0498b/Ciadfiba.html](#)

Other information

- ARM patch downloads, <http://www.arm.com/support>

2.13 The RVI host software

The RVI host software provides the interface between your debugger and the RVI unit that controls the JTAG devices. It translates debugger commands, such as start, stop, and download, into JTAG control sequences for a particular processor. The RVI software provides support for debugging on a wide range of ARM processors. To see a list of supported processors, open the RVI Update application and expand the **JTAG Templates** and **ARM** trees. A list of templates for all supported processors is displayed.

The RVI software can address each JTAG device individually, without affecting other devices on the board. It uses this ability to create virtual connections for each of the JTAG devices on the board. Your debugger can attach to one of these virtual connections, and perform debugging operations with no knowledge of the other devices on the board.

The RVI software enables multiple concurrent connections. You can debug multiprocessor systems, and for more information see the documentation that accompanies your debugger. The software can also perform a synchronized start or stop of processors, for debugging multiprocessor systems where the processors interact with each other.

The RVI software also supports connections across a network, so that you can run the debugging software on several different computers.

2.13.1 See also

Concepts

- [The RVI debug unit on page 2-10](#)
- [The RVI firmware on page 2-15.](#)

ARM® DSTREAM™ and RVT™ Using the Debug Hardware Configuration Utilities:

- *Managing the firmware on your debug hardware unit,*
[../com.arm.doc.dui0498b/Ciadfiba.html](#)

2.14 RVT front panel components

In RVT, the layout of the RVT front panel is as shown in the following figure:

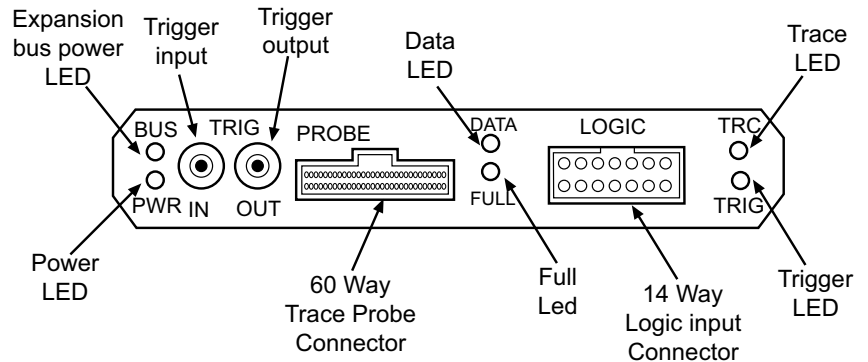


Figure 2-6 RVT front panel layout

The components comprise LEDs and trace probe connectors.

———— **Note** ————

The Trigger input, Trigger output and Logic connectors are not currently supported by RVI.

The LEDs on the front panel of the RVT unit have the following functions:

- PWR** The PWR LED indicates that the RVT unit is powered up. This is always lit when the unit is powered from its own external power supply. When RVT is powered by RVI, the Power LED is lit only when RVI is initializing the RVT unit.
- BUS** The BUS LED indicates module initialization and RVI expansion bus power. It lights up when RVI is initializing the RVT unit, and remains lit while the RVI expansion bus is powered. The BUS LED flashes on a module connected to RVI through the expansion bus if an error is detected in trying either to identify the module or to provide power to it. Modules might require more power than RVI can provide, in which case the module must be separately powered. If the module is separately powered and this LED flashes, it indicates a problem in identifying the module.
- DATA** The DATA LED indicates that the RVT module has data in its buffer
- FULL** The FULL LED indicates that the RVT module data buffer is full.
- TRC** The TRC LED indicates that the RVT module has enabled the buffer for capture.
- TRIG** The TRIG LED indicates that the RVT module has triggered.

2.14.1 See also

Reference

System and Interface Design Reference:

- [Trace signals on page 5-2.](#)

Other information

- ETMv1 and ETMv3 architecture pinouts,
<http://infocenter.arm.com/help/topic/com.arm.doc.ih0014-/index.html>

2.15 RVT2 front panel components

In RVT2, the layout of the RVT2 front panel is as shown in the following figure:

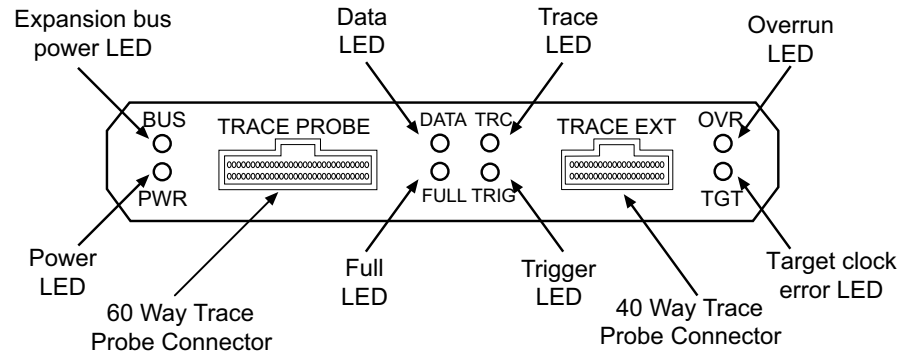


Figure 2-7 RVT2 front panel layout

The components comprise LEDs and trace probe connectors.

The LEDs on the front panel of the RVT2 unit have the following functions:

- PWR** The PWR LED indicates that the RVT2 unit is powered up. This is always lit when the unit is powered from its own external power supply. When RVT2 is powered by RVI, the Power LED is lit only when RVI is initializing the RVT2 unit.
- BUS** The BUS LED indicates module initialization and RVI expansion bus power. It lights up when RVI is initializing the RVT unit, and remains lit while the RVI expansion bus is powered. The BUS LED flashes on a module connected to RVI through the expansion bus if an error is detected in trying either to identify the module or to provide power to it. Modules might require more power than RVI can provide, in which case the module must be separately powered. If the module is separately powered and this LED flashes, it indicates a problem in identifying the module.
- DATA** The DATA LED indicates that the RVT2 module has data in its buffer.
- FULL** The FULL LED indicates that the RVT2 module data buffer is full.
- TRC** The TRC LED indicates that the RVT2 module has enabled the buffer for capture.
- TRIG** The TRIG LED indicates that the RVT2 module has triggered.
- OVR** The OVR LED indicates that the streaming trace has overrun the available USB bandwidth. When this occurs, this LED flashes.
- TGT** The TGT LED indicates if there is a problem with the target. If the target present line is low, or if there is no clock, this LED flashes.

2.15.1 See also

Reference

ARM® RVI™ and RVT™ System and Interface Design Reference:

- [Trace signals on page 5-2.](#)

Other information

- ETMv1 and ETMv3 architecture pinouts,
<http://infocenter.arm.com/help/topic/com.arm.doc.ih0014-/index.html>

Chapter 3

System requirements for using RVI and RVT

The following topics describe the system requirements for ARM® RVI™, and how to connect the RVI hardware to your host computer and target system. The topics also describe how to use some common parts of the RVI software:

- *Host software requirements on page 3-2*
- *Host hardware requirements on page 3-3*
- *Target hardware requirements on page 3-4*
- *Connecting the RVI hardware on page 3-5*
- *Using nonstandard connectors on page 3-8*
- *Hot-plugging and unplugging the JTAG cable on page 3-9*
- *Connecting the RVT hardware on page 3-10*
- *Using RVI and RVT on page 3-14.*