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## Programmable USB Type-C PD Controller

### General Description

The RT1715 is a USB Type-C controller that complies with the latest USB Type-C and PD standards. The RT1715 integrates a complete Type-C Transceiver including the Rp and Rd resistors. It does the USB Type-C detection including attach and orientation. The RT1715 integrates the physical layer of the USB BMC power delivery protocol to allow up to 100W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

### Ordering Information

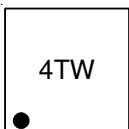
RT1715 □  
 Package Type  
 WSC : WL-CSP-9B 1.38x1.34 (BSC)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

### Marking Information



4T : Product Code  
 W : Date Code

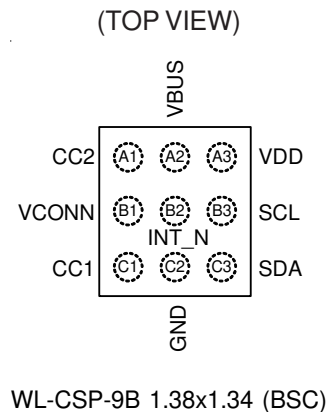
### Features

- Dual-Role PD Compatible
- Attach/Detach Detection as Host, Device or DRP
- Current Capability Definition and Detection
- Cable Recognition
- Alternate Mode Support
- Supporting VCONN with Programmable OCP
- Dead Battery Support
- Ultra-Low Power Mode for Attach Detection
- Simple I<sup>2</sup>C Interface with AP or EC
- BIST Mode Supported
- Supported PD 3.0 except Fast Role Swap Function
- e-fuse IP
- 9-Ball WL-CSP Package

### Applications

- Smartphones
- Tablets
- Laptops

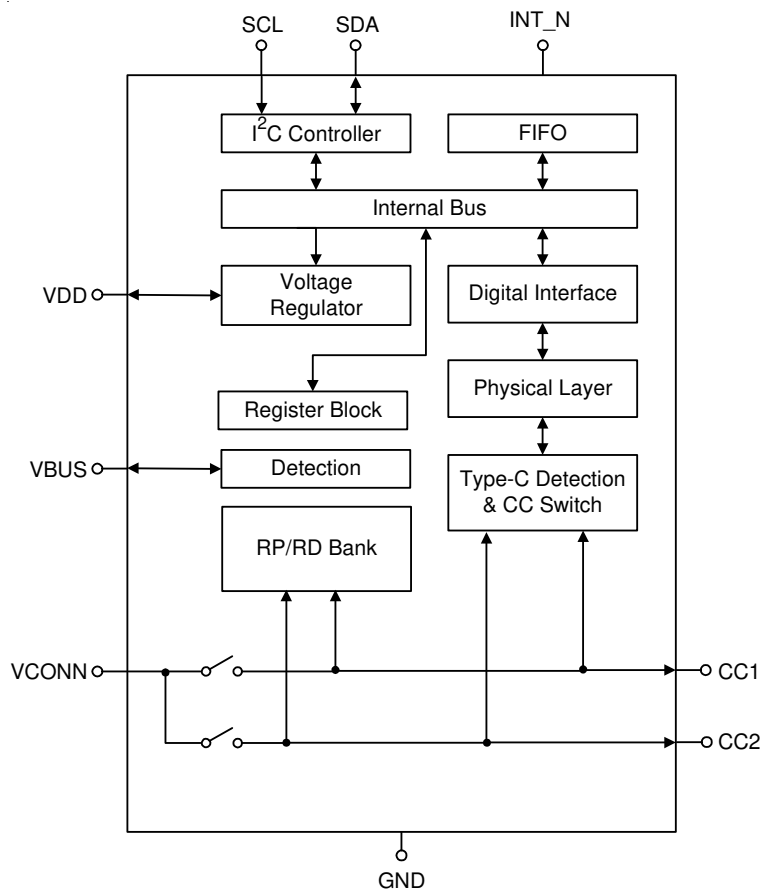
### Pin Configuration



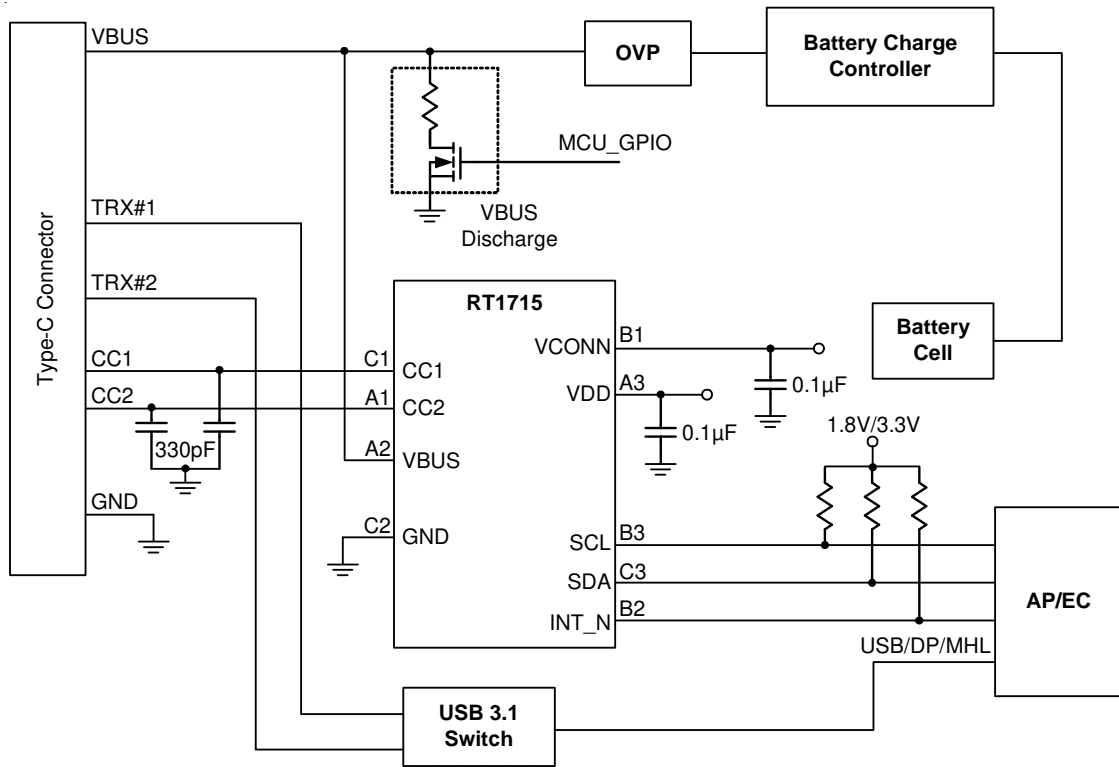
Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	CC2	Type-C Connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation detected.
A2	VBUS	VBUS input pin for attach and detach detection when operating as an UFP port (Device).
A3	VDD	Input supply voltage.
B1	VCONN	Regulated input pin to be switched to correct CC pin as VCONN to power Type-C full-featured cables and other accessories.
B2	INT_N	Active low and open drain type interrupt output used to prompt the processor to read the registers.
B3	SCL	I <sup>2</sup> C serial data signal to be connected to the I <sup>2</sup> C master.
C1	CC1	Type-C Connector Configuration Channel (CC) Pins. Initially used to determine when an attach has occurred and what the orientation detected.
C2	GND	Ground pin.
C3	SDA	I <sup>2</sup> C serial data signal to be connected to the I <sup>2</sup> C master.

Functional Block Diagram



**Typical Application Circuit**



**Absolute Maximum Ratings** (Note 1)

- VDD/VCONN ----- -0.3V to 6V
- CC1/CC2 (Testing Condition : VDD ≥ 3V) ----- -0.3V to 24V
- CC1/CC2 (Testing Condition : VDD < 3V) ----- -0.3V to 6V
- VBUS ----- -0.3V to 28V
- SDA/SCL/INT\_N ----- -0.3V to 6V
- Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C  
 WL-CSP-9B 1.38x1.34 (BSC) ----- 1.22W
- Package Thermal Resistance (Note 2)  
 WL-CSP-9B 1.38x1.34 (BSC), θ<sub>JA</sub> ----- 81.5°C/W
- Lead Temperature (Soldering, 10sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)  
 HBM (Human Body Model) ----- 2kV

**Recommended Operating Conditions** (Note 4)

- Suply Input Voltage ----- 3.0V to 5.5V
- VCONN Input Voltage ----- 3.3V to 5.5V
- VCON Supply Current ----- 200mA to 600mA
- VCON Supply Voltage ----- 3V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

**Electrical Characteristics**

(V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Common Normative Signaling Requirements</b>						
Bit Rate	f <sub>BitRate</sub>		270	300	330	Kbps
<b>Common Normative Signaling Requirements for Transmitter</b>						
Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate	ρ <sub>BitRate</sub>		--	--	0.25	%
Time from the end of last bit of a Frame until the start of the first bit of the next Preamble	t <sub>InterFrameGap</sub>		25	--	--	μs
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line	t <sub>StartDrive</sub>		-1	--	1	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>BMC Common Normative Requirements</b>						
Time to cease driving the line after the end of the last bit of the Frame	t <sub>EndDriveBMC</sub>		--	--	23	μs
Fall Time	t <sub>Fall</sub>		300	--	--	ns
Time to cease driving the line after the final high-to-low transition	t <sub>HoldLowBMC</sub>		1	--	--	μs
Rise Time	t <sub>Rise</sub>		300	--	--	ns
Voltage Swing	V <sub>Swing</sub>		1.050	1.125	1.200	V
Transmitter Output Impedance	Z <sub>Driver</sub>		33	--	75	Ω
<b>BMC Receiver Normative Requirements</b>						
Time Window for Detecting Non-Idle	t <sub>TransitionWindow</sub>		12	--	20	μs
Receiver Input Impedance	Z <sub>BmcRx</sub>		1	--	--	MΩ
<b>Power Consumption</b>						
Stand-by Current	I <sub>SB</sub>	Cable attached (Full function on)	--	2.8	--	mA
Ultra-Low Power Mode	I <sub>UL</sub>	VCONN5V supply on, DRP toggle	--	I <sub>VDD</sub> = 20	--	μA
			--	I <sub>VCONN5V</sub> = 25	--	
		VCONN5V supply off, DRP toggle	--	10	--	
<b>Type-C Port Control</b>						
Ron for VCONN Switch	R <sub>ON</sub>	VCONN input = 3.3V, R <sub>ON</sub> = 1.3Ω	--	1	--	Ω
OCP Range	I <sub>OCP</sub>		200	--	600	mA
Time for VCONN Switch to turn-On State	t <sub>Soft</sub>		--	1.2	--	ms
DFP 80μA CC Current	DFP <sub>80μ</sub>		64	80	96	μA
DFP 180μA CC Current	DFP <sub>180μ</sub>		166	180	194	μA
DFP 330μA CC Current	DFP <sub>330μ</sub>		304	330	356	μA
UFP Rd	R <sub>d</sub>		4.59	5.10	5.61	kΩ
UFP Pull-Down Voltage in Dead Battery Under DFP80u and DFP180μA	V <sub>DBL</sub>		--	--	1.6	V
UFP Pull-Down Voltage in Dead Battery Under DFP330μA	V <sub>DBH</sub>		--	--	2.6	V
VBUS Detection Valid Voltage			--	4	--	V

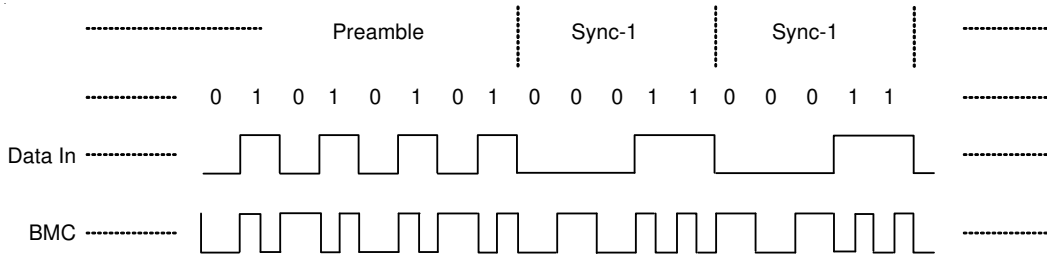
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS Measure Range			5	--	20	V
VBUS Measurement Step when VBUS Range Under 4V to 10V			--	0.5	--	V
VBUS Measurement Step when VBUS Range Under 10V to 20V			--	1	--	V
<b>I<sup>2</sup>C Electrical Characteristics</b>						
I <sup>2</sup> C Bus Supply Voltage	I <sup>2</sup> C_VDD		1.5	--	3.6	V
LOW-Level Input Voltage	V <sub>IL</sub>		--	--	0.4	V
HIGH-Level Input Voltage	V <sub>IH</sub>		1.3	--	--	V
LOW-Level Output Voltage	V <sub>OL</sub>	Open-drain	--	--	0.4	V
Input Current Each IO Pin	I <sub>I</sub>	0.1V <sub>DD</sub> < V <sub>I</sub> < 0.9V <sub>DDMAX</sub>	-10	--	10	μA
SCL Clock Frequency	f <sub>SCL</sub>		0	--	3400	kHz
Pulse width of spikes that must be suppressed by the input filter	t <sub>SP</sub>		--	--	50	ns
Data Hold Time	t <sub>HD:DAT</sub>		30	--	--	ns
Data Set-Up Time	t <sub>SU:DAT</sub>		70	--	--	ns

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

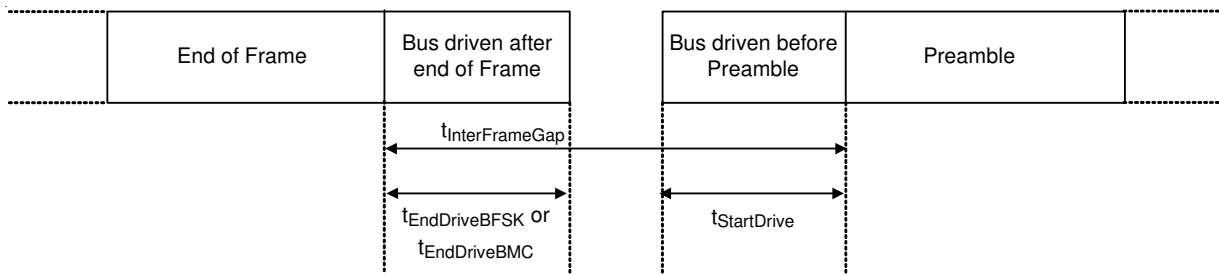
**Note 2.** θ<sub>JA</sub> is measured under natural convection (still air) at T<sub>A</sub> = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

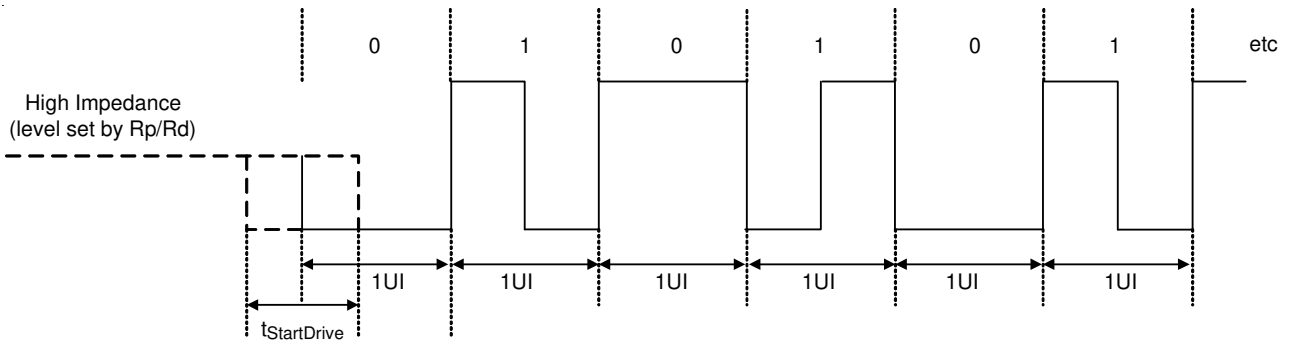
**Note 4.** The device is not guaranteed to function outside its operating conditions.



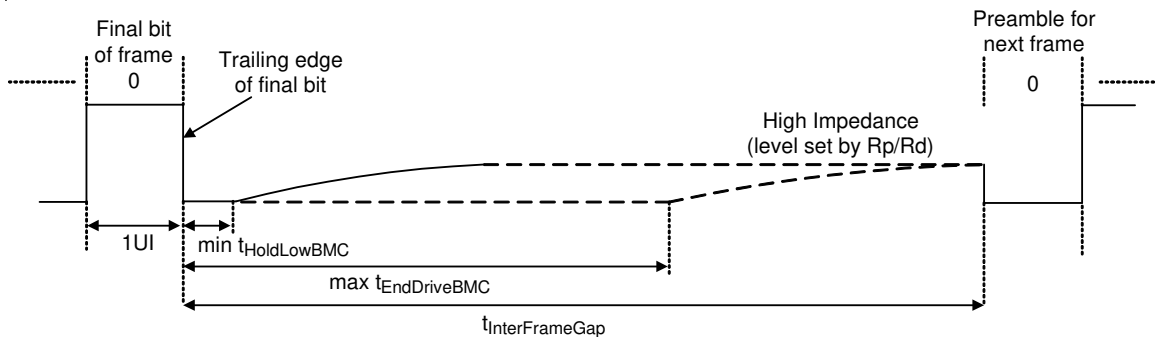
BMC Example



Inter-Frame Gap Timings



BMC Encoded Start of Preamble

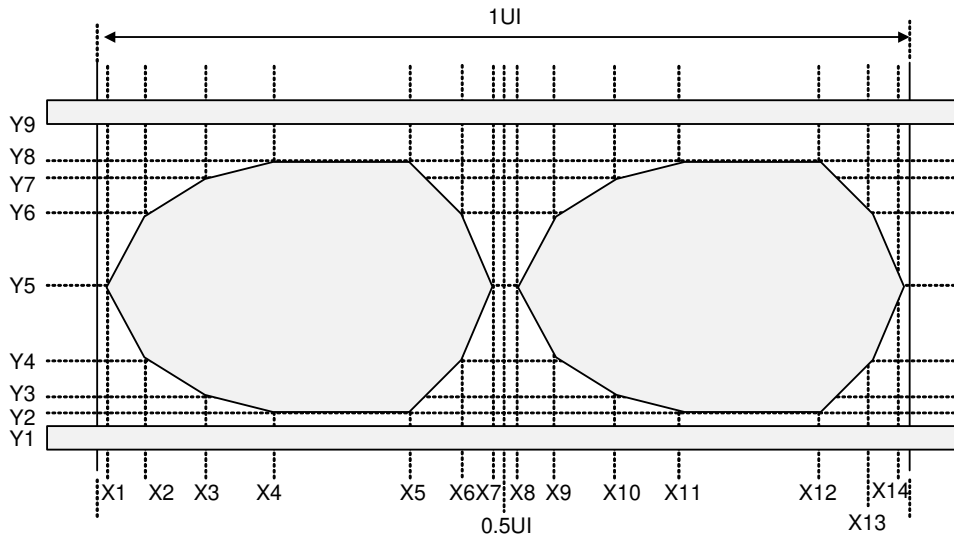


Transmitting or Receiving BMC Encoded Frame Terminated

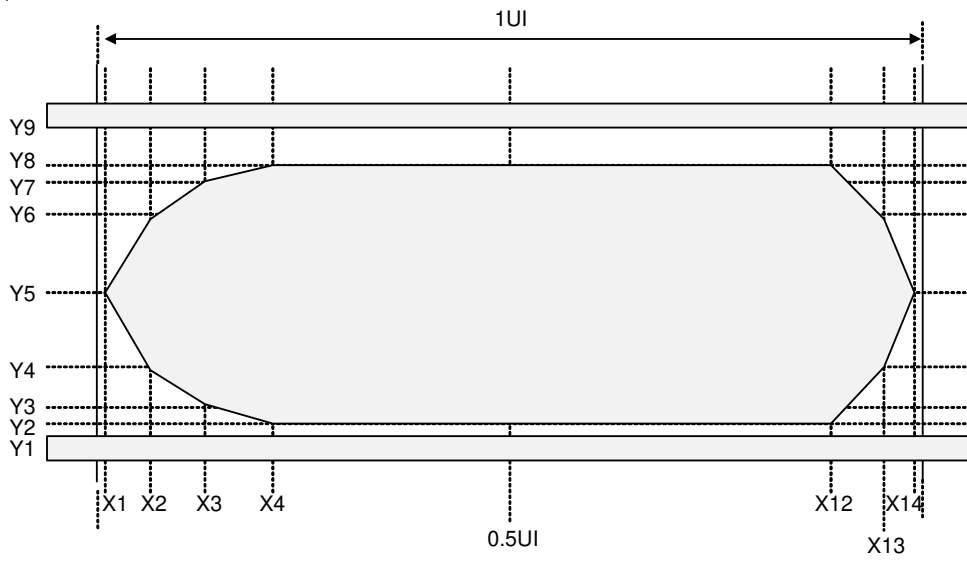


BMC TC Mask Definition, X Values						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Left Edge of Mask	X1Tx			0.015		UI
X2Tx point	X2Tx			0.07		UI
X3Tx point	X3Tx			0.15		UI
X4Tx point	X4Tx			0.25		UI
X5Tx point	X5Tx			0.35		UI
X6Tx point	X6Tx			0.43		UI
X7Tx point	X7Tx			0.485		UI
X8Tx point	X8Tx			0.515		UI
X9Tx point	X9Tx			0.57		UI
X10Tx point	X10Tx			0.65		UI
X11Tx point	X11Tx			0.75		UI
X12Tx point	X12Tx			0.85		UI
X13Tx point	X13Tx			0.93		UI
Right Edge of Mask	X14Tx			0.985		UI

BMC TC Mask Definition, Y Values						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Lower bound of Outer mask	Y1Tx			-0.075		V
Lower bound of inner mask	Y2Tx			0.075		V
Y3Tx point	Y3Tx			0.15		V
Y4Tx point	Y4Tx			0.325		V
Inner mask vertical midpoint	Y5Tx			0.5625		V
Y6Tx point	Y6Tx			0.8		V
Y7Tx point	Y7Tx			0.975		V
Y8Tx point	Y8Tx			1.04		V
Upper Bound of Outer mask	Y9Tx			1.2		V



BMC T<sub>x</sub> "ONE" Mask



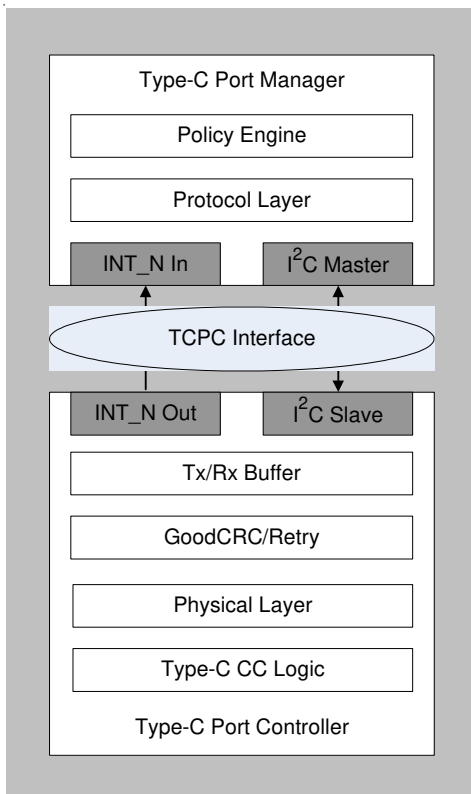
BMC T<sub>x</sub> "ZERO" Mask

### Application Information

Abbreviations :

Term	Description
BMC	Biphase Mark Coding
TCPC	Type-C Port Controller
TCPCI	Type-C Port Controller Interface
TCPM	Type-C Port Manager

#### Type-C Port Controller (TCPC) Interface :



The Type-C Port Controller Interface, TCPCI, is the interface between a Type-C Port Manager and a Type-C Port Controller.

#### The Controller Interface uses the I<sup>2</sup>C protocol :

- The TCPM is the only master on this I<sup>2</sup>C bus
- The TCPC is a slave device on this I<sup>2</sup>C bus
- Each Type-C port has its own unique I<sup>2</sup>C slave address. The TCPC shall have equal numbers of unique I<sup>2</sup>C slave addresses and supported Type-C ports
- The TCPC supports Fast-mode bus speed
- The TCPC has an open drain output, active low INT\_N Pin. This pin is used to indicate change of state, where INT\_N pin is asserted when any Alert Bits are set
- The TCPCI supports an I/O nominal voltage range of 1.8V and 3.3V
- The TCPC can auto-increment the I<sup>2</sup>C internal register address of the last byte transferred during a read independent of an ACK/NACK from the master
- The default I<sup>2</sup>C address shows below

1	0	0	1	1	1	0	RW
MSB							LSB

Register Map :

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x00	1	VENDOR_ID	7:0	VID[7:0]	0xCF	R	A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.
0x01	1		7:0	VID[15:8]	0x29	R	
0x02	1	PRODUCT_ID	7:0	PID[7:0]	0x11	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC.
0x03	1		7:0	PID[15:8]	0x17	R	
0x04	1	DEVICE_ID	7:0	DID[7:0]	0x73	R	A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the TCPC.
0x05	1		7:0	DID[15:8]	0x21	R	
0x06	1	USBTYPEC_REV	7:0	USBTYPEC_REV	0x11	R	Version number assigned by USB-IF (Currently at Revision 1.1 – 0001 0001)
0x07	1		7:0	Reserved	0	R	
0x08	1	USBPD_REV_VER	7:0	USBPD_VER	0x11	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x09	1		7:0	USBPD_REV	0x20	R	0010 0000 – Revision 2.0
0x0A	1	PD_INTERFACE_REV	7:0	PDIF_VER	0x10	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x0B	1		7:0	PDIF_REV	0x10	R	0010 0000 – Revision 1.0
0x10	1	ALERT	7	ALARM_VBUS_VOLTAGE_H	0	R	Not support.
			6	TX_SUCCESS	0	RW	0b: Cleared, 1b : Reset or SOP* message transmission successful.
			5	TX_DISCARD	0	RW	0b: Cleared, 1b: Reset or SOP* message transmission not sent due to incoming receive message.
			4	TX_FAIL	0	RW	0b: Cleared, 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.
			3	RX_HARD_RESET	0	RW	0b : Cleared, 1b : Received Hard Reset message
			2	RX_SOP_MSG_STATUS	0	RW	0b : Cleared, 1b : Receive status register changed
			1	POWER_STATUS	0	RW	0b : Cleared, 1b : Port status changed
			0	CC_STATUS	0	RW	0b : Cleared, 1b : CC status changed

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x11	1	ALERT	7	Reserved	0	R	
			6	Reserved	0	R	
			5	Reserved	0	R	
			4	Reserved	0	R	
			3	VBUS_SINK_DISCNT	0	R	Not support.
			2	RXBUF_OVFLOW	0	RW	0b : TCPC Rx buffer is functioning properly. 1b : TCPC Rx buffer has overflowed.
			1	FAULT	0	RW	0b : No Fault. 1b : A Fault has occurred. Read the FAULT_STATUS register.
			0	ALARM_VBUS_VOLTAGE_L	0	R	Not support.
0x12	1	ALERT_MASK	7	M_ALARM_VBUS_VOLTAGE_H	1	R	Not support.
			6	M_TX_SUCCESS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			5	M_TX_DISCARD	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			4	M_TX_FAIL	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			3	M_RX_HARD_RESET	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			2	M_RX_SOP_MSG_STATUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			1	M_POWER_STATUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			0	M_CC_STATUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
0x13	1	ALERT_MASK	7	Reserved	0	R	
			6	Reserved	0	R	
			5	Reserved	0	R	
			4	Reserved	0	R	
			3	M_VBUS_SINK_DISCNT	1	R	Not support.
			2	M_RXBUF_OVFLOW	1	RW	0b: Interrupt masked, 1b: Interrupt unmasked
			1	M_FAULT	1	RW	0b: Interrupt masked, 1b: Interrupt unmasked
			0	M_ALARM_VBUS_VOLTAGE_L	1	R	Not support.

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x14	1	POWER_STATUS_MASK	7	Reserved	0	R	Not support.
			6	M_TCPC_INITIAL	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			5	M_SRC_HV	1	R	Not support.
			4	M_SRC_VBUS	1	R	Not support.
			3	M_VBUS_PRESENT_DETC	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			2	M_VBUS_PRESENT	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			1	M_VCONN_PRESENT	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			0	M_SINK_VBUS	1	R	Not support.
0x15	1	FAULT_STATUS_MASK	7	M_VCON_OV	0	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			6	M_FORCE_OFF_VBUS	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			5	M_AUTO_DISC_FAIL	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			4	M_FORCE_DISC_FAIL	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			3	M_VBUS_OC	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			2	M_VBUS_OV	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			1	M_VCON_OC	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
			0	M_I2C_ERROR	1	RW	0b : Interrupt masked, 1b : Interrupt unmasked
0x18	1	CONFIG_STANDAR_OUTPUT	7	H_IMPEDENCE	0	R	Not support.
			6	DBG_ACC_CONNECT_O	0	R	Not support.
			5	AUDIO_ACC_CONNECT	0	R	Not support.
			4	ACTIVE_CABLE_CONNECT	0	R	Not support.
			3:2	MUX_CTRL	0	R	Not support.
			1	CONNECT_PRESENT	0	R	Not support.
			0	CONNECT_ORIENT	0	R	Not support.

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x19	1	TCPC_C ONTROL	7:5	Reserved	0	R	
			4	Reserved	0	R	
			3:2	I2C_CK_ STRETCH	00	R	Not support.
			1	BIST_TEST_ MODE	0	RW	0 : Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1 : BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.
			0	PLUG_ORIENT	0	RW	0b : When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b : When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. Required
0x1A	1	ROLE_C ONTROL	7	Reserved	0	R	
			6	DRP	0	RW	0b : No DRP. Bits B3..0 determine Rp/Rd/Ra settings 1b: DRP
			5:4	RP_VALUE	0	RW	00b : Rp default 01b : Rp 1.5A 10b : Rp 3.0A 11b : Reserved
			3:2	CC2	10	RW	00b : Reserved 01b : Rp (Use Rp definition in B5..4) 10b : Rd 11b : Open (dDisconnect or don't care) Set to 11b if enabling DRP in B7..6
			1:0	CC1	10	RW	00b : Reserved 01b : Rp (Use Rp definition in B5..4) 10b : Rd 11b : Open (dDisconnect or don't care) Set to 11b if enabling DRP in B7..6

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x1B	1	FAULT_C ONTROL	7	DIS_VCON_OV	0	RW	0b: Fault detection circuit enabled 1b: Fault detection circuit disabled
			6:5	Reserved	0	R	
			4	DIS_FORCE_ OFF_VBUS	0	R	Not support.
			3	DIS_VBUS_DIS C_FAULT_ TIMER	0	R	Not support.
			2	DIS_VBUS_OC	0	R	Not support.
			1	DIS_VBUS_OV	0	R	Not support.
			0	DIS_VCON_OC	0	RW	0b : Fault detection circuit enabled 1b : Fault detection circuit disabled
0x1C	1	POWER_ CONTRO L	7	Reserved	0	R	
			6	VBUS_VOL_ MONITOR	0	R	Not support.
			5	DIS_VOL_ ALARM	0	R	Not support.
			4	AUTO_DISC_ DISCNCT	0	R	Not support.
			3	BLEED_DISC	0	R	Not support.
			2	FORCE_DISC	0	R	Not support.
			1	VCONN_ POWER_SPT	0	RW	0b : TCPC delivers at least 1W on VCONN 1b : TCPC delivers at least the power indicated in DEVICE_CAPABILITIES.VCONNPower Supported
			0	EN_VCONN	0	RW	0b : Disable VCONN Source (default) 1b : Enable VCONN Source to CC Required



Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x1D	1	CC_STATUS	7:6	Reserved	0	R	
			5	DRP_STATUS	0	R	0b: the TCPC has stopped toggling or (ROLE_CONTROL.DRP = 00) 1b: the TCPC is toggling
			4	DRP_RESULT	0	R	0b: the TCPC is presenting Rp 1b: the TCPC is presenting Rd
			3:2	CC2_STATUS	0	R	<p>If (ROLE_CONTROL.CC2 = Rp) or (DrpResult = 0) 00b: SRC.Open (Open, Rp) 01b: SRC.Ra (below maximum vRa) 10b: SRC.Rd (within the vRd range) 11b: reserved</p> <p>If (ROLE_CONTROL.CC2 = Rd) or (DrpResult = 1) 00b: SNK.Open (Below maximum vRa) 01b: SNK.Default (Above minimum vRd-Connect) 10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A 11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A</p> <p>If ROLE_CONTROL.CC2 = Ra, this field is set to 00b If ROLE_CONTROL.CC2 = Open, this field is set to 00b</p> <p>This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVCONN = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.</p>

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x1D	1	CC_STATUS	1:0	CC1_STATUS	0	R	<p>If (ROLE_CONTROL.CC1 = Rp) or (DrpResult = 0)                      00b: SRC.Open (Open, Rp)                      01b: SRC.Ra (below maximum vRa)                      10b: SRC.Rd (within the vRd range)                      11b: reserved</p> <p>If (ROLE_CONTROL.CC1 = Rd) or DrpResult = 1)                      00b: SNK.Open (Below maximum vRa)                      01b: SNK.Default (Above minimum vRd-Connect)                      10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A                      11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A</p> <p>If ROLE_CONTROL.CC1 = Ra, this field is set to 00b                      If ROLE_CONTROL.CC1 = Open, this field is set to 00b</p> <p>This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVCONN = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.</p>

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x1E	1	POWER_STATUS	7	DBG_ACC_CONNECT	0	R	Not support.
			6	TCPC_INITIAL	0	R	0b : The TCPC has completed initialization and all registers are valid 1b : The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh
			5	SRC_HV	0	R	Not support.
			4	SRC_VBUS	0	R	Not support.
			3	VBUS_PRESENT_DETC	1	R	0b : VBUS Present Detection Disabled 1b : VBUS Present Detection Enabled (default)
			2	VBUS_PRESENT	0	R	0b : VBUS Disconnected 1b : VBUS Connected
			1	VCONN_PRESENT	0	R	0b: VCONN is not present 1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V
			0	SINK_VBUS	0	R	Not support.
0x1F	1	FAULT_STATUS	7	VCON_OV	0	RW	0b : Not in an over-voltage protection state 1b : Over-voltage fault latched.
			6	FORCE_OFF_VBUS	0	R	Not support.
			5	AUTO_DISC_FAIL	0	R	Not support.
			4	FORCE_DISC_FAIL	0	R	Not support.
			3	VBUS_OC	0	R	Not support.
			2	VBUS_OV	0	R	Not support.
			1	VCON_OC	0	RW	0b : No Fault detected 1b : Over-current VCONN fault latched
			0	I2C_ERROR	0	RW	
0x20	1		7:0	Reserved	0	R	
0x21	1		7:0	Reserved	0	R	
0x22	1		7:0	Reserved	0	R	
0x23	1	COMMAND	7:0	COMMAND	0	R	

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x24	1	DEVICE_CAPABILITIES_1L	7:5	ROLES_SUPPORT	110	R	000b : Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b : Source only 010b : Sink only 011b : Sink with accessory support (optional) 100b : DRP only 101b : Adapter or Cable (Ra) only 110b : Source, Sink, DRP, Adapter/Cable all supported 111b : Not valid
			4	ALL_SOP_SUPPORT	1	R	0b : All SOP* except SOP*_DBG/SOP*_DBG 1b : All SOP* messages are supported
			3	SOURCE_VCONN	1	R	0b : TCPC is not capable of switching VCONN 1b : TCPC is capable of switching VCONN
			2	CPB_SINK_VBUS	0	R	0b : TCPC is not capable controlling the sink path to the system load 1b : TCPC is capable of controlling the sink path to the system load
			1	SOURCE_HV_VBUS	0	R	0b : TCPC is not capable of controlling the source high voltage path to VBUS 1b : TCPC is capable of controlling the source high voltage path to VBUS
			0	SOURCE_VBUS	0	R	0b : TCPC is not capable of controlling the source path to VBUS 1b : TCPC is capable of controlling the source path to VBUS

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x25	1	DEVICE_CAPABILITIES_1H	7	Reserved	0	R	
			6	CPB_VBUS_OC	0	R	0b: VBUS OCP is not reported by the TCPC 1b: VBUS OCP is reported by the TCPC
			5	CPB_VBUS_OV	0	R	0b : VBUS OVP is not reported by the TCPC 1b : VBUS OVP is reported by the TCPC
			4	CPB_BLEED_DISC	0	R	0b : No Bleed Discharge implemented in TCPC 1b : Bleed Discharge is implemented in the TCPC
			3	CPB_FORCE_DISC	0	R	0b : No Force Discharge implemented in TCPC 1b : Force Discharge is implemented in the TCPC
			2	VBUS_MEASURE_ALARM	0	R	0b : No VBUS voltage measurement nor VBUS Alarms 1b : VBUS voltage measurement and VBUS Alarms
			1:0	SOURCE_RP_SUPPORT	10	R	00b : Rp default only 01b : Rp 1.5A and default 10b : Rp 3.0A, 1.5A, and default 11b : Reserved Rp values which may be configured by the TPCM via the ROLE_CONTROL register

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x26	1	DEVICE_CAPABILITYES_2L	7	SINK_DISCONNECT_DET	0	R	0b : VBUS_SINK_DISCONNECT_THRESH OLD not implemented (default: Use POWER_STATUS.VbusPresent=0b to indicate a Sink disconnect) 1b : VBUS_SINK_DISCONNECT_THRESH OLD implemented
			6	STOP_DISC_THD	0	R	0b : VBUS_STOP_DISCHARGE_THRESH OLD not implemented (default) 1b : VBUS_STOP_DISCHARGE_THRESH OLD implemented
			5:4	VBUS_VOL_ALARM_LSB	11	R	00 : TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01 : TCPC has 50mV LSB for its voltage alarm and uses only 9 bits.  VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0 ] are ignored by TCPC. 10: TCPC has 100mV LSB for its voltage alarm and uses only 8 bits.  VBUS_VOLTAGE_ALARM_HI_CFG[1: 0] and VBUS_VOLTAGE_ALARM_LO_CFG[1 :0] are ignored by TCPC. 11 : reserved
			3:1	VCONN_POWER	010	R	000b : 1.0W 001b : 1.5W 010b : 2.0W 011b : 3W 100b : 4W 101b : 5W 110b : 6W 111b : External
			0	VCONN_OCF	1	R	0b : TCPC is not capable of detecting a VCONN fault 1b : TCPC is capable of detecting a VCONN fault
0x27	1	DEVICE_CAPABILITYES_2H	7:0	Reserved	0	R	

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x28	1	STANDARD_INPUT_CAPABILITIES	7:3	Reserved	0	R	
			2	VBUS_EXT_OVF	0	R	0b : Not present in TCPC 1b : Present in TCPC
			1	VBUS_EXT_OCF	0	R	0b : Not present in TCPC 1b : Present in TCPC
			0	FORCE_OFF_VBUS_IN	0	R	0b : Not present in TCPC 1b : Present in TCPC
0x29	1	STANDARD_OUTPUT_CAPABILITIES	7	Reserved	0	R	
			6	CPB_DBG_ACC_IND	0	R	0b : Not present in TCPC 1b : Present in TCPC
			5	CPB_VBUS_PRESENT_MNT	0	R	0b : Not present in TCPC 1b : Present in TCPC
			4	CPB_AUDIO_ADT_ACC_IND	0	R	0b : Not present in TCPC 1b : Present in TCPC
			3	CPB_ACTIVE_CABLE_IND	0	R	0b : Not present in TCPC 1b : Present in TCPC
			2	CPB_MUX_CFG_CTRL	0	R	0b : Not present in TCPC 1b : Present in TCPC
			1	CPB_CONNECT_PRESENT	0	R	0b : Not present in TCPC 1b : Present in TCPC
			0	CPB_CONNECT_ORIENT	0	R	0b : Not present in TCPC 1b : Present in TCPC
0x2E	1	MESSAGE_HEADER_INFO	7:5	Reserved	0	R	
			4	CABLE_PLUG	0	RW	0b : Message originated from Source, Sink, or DRP 1b : Message originated from a Cable Plug
			3	DATA_ROLE	0	RW	0b : Sink 1b : Source
			2:1	USBPD_SPECREV	01	RW	00b : Revision 1.0 01b : Revision 2.0 10b – 11b : Reserved
			0	POWER_ROLE	0	RW	0b : Sink 1b : Source

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x2F	1	RECEIVE_DETECT	7	Reserved	0	R	
			6	EN_CABLE_RST	0	RW	0b : TCPC does not detect Cable Reset signaling (default) 1b : TCPC detects Cable Reset signaling
			5	EN_HARD_RST	0	RW	0b: TCPC does not detect Hard Reset signaling (default) 1b : TCPC detects Hard Reset signaling
			4	EN_SOP2DB	0	RW	0b: TCPC does not detect SOP_DBG'' message (default) 1b : TCPC detects SOP_DBG'' message
			3	EN_SOP1DB	0	RW	0b : TCPC does not detect SOP_DBG' message (default) 1b : TCPC detects SOP_DBG' message
			2	EN_SOP2	0	RW	0b : TCPC does not detect SOP'' message (default) 1b : TCPC detects SOP'' message
			1	EN_SOP1	0	RW	0b : TCPC does not detect SOP' message (default) 1b : TCPC detects SOP' message
			0	EN_SOP	0	RW	0b : TCPC does not detect SOP message (default) 1b : TCPC detects SOP message
0x30	1	RX_BYTE_COUNT	7:0	RX_BYTE_COUNT	0	RW	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register.
0x31	1	RX_BUF_FRAME_TYPE	7:3	Reserved	0	R	
			2:0	RX_FRAME_TYPE	0	R	Type of received frame 000b : Received SOP 001b : Received SOP' 010b : Received SOP'' 011b : Received SOP_DBG' 100b : Received SOP_DBG'' 110b : Received Cable Reset All others are reserved.
0x32	1	RX_BUF_HEADER_BYTE_0	7:0	RX_HEAD_0	0	R	Byte 0 (bits 7..0) of message header
0x33	1	RX_BUF_HEADER_BYTE_1	7:0	RX_HEAD_1	0	R	Byte 1 (bits 15..8) of message header
0x34	1	RX_BUF_OBJ1_BYTE_0	7:0	RX_OBJ1_0	0	R	Byte 0 (bits 7..0) of 1st data object



Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x35	1	RX_BUF_OBJ1_BYTE_1	7:0	RX_OBJ1_1	0	R	Byte 1 (bits 15..8) of 1st data object
0x36	1	RX_BUF_OBJ1_BYTE_2	7:0	RX_OBJ1_2	0	R	Byte 2 (bits 23..16) of 1st data object
0x37	1	RX_BUF_OBJ1_BYTE_3	7:0	RX_OBJ1_3	0	R	Byte 3 (bits 31..24) of 1st data object
0x38	1	RX_BUF_OBJ2_BYTE_0	7:0	RX_OBJ2_0	0	R	Byte 0 (bits 7..0) of 2st data object
0x39	1	RX_BUF_OBJ2_BYTE_1	7:0	RX_OBJ2_1	0	R	Byte 1 (bits 15..8) of 2st data object
0x3A	1	RX_BUF_OBJ2_BYTE_2	7:0	RX_OBJ2_2	0	R	Byte 2 (bits 23..16) of 2st data object
0x3B	1	RX_BUF_OBJ2_BYTE_3	7:0	RX_OBJ2_3	0	R	Byte 3 (bits 31..24) of 2st data object
0x3C	1	RX_BUF_OBJ3_BYTE_0	7:0	RX_OBJ3_0	0	R	Byte 0 (bits 7..0) of 3st data object
0x3D	1	RX_BUF_OBJ3_BYTE_1	7:0	RX_OBJ3_1	0	R	Byte 1 (bits 15..8) of 3st data object
0x3E	1	RX_BUF_OBJ3_BYTE_2	7:0	RX_OBJ3_2	0	R	Byte 2 (bits 23..16) of 3st data object
0x3F	1	RX_BUF_OBJ3_BYTE_3	7:0	RX_OBJ3_3	0	R	Byte 3 (bits 31..24) of 3st data object
0x40	1	RX_BUF_OBJ4_BYTE_0	7:0	RX_OBJ4_0	0	R	Byte 0 (bits 7..0) of 4st data object
0x41	1	RX_BUF_OBJ4_BYTE_1	7:0	RX_OBJ4_1	0	R	Byte 1 (bits 15..8) of 4st data object
0x42	1	RX_BUF_OBJ4_BYTE_2	7:0	RX_OBJ4_2	0	R	Byte 2 (bits 23..16) of 4st data object
0x43	1	RX_BUF_OBJ4_BYTE_3	7:0	RX_OBJ4_3	0	R	Byte 3 (bits 31..24) of 4st data object

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x44	1	RX_BUF_OBJ5_BYTE_0	7:0	RX_OBJ5_0	0	R	Byte 0 (bits 7..0) of 5st data object
0x45	1	RX_BUF_OBJ5_BYTE_1	7:0	RX_OBJ5_1	0	R	Byte 1 (bits 15..8) of 5st data object
0x46	1	RX_BUF_OBJ5_BYTE_2	7:0	RX_OBJ5_2	0	R	Byte 2 (bits 23..16) of 5st data object
0x47	1	RX_BUF_OBJ5_BYTE_3	7:0	RX_OBJ5_3	0	R	Byte 3 (bits 31..24) of 5st data object
0x48	1	RX_BUF_OBJ6_BYTE_0	7:0	RX_OBJ6_0	0	R	Byte 0 (bits 7..0) of 6st data object
0x49	1	RX_BUF_OBJ6_BYTE_1	7:0	RX_OBJ6_1	0	R	Byte 1 (bits 15..8) of 6st data object
0x4A	1	RX_BUF_OBJ6_BYTE_2	7:0	RX_OBJ6_2	0	R	Byte 2 (bits 23..16) of 6st data object
0x4B	1	RX_BUF_OBJ6_BYTE_3	7:0	RX_OBJ6_3	0	R	Byte 3 (bits 31..24) of 6st data object
0x4C	1	RX_BUF_OBJ7_BYTE_0	7:0	RX_OBJ7_0	0	R	Byte 0 (bits 7..0) of 7st data object
0x4D	1	RX_BUF_OBJ7_BYTE_1	7:0	RX_OBJ7_1	0	R	Byte 1 (bits 15..8) of 7st data object
0x4E	1	RX_BUF_OBJ7_BYTE_2	7:0	RX_OBJ7_2	0	R	Byte 2 (bits 23..16) of 7st data object
0x4F	1	RX_BUF_OBJ7_BYTE_3	7:0	RX_OBJ7_3	0	R	Byte 3 (bits 31..24) of 7st data object