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# 2.5MHz, Synchronous Boost Regulator with Bypass Mode

# **General Description**

The RT4803A allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-lon battery chemistries.

The RT4803A is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 2A. Quiescent current in Shutdown Mode is less than  $1\mu\text{A},$  which maximizes battery life. The regulator transitions smoothly between Bypass and normal Boost Mode. The device can be forced into Bypass Mode to reduce quiescent current.

The RT4803A is available in the WL-CSP-16B 1.67x1.67 (BSC) package.

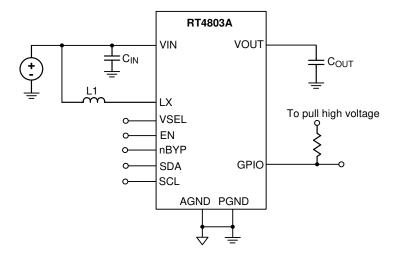
### **Features**

- 4 Few External Components: 0.47μH Inductor and 0603 Case Size Input and Output Capacitors
- Input Voltage Range: 1.8V to 5V
- Output Range from 2.85V to 4.4V
  - ▶ VSEL = L 3.15V
  - ▶ VSEL = H 3.4V
- Maximum Continuous Load Current : 2A at V<sub>IN</sub> > 2.65V Boosting V<sub>OUT</sub> to 3.35V
- Up to 96% Efficient
- True Bypass Operation when V<sub>IN</sub> > Target V<sub>OUT</sub>
- Internal Synchronous Rectifier
- True Load Disconnect when Shut Down
- Forced Bypass Mode
- V<sub>SEL</sub> Control to Optimize Target V<sub>OUT</sub>
- Short-Circuit Protection
- I<sup>2</sup>C Controlled Interface
- Ultra low Operating Quiescent Current
- Small WL-CSP 16B Package
- Discharge Function

# **Applications**

- Single-Cell Li-Ion, LiFePO4 Smart-Phones or Tablet
- 2.5G/3G/4G Mini-Module Data Cards

# **Simplified Application Circuit**



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# **Ordering Information**

# **Pin Configuration**

RT4803A 📮

Package Type

WSC: WL-CSP-16B 1.67x1.67 (BSC)

Note:

Richtek products are:

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

GPIO ĒΝ VIN VIN (B1) (B2) (B3) (B4) VŠEL ŠČL VOUT VOUT (C2) (C1) nBÝP SĎÁ ĽΧ D2)

(TOP VIEW)

WL-CSP-16B 1.67x1.67 (BSC)

AĞND PĞND PĞND PĞND

# **Marking Information**



38 : Product Code W: Date Code

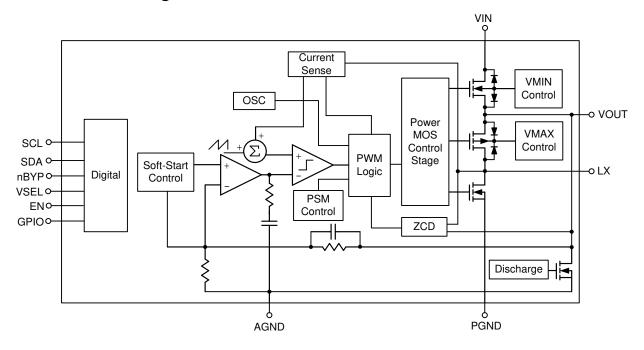
# **Functional Pin Description**

Pin No.	Pin Name	Pin Function
A1	EN	Enable. When this pin is HIGH, the circuit is enabled.
A2	GPIO	General purpose input/output.
A3, A4	VIN	Input voltage. Connect to Li-Ion battery input power source.
B1	VSEL	Output voltage select. When boost is running, this pin can be used to select output voltage
B2	SCL	Serial interface clock. (Pull down if I <sup>2</sup> C is non-used).
B3, B4	VOUT	Output voltage. Place Cout as close as possible to the device.
C1	nBYP	Bypass. This pin can be used to activate Forced Bypass Mode. When this pin is LOW, the bypass switches are turned on and the IC is otherwise inactive.
C2	SDA	Serial interface date line. (Pull down if I <sup>2</sup> C is non-used).
C3, C4	LX	Switching node. Connect to inductor.
D1	AGND	Analog ground. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
D2, D3, D4	PGND	Power ground. This is the power return for the IC. The C <sub>OUT</sub> bypass capacitor should be returned with the shortest path possible to these pins.

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# **Functional Block Diagram**





# Operation

The RT4803A combined built-in power transistors, synchronous rectification, and low supply current, it provides a compact solution for system using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed to a maximum load current of 2A. Quiescent current in Shutdown mode is less than 1µA, which maximizes battery life.

Mode		Depiction	Condition	
LIN 1		Linear startup 1	$V_{\text{IN}} > V_{\text{OUT}}$	
LIN LIN 2		Linear startup 2	VIN > VOUT	
Soft-Start		Boost soft-start Vout < Vout		
Boost		Boost mode	$V_{\text{OUT}} = V_{\text{OUT}(\text{MIN})}$	
Bypass		Bypass mode	$V_{\text{IN}} > V_{\text{OUT}(\text{MIN})}$	

### **LIN State**

When V<sub>IN</sub> is rising, it enters the LIN State. There are two parts for the LIN state. It provides maximum current for 1A to charge the Cout in LIN1, and the other one is for 2A in LIN2. By the way, the EN is pulled high and VIN > UVLO.

As the figure shown, if the timeout is over the specification, it will enter the Fault mode.

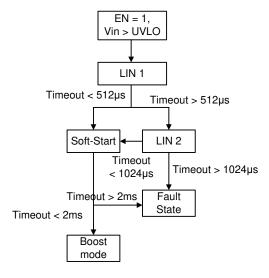


Figure 1. RT4803A State Chart

### Startup and Shutdown State

When V<sub>IN</sub> is rising and through the LIN state, it will enter the Startup state. If EN is pulled low, any function is turned-off in shutdown mode.

#### **Soft-Start State**

It starts to switch in Soft-start state. After the LIN state, output voltage is rising with the internal reference voltage.

There is a point, it will go to fault condition, if the large output capacitor is used and the timeout is over 2ms after the soft-start state.

#### **Fault State**

As the Figure 1 shown, it will enter to the Fault state as below.

- The timeout of LIN2 is over the 1024µs.
- ▶ It is over the 2ms when the state changed from Soft-start state to Boost mode.

It will be the high impedance between the input and output when the fault is triggered. A restart will be start after 1ms.

#### **Boost Mode**

There are two normal operation modes, one is the Boost mode, and the other one is Bypass mode. In the Boost mode, it provides the power to load by internal synchronous switches after the soft-start state.

### **Bypass Mode**

In Bypass mode, output voltage will increase with VIN when input voltage is rising after the soft-start state.

## **Bypass Mode Operation**

In automatic mode, it transits from Boost mode to Bypass mode. As the Figure 2 shown, there are three MOSFET (Q1 to Q3). The Q1 & Q2 is for Boost mode, it is used by Q3 for Bypass mode. V<sub>OUT</sub> will be followed the V<sub>IN</sub> when V<sub>IN</sub> is higher than the target output voltage. As the Figure 3 shown, it is transited by bypass MOSFET (Q3). Vout followed the VIN.

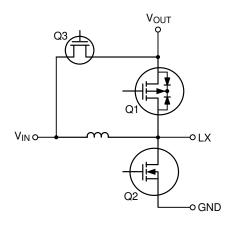


Figure 2. Boost Converter With Bypass Mode

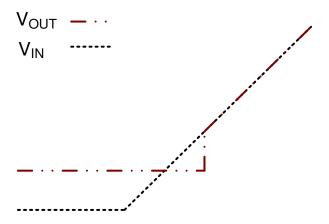


Figure 3. RT4803A mode changed

## **Force Pass-Through Mode**

When EN pulled high and nBYP pulled low. The device is active in the Force pass-through mode. It supplies current is approximately 15 $\mu$ A typ. From the battery, the device is short circuit protected by a current limit of 4000mA.

#### **VSEL**

It is concerned the minimum output voltage at the heavy load condition. There are two output voltage levels (3.15V & 3.4V) in Boost mode and Bypass mode. It can be selected by VSET, so it must not be floating.

## **GPIO**

GPIO is arranged to be either a mode selection or nRST/nFault pin. It also be controlled by Reg.0x01[3]. GPIO port configuration bit.

0: It supports manual reset input (nRST) and interrupt

generation output (nFault).

1: It is a input of device mode selection.

Fault output (open drain interrupt): Give a indication if the fault occurred (OTP, OCP, OVP...).

Manuel Reset Input: Drive the nRST and nFault. It will pull low, if the fault occurs.

MODE\_CTRL[1:0] in Register 0x01[1:0] set 2'b00, and GPIOCFG in Register 0x01[3] set 1'b1. GPIO pin must be configured as the mode selection input.

GPIO pin set Low : Auto mode GPIO pin set High : Force CCM

#### **OCP**

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, the OCP is cycle by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

### **OTP**

The converter has an over-temperature protection. When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be regulated until the junction temperature drops under the falling threshold.

### EN & nBYP

It is used to select mode. As the table 1 shown, there are four device states.

When both EN and nBYP pull low. It enters low IQ Bypass mode (4 $\mu$ A). When the EN pull low and nBYP pull high, it is forced shut-down and quiescent current is less than 1 $\mu$ A. It works in force pass-through mode, if the EN pulled high and nBYP pulled low. When EN and nBYP both pull high, the RT4803A is normal operation and enter automatic mode. There should be a delay time (>  $60\mu$ S) from EN pull high to nBYP pull high to guarantee normal automatic mode operation.

### **Discharge**

As the following figures shown, the RT4803A features the discharge function depends on the GPIO. The function is released when GPIO goes high 2ms later in

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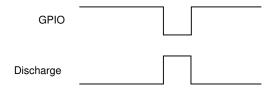
every modes but shut down mode.

In shut down mode, it is released right away when GPIO goes high.

Table 1

EN input	nBYP input	Device State
0	0	The device is shut down in pass-through mode featuring a low quiescent current down to ca. $4\mu A$ typ.
0	1	The device is shut down and the output voltage is reduced to a minimum value. The device shutdown current is approximately $1\mu A$ typ.
1	0	The device is active in forced pass-through mode. The device supply current is approximately 15 $\mu$ A typ. From the battery. The device is short circuit protected by a current limit of ca. 4000mA.
1	1	The device is active in auto mode (dc/dc boost, pass-through mode) The device supply current is approximately 55µA typ. from the battery

## In Shut down Mode (EN = 0, nBYP = 1)



### **In Other Modes**

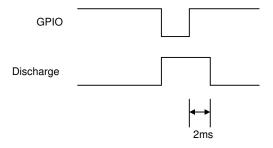


Figure 4. Discharge Function Diagram

### Table 2

EN	nBYP	GPIO	GPIO Pull High 2ms later Discharge Released Function	Mode
0	0	0	V	FBYP_Low IQ
0	1	0	X	Shut-down
1	0	0	V	FBYP
1	1	0	V	Boost + Auto Bypass



Absolute Maximum Ratings (Note 1)	
• VIN, VOUT to AGND	0.2V to 6V
• EN, VSEL, GPIO, nBYP to AGND	0.2V to to 6V
• LX	- (PGND – 0.2V) to 6V
• Power Dissipation, P <sub>D</sub> @ T <sub>A</sub> = 25°C	
WL-CSP-16B 1.67x1.67 (BSC)	- 2.09W
Package Thermal Resistance (Note 2)	
WL-CSP-16B 1.67x1.67 (BSC), $\theta$ JA	- 47.7°C/W
Lead Temperature (Soldering, 10 sec.)	- 260°C
Junction Temperature	- 150°C
Storage Temperature Range	- −65°C to 150°C
• ESD Susceptibility (Note 3)	
HBM (Human Body Model)	- 2kV
MM (Machine Model)	- 200V
CDM (Charge Device Model)	- 1kV
Recommended Operating Conditions (Note 4)	
Input Voltage Range	- 1.8V to 5V
Output Voltage Range	- 2.85V to 4.4V
Ambient Temperature Range	40°C to 85°C

• Junction Temperature Range ----- -40°C to 125°C

# **Electrical Characteristics**

 $(V_{IN} = 3V, V_{OUT} = 3.4V, T_A = 25^{\circ}C, unless otherwise specified)$ 

Parameter	Parameter Symbol Test Conditions		Min	Тур	Max	Unit
VIN Operation Range	VIN		1.8		5	V
VIN Quiescent Current	IQ	Auto Bypass Mode, V <sub>IN</sub> = 3.8V		35	70	μΑ
VIN Quiescent Current	IQ	Boost mode, I <sub>LOAD</sub> = 0mA, Switching, V <sub>IN</sub> = 3V		55	100	μΑ
VIN Quiescent Current	IQ	Force Bypass with LIQ, V <sub>IN</sub> = 3.6V		4	8	μΑ
VIN Quiescent Current	IQ	Force Bypass without LIQ, V <sub>IN</sub> = 3.6V		15	25	μΑ
VIN Shutdown Current	I <sub>SHDN</sub>	EN = 0V, nBYP = H, V <sub>IN</sub> = 3.6V			1	μА
VOUT to VIN Reverse Leakage	ILK	Vout = 5V, EN = nBYP = H, VIN < Vout		0.2	1	μА
VOUT Leakage Current	I <sub>LK_OUT</sub>	$V_{OUT} = 0V$ , $EN = 0V$ , $V_{IN} = 4.2V$		0.1	1	μΑ
VOUT Discharge Impedance	R_DIS_OUT	GPIO = L		80		Ω
Under Voltage Lock Out	Vuvlo	V <sub>IN</sub> Rising		1.6	1.8	V
Under Voltage Lock Out Hysteresis	Vuvlo_HYS			200		mV
GPIO Low	V <sub>GPIO</sub>	I <sub>GPIO</sub> = 5mA			0.4	V

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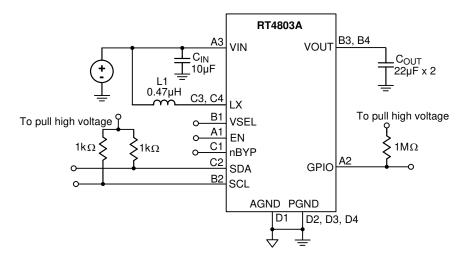
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
GPIO Leakage Current	I <sub>GPIO_LK</sub>	V <sub>GPIO</sub> = 5V			1	μА
Logic Level High EN, VSEL, nBYP, SCL, SDA, GPIO	VIH		1.2			V
Logic Level Low EN, VSEL, nBYP, SCL, SDA, GPIO	V <sub>IL</sub>				0.4	V
Output Voltage Accuracy	VREG	Vout – V <sub>IN</sub> > 100mV, PWM	-2		2	%
Minimum On Time	Ton	VIN = 3V, V <sub>OUT</sub> = 3.5V, I <sub>LOAD</sub> > 1000mA		80		ns
Maximum Duty Cycle	D <sub>MAX</sub>		40			%
Switching Frequency	f <sub>SW</sub>	V <sub>IN</sub> = 2.65V, V <sub>OUT</sub> = 3.5V, I <sub>LOAD</sub> = 1000mA	2	2.5	3	MHz
Boost Valley Current Limit	IcL	V <sub>IN</sub> = 2.9V	3.5	4	4.5	Α
Soft-Start Input Current Limit	ISS_PK	LIN1		1000		mA
Soft-Start Input Current Limit	I <sub>SS_PK</sub>	LIN2		2000		mA
Pass Through Mode Current Limit	I <sub>BPCL</sub>	V <sub>IN</sub> = 3.2V		4		Α
N-Channel Boost Switch RDS(ON)	R <sub>DSN</sub>	V <sub>IN</sub> = 3.2V, V <sub>OUT</sub> = 3.5V		60	95	mΩ
P-Channel Boost Switch RDS(ON)	R <sub>DSP</sub>	V <sub>IN</sub> = 3.2V, V <sub>OUT</sub> = 3.5V		40	80	mΩ
N-Channel Bypass Switch RDS(ON)	R <sub>DSP_BYP</sub>	V <sub>IN</sub> = 3.2V, V <sub>OUT</sub> = 3.5V		40	60	mΩ
Hot Die Trigger Threshold	T <sub>HD</sub>			100		°C
Hot Die Release Threshold	T <sub>HDR</sub>			90		°C
Over Temperature Protection	T <sub>OTP</sub>			160		°C
Over Temperature Protection Hysteresis	T <sub>OTP_HYS</sub>			20		°C
FAULT Restart Time	T <sub>RST</sub>			1		ms

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

- Note 2.  $\theta_{JA}$  is measured at  $T_A = 25$ °C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.
- Note 3. Devices are ESD sensitive. Handling precaution recommended.
- **Note 4.** The device is not guaranteed to function outside its operating conditions.



# **Typical Application Circuit**

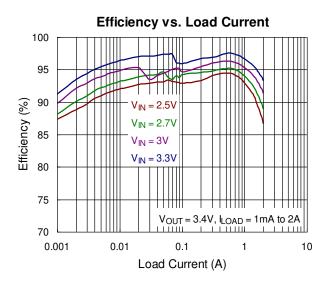


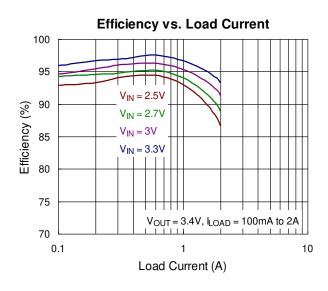
### **BOM of Test Board**

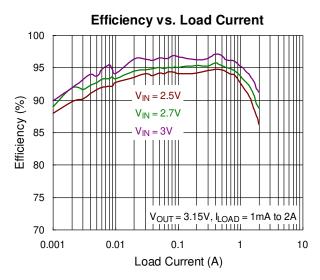
Reference	Description	Manufacturer	Package	Parameter	Тур.	Unit
C <sub>IN</sub>	10μF/16V/X5R	Taiyo : EMK212ABJ106KG	0805	С	10	μF
Соит	22μF/10V/X5R	Taiyo : LMK212BBJ226MG	0805	С	22	μF
1.4	0.47 +200/	TOKO : DFE2520F-R47M	2520	L	0.47	μН
L1 0.47μH, ±20%		10KU . DFE2520F-R4/M	2520	DCR (Series R)	29	mΩ

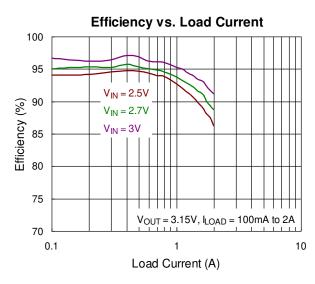


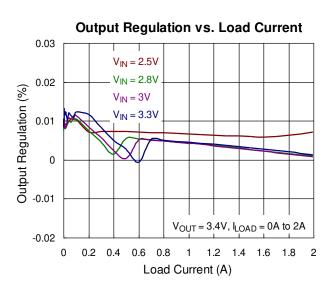
# **Typical Operating Characteristics**

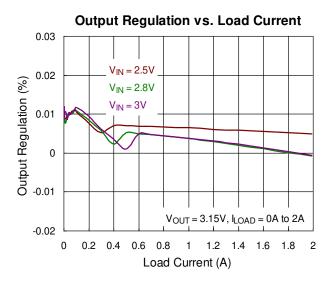




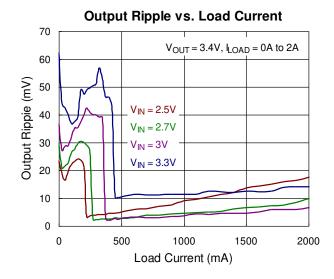


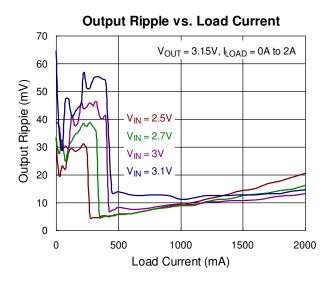


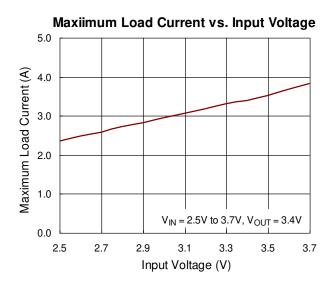


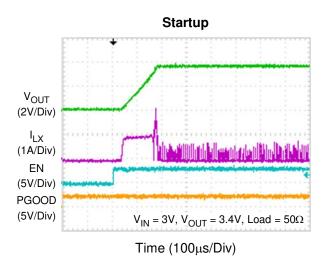


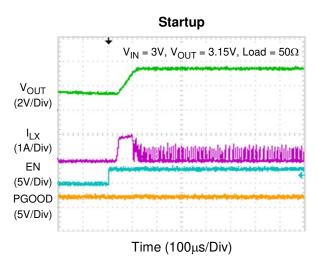


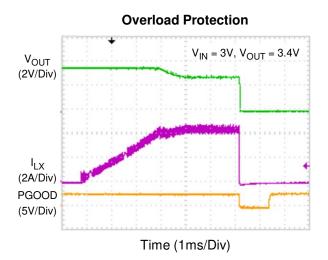








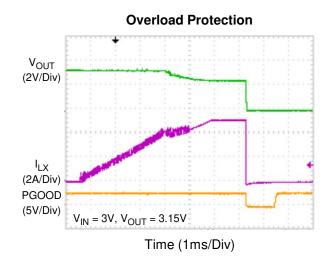


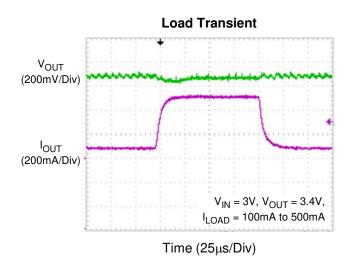


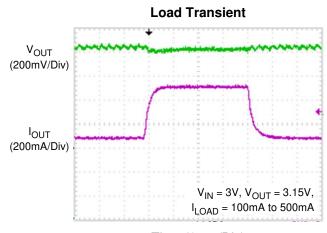
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Time (25µs/Div)



# **Application Information**

### **Enable**

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

### **Soft-Start State**

After the successful completion of the LIN state ( $V_{OUT} \ge V_{IN} - 300 mV$ ).

During Soft-Start state,  $V_{OUT}$  is ramped up by Boost internal loop. If  $V_{OUT}$  fails to reach target value during the Soft-Start period for more than 2ms, a fault condition is declared.

### **Output Voltage Setting**

User can select the output voltage level by VSEL and I2C. If the VSEL pulled low, the default is 3.15V, and if it pulled high, the default is 3.4V.

The output voltage range is from 2.85V to 4.4V.

#### **Power Save Mode**

PSM is the way to improve efficiency at light load.

When the output voltage is lower than a set threshold voltage, the converter will operate in PSM.

It raises the output voltage with several pulses until the loop exits PSM.

### **Under-Voltage Lockout**

The under-voltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the power switches under undefined conditions and prevents the battery from deep discharge. VIN voltage must be greater than 1.7V to enable the converter. During operation, if VIN voltage drops below 1.6V, the converter is disabled until the supply exceeds the UVLO rising threshold. The RT4803A automatically

restarts if the input voltage recovers to the input voltage UVLO high level.

### **Thermal Shutdown**

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over temperature threshold.

#### **Inductor Selection**

The recommended nominal inductance value is  $0.47\mu H.$ 

It is recommended to use inductor with dc saturation current ≥ 3500mA

### **Input Capacitor Selection**

At least a  $10\mu F$  input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit for LX. And at least a  $1\mu F$  ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

### **Output Capacitor Selection**

At least  $22\mu F$  x 2 capacitors is recommended to improve  $V_{OUT}$  ripple.

Output voltage ripple is inversely proportional to COUT.

Output capacitor is selected according to output ripple which is calculated as :

$$\begin{split} &V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}} \\ &\text{and} \\ &t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \\ &\text{therefore}: \\ &C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}} \\ &\text{and} \\ &t_{SW} = \frac{1}{f_{out}} \end{split}$$

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The maximum V<sub>RIPPLE</sub> occurs when V<sub>IN</sub> is at minimum and ILOAD is at maximum.

### **Output Discharge Function**

About this function, it depends on the GPIO pin. When GPIO pin pull high 2ms later. The function starts to release but in the shut-down mode. In the shut-down mode, it is not exist.

This feature prevents residual charge voltages on capacitor connected to VOUT pins, which may impact proper power up of the system.

### **Current Limit**

The RT4803A employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (Vout - Vin) / Vout ratio. The output voltage decreases when further loading current increase. As the following figure shown, the current limit function is implemented by the scheme.

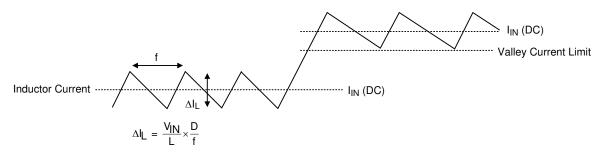


Figure 5. Inductor Currents In Current Limit Operation

### **Protection**

The RT4803A features some protections, such as OCP, OVP, UVP and OTP. As the table shown, it is described the protection actions.

Protection Type	Threshold Refer to Electrical Spec.	Protection Method	Shut Down Delay Time	Reset Method
OCP	IL > 4A	Turn on UG until IL < 4A	2ms	After FAULT 1ms
OVP	VIN > 6V	Turn off UG, LG, BYP_MOS	No delay	VIN < 5.7V
UVP	VIN <1.6V	Turn off UG, LG, BYP_MOS	No delay	VIN>1.7V
ОТР	TEMP > 160°C	Turn off UG, LG, BYP_MOS	No delay	OTP Hysteresis = 20°C

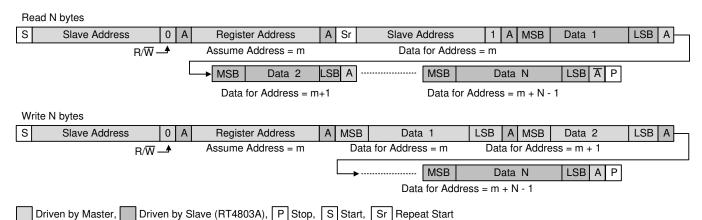


## Register Table Lists [Slave address = 1110101 (0x75)]

Name	Address	Description
CONFIG	0x01	MODE control & Spread modulation control
VOUTFLOOR	0x02	Output Voltage Selection
VOUTROOF 0x03		Output Voltage Selection
ILIMSET	0x04	Set current limit & Soft-start current limit
STATUS	0x05	Read IC status

## I<sup>2</sup>C Interface

The RT4803A I<sup>2</sup>C slave address is 1110101 (7bits). The I<sup>2</sup>C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream  $(N \ge 1)$  is shown below :



# RT4803A



00000									
	set 0x01				CONFIG		Т		
Bits	7	6	5	4	3	2	1	0	
Name	RESET	ENABLE<1>	ENABLE<0>	RESERVED	GPIOCFG	SSFM	MODE_CTRL <1>	MODE_CTRL <0>	
Reset	0	0	0	0	0	0	0	1	
Type	RW	RW	RW	RW	RW	RW	RW	RW	
Off	set 0x02		VOUTFLOC						
Bits	7	6	5	4	3	2	1	0	
Name	RESERVED	RESERVED	RESERVED	VSEL<4>	VSEL<3>	VSEL<2>	VSEL<1>	VSEL<0>	
Reset	0	0	0	0	0	1	1	0	
Туре	RW	RW	RW	RW	RW	RW	RW	RW	
Off	set 0x03				VOUTROOF				
Bits	7	6	5	4	3	2	1	0	
Name	RESERVED	RESERVED	RESERVED	VSEL<4>	VSEL<3>	VSEL<2>	VSEL<1>	VSEL<0>	
Reset	0	0	0	0	1	0	1	1	
Туре	RW	RW	RW	RW	RW	RW	RW	RW	
Off	set 0x04				ILIMSET				
Bits	7	6	5	4	3	2	1	0	
Name	RESERVED	RESERVED	ILIM_OFF	SOFT_START	ILIM<3>	ILIM<2>	ILIM<1>	ILIM<0>	
Reset	0	0	0	1	1	1	0	1	
Туре	RW	RW	RW	RW	RW	RW	RW	RW	
Off	set 0x05				et 0x05 STATUS				
Bits	7	6	5	4	3	2	1	0	
Name	TSD	HOTDIE	DCDCMODE	OPMODE	ILIMPT	ILIMBST	FAULT	PGOOD	
Reset	0	0	0	0	0	0	0	0	
Туре	RO	RO	RO	RO	RO	RO	RO	RO	



Name Function Addr		Function	Addr	
CON	NFIG	MODE control & Spread modulation control	0x01	
Bit	Mode	Name	Reset	Description
7	R/W	RESET	0	Normal operation.     All registers are reset to default value.
[6:5]	R/W	ENABLE[1 : 0]	0	<ul> <li>00 : Device operation follows hardware control signal. (refer to table 1)</li> <li>01 : Device operation in auto transition mode (boost/bypass). regardless of the nBYP control signal (EN = 1).</li> <li>10 : Device is forced in pass-through mode regardless of the nBYP control signal (EN = 1).</li> <li>11 : Device is in shutdown mode. Regardless of the nBYP control signal (EN = 1).</li> </ul>
4	R/W	Reserved	0	
3	R/W	GPIOCFG	0	GPIO port is configured to support manual reset input (nRST) and interrupt generation output (nFAULT).     GPIO port is configured as a device mode selection input.
2	R/W	SSFM	0	Spread spectrum modulation is disabled.     Spread spectrum modulation is enabled in PWM mode.
[1:0]	R/W	MODE_CTRL[1:0]	01	<ul> <li>00 : Device operation follows hardware control signal (GPIO must be configured as mode selection input).</li> <li>01 : PFM with automatic transition into PWM operation.</li> <li>10 : Forced PWM operation.</li> <li>11 : PFM with automatic transition into PWM operation (VSEL = L), forced PWM operation (VSEL = H).</li> </ul>
Na	me	Function	Addr	
VOUTI	FLOOR	Output Voltage Selection	0x02	
Bit	Mode	Name	Reset	Description
[7:5]	R/W	Reserved	000	
[4:0]	R/W	VOUT[4 : 0]	00110	00000 : Vout = 2.85V 00001 : Vout = 2.9V 00010 : Vout = 2.95V 00011 : Vout = 3V 00100 : Vout = 3.05V  00110 : Vout = 3.15V (default)  11111 : Vout = 4.4V

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Name		Function	Addr			
VOUTROOF		Output Voltage Selection	0x03			
Bit	Mode	Name	Reset	Description		
[7:5]	R/W	Reserved	000			
[4:0]	R/W	VOUT[4 : 0]	01011	00000: V <sub>OUT</sub> = 2.85V 00001: V <sub>OUT</sub> = 2.9V 00010: V <sub>OUT</sub> = 2.95V 00011: V <sub>OUT</sub> = 3V 00100: V <sub>OUT</sub> = 3.05V  01011: V <sub>OUT</sub> = 3.4V (default)  11111: V <sub>OUT</sub> = 4.4V		
Na	me	Function	Addr			
ILIMSET		Set current limit & Softstart current limit	0x04			
Bit	Mode	Name	Reset	Description		
[7:6]	R/W	Reserved	00			
5	R/W	ILIM_OFF	0	0 : Current Limit Enabled. 1 : Current Limit Disabled.		
4	R/W	Soft-Start	1	Boost soft-start current is limited per ILIM bit settings.     Boost soft-start current is limited to ca. 1250mA inductor valley current.		
[3:0]	R/W	ILIM[3 : 0]	1101	1000:1500mA 1001:2000mA 1010:2500mA 1011:3000mA 1100:3500mA 1101:4000mA (default) 1110:4500mA 1111:5000mA		



Name		Function	Addr		
STATUS		Read IC status	0x05		
Bit	Mode	Name	Reset	Description	
7	R	TSD	0	O : Normal operation.     1 : Thermal shutdown tripped. The flag is reset after readout.	
6	R	HOTDIE	0	0 : T <sub>J</sub> < 115°C. 1 : T <sub>J</sub> > 115°C.	
5	R	DCDCMODE	0	0 : Device operates in PFM mode. 1 : Device operates in PWM mode.	
4	R	OPMODE	0	0 : Device operates in pass-through mode. 1 : Device operates in dc/dc mode.	
3	R	ILIMPT	0	Normal operation.     Indicates that the bypass FET current limit has triggered. This flag is reset after readout.	
2	R	ILIMBST	0	Normal operation.     Indicates that the average input current limit has triggered for 1.5ms in dc/dc boost mode. This flag is reset after readout.	
1	R	FAULT	0	Normal operation.     Indicates that a fault condition has occurred. This flag is reset after readout.	
0	R	PGOOD	0	O: Indicates the output voltage is out of regulation.     I: Indicates the output voltage is within its nominal range. This bit is set if the converter is forced in pass-through mode.	



#### **Thermal Considerations**

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where T<sub>J(MAX)</sub> is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For WL-CSP-16B 1.67x1.67 (BSC) package, the thermal resistance, θ<sub>JA</sub>, is 47.7°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^{\circ}C$  can be calculated by the following formula:

 $P_{D(MAX)} = (125^{\circ}C - 25^{\circ}C) / (47.7^{\circ}C/W) = 2.09W \text{ for}$ WL-CSP-16B 1.67x1.67 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed T<sub>J(MAX)</sub> and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

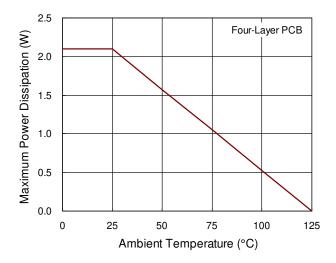


Figure 6. Derating Curve of Maximum Power Dissipation

### **Layout Consideration**

The PCB layout is an important step to maintain the high performance of the RT4803A.

Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the RT4803A through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4803A, the following PCB layout guidelines must be strictly followed.

- ▶ Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- ▶ For thermal consider, it needed to maximize the pure area for the power stage area besides the LX.

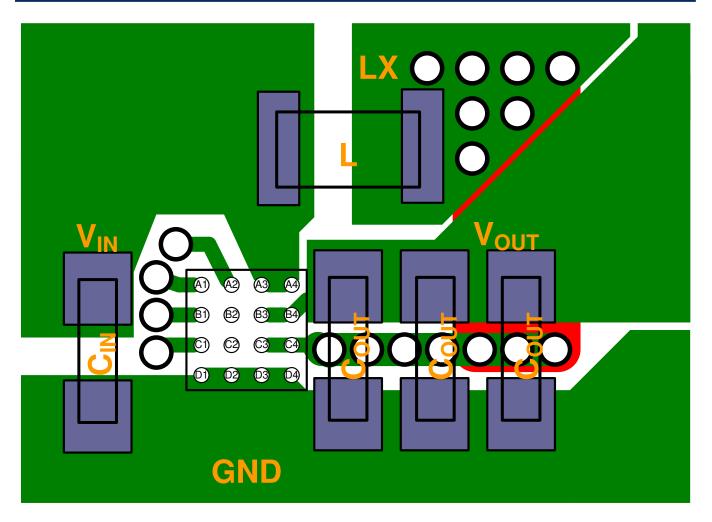
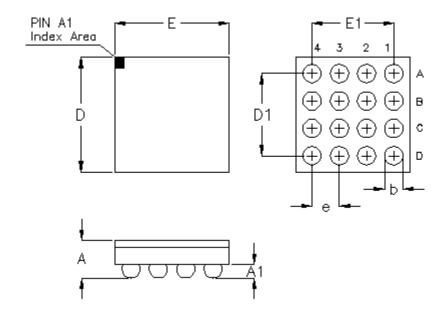


Figure 7. PCB Layout Guide

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## **Outline Dimension**



Cymahal	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	0.500	0.600	0.020	0.024	
A1	0.170	0.230	0.007	0.009	
b	0.240	0.300	0.009	0.012	
D	1.620	1.720	0.064	0.068	
D1	1.2	200	0.047		
E	1.620	1.720	0.064	0.068	
E1	1.2	200	0.047		
е	0.4	100	0.016		

WL-CSP-16B 1.67x1.67 (BSC)

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